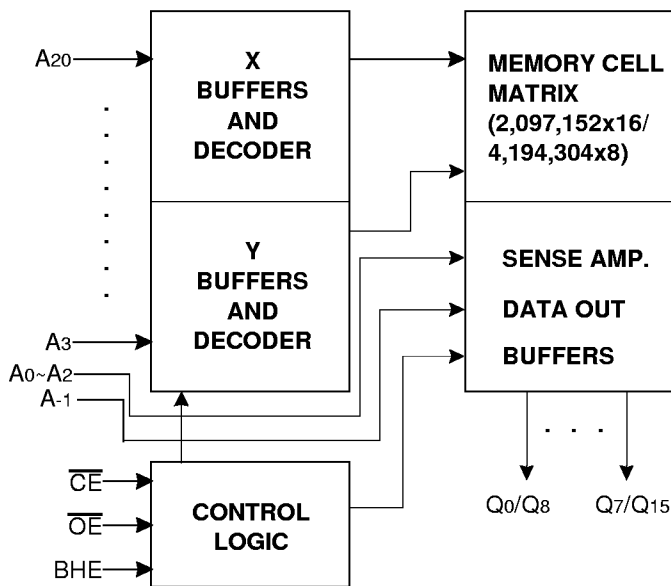


32M-Bit (4Mx8 /2Mx16) CMOS MASK ROM

FEATURES

- Switchable organization
4,194,304x8(byte mode)
2,097,152x16(word mode)
- Fast access time
Random Access : 100ns(Max.)
Page Access : 30ns(Max.)
- Supply voltage : single +5V
- Current consumption
Operating : 150mA(Max.)
Standby : 50μA(max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
-. KM23C32005BG : 44-SOP-600

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A0 - A2	Page Address Inputs
A3 - A20	Address Inputs
Q0 - Q14	Data Outputs
Q15 /A-1	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte selection
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

GENERAL DESCRIPTION

The KM23C32005BG is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 4,194,304x8 bit(byte mode) or as 2,097,152x16 bit(word mode) depending on BHE voltage level.(See mode selection table)

This device includes page read mode function, page read mode allows four to eight words of data to read fast in the same page, \overline{CE} and A3 ~ A20 should not be changed.

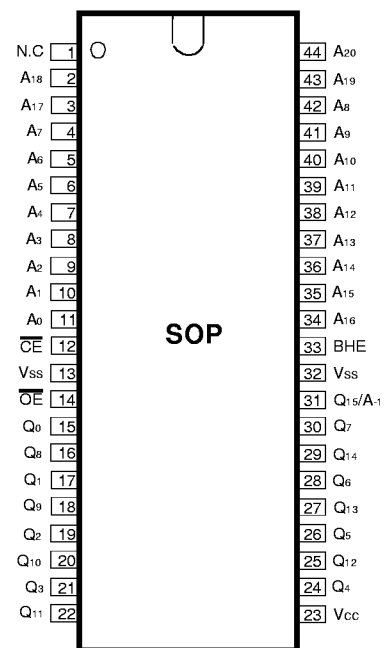
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23C32005BG is packaged in a 44-SOP.

PIN CONFIGURATION



KM23C32005BG

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN	-0.3 to +7.0	V
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-55 to +150	°C

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, TA=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	ICC	$\overline{CE}=\overline{OE}=V_{IL}$ all outputs open	-	150	mA
Standby Current(TTL)	ISB1	$\overline{CE}=V_{IH}$, all outputs open	-	1	mA
Standby Current(CMOS)	ISB2	$\overline{CE}=V_{CC}$, all outputs open	-	50	μA
Input Leakage Current	ILI	VIN=0 to Vcc	-	10	μA
Output Leakage Current	ILO	VOUT=0 to Vcc	-	10	μA
Input High Voltage, All Inputs	VIH		2.2	Vcc+0.3	V
Input Low Voltage, All Inputs	VIL		-0.3	0.8	V
Output High Voltage Level	VOH	I _{OH} =-400μA	2.4	-	V
Output Low Voltage Level	VOL	I _{OL} =2.1mA	-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input pins(V_{IH}) is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.

MODE SELECTION

\overline{CE}	\overline{OE}	BHE	Q15/A-1	Mode	Data	Power
H	X	X	X	Standby	High-Z	Standby
L	H	X	X	Operating	High-Z	Active
L	L	H	Output	Operating	Q0~Q15 : Dout	Active
		L	Input	Operating	Q0~Q7 : Dout Q8~Q14 : Hi-Z	Active

CAPACITANCE(TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	COUT	VOUT=0V	-	12	pF
Input Capacitance	CIN	VIN=0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

AC CHARACTERISTICS (TA=0°C to +70°C, Vcc=5V±10%, unless otherwise noted.)

TEST CONDITIONS

Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and CL=100pF

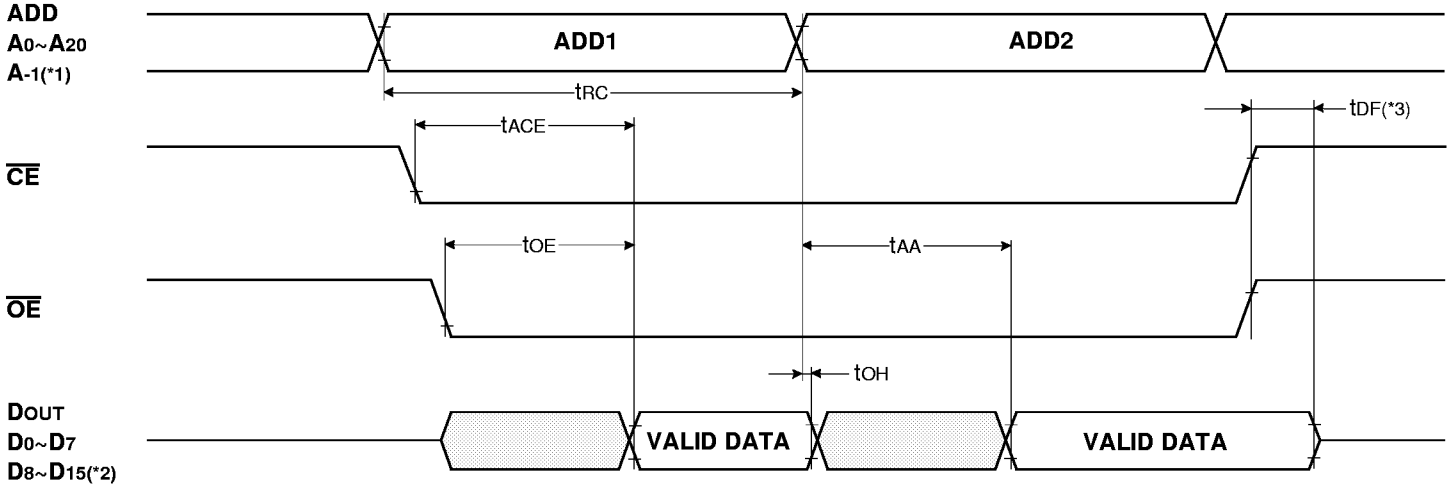
READ CYCLE

Item	Symbol	KM23C32005BG-10		KM23C32005BG-12		KM23C32005BG-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	100		120		150		ns
Chip Enable Access Time	tACE		100		120		150	ns
Address Access Time	tAA		100		120		150	ns
Page Address Access Time	tPA		30		50		70	ns
Output Enable Access Time	tOE		30		50		70	ns
Output or Chip Disable to Output High-Z	tDF		20		20		30	ns
Output Hold from Address Change	tOH	0		0		0		ns

NOTE : Page Address ; A0, A1, A2.

TIMING DIAGRAM

READ

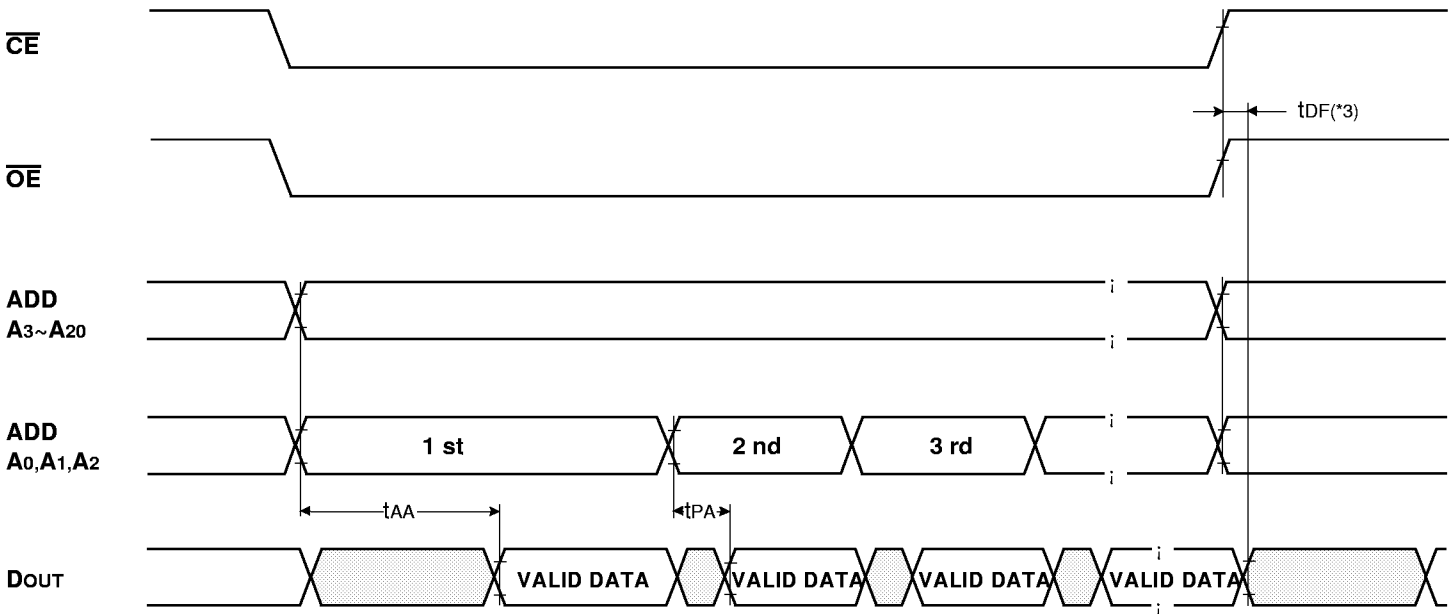


NOTES : *1. Byte Mode only. A-1 is Least Significant Bit Address.(BHE=V_{IL})

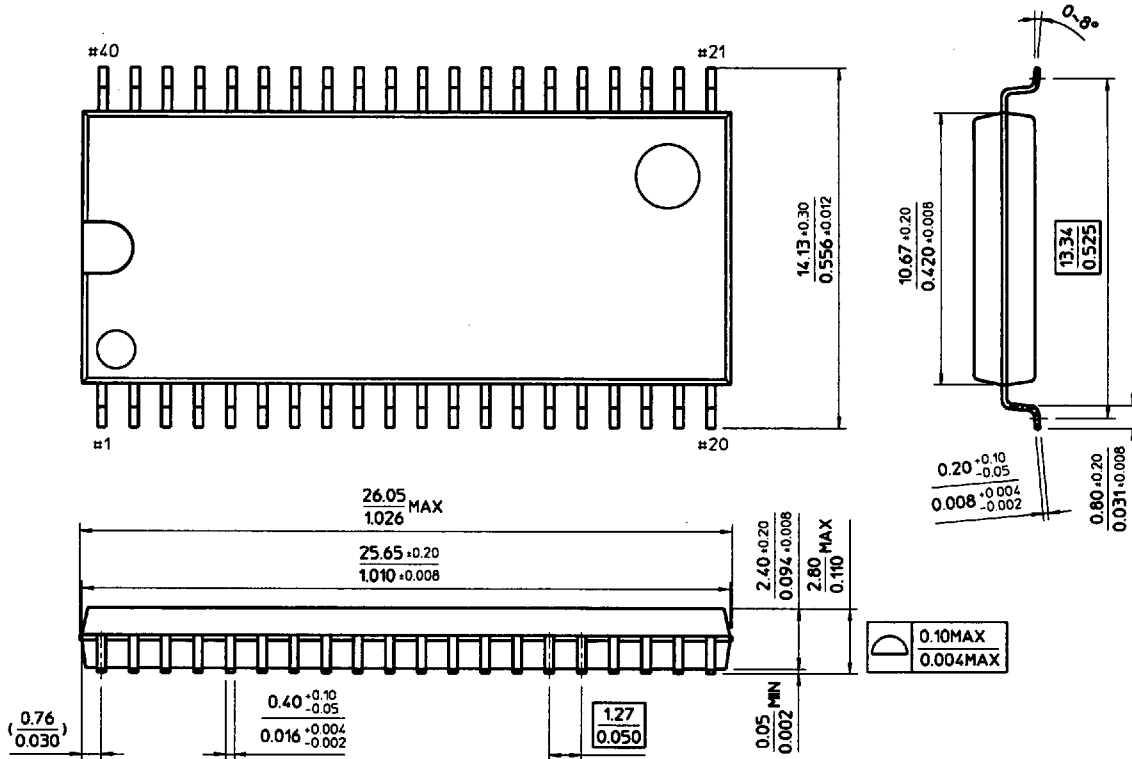
*2. Word Mode only.(BHE=V_{IH})

*3. t_{DF} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.

PAGE READ



40-SOP-525



44-SOP-600

