NEC

MOS INTEGRATED CIRCUIT

μPD4382161, 4382181, 4382321, 4382361

8M-BIT CMOS SYNCHRONOUS FAST SRAM
FLOW THROUGH OPERATION

Description

The μPD4382161 is a 524,288-word by 16-bit, the μPD4382181 is a 524,288-word by 18-bit, the μPD4382321 is a 262,144-word by 32-bit and the μPD4382361 is a 262,144-word by 36-bit synchronous static RAM fabricated with advanced CMOS technology using N-channel four-transistor memory cell.

The μPD4382161, μPD4382181, μPD4382321 and μPD4382361 integrate unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (CLK).

The μPD4382161, μPD4382181, μPD4382321 and μPD4382361 are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as cache and buffer memory.

ZZ has to be set LOW at the normal operation. When ZZ is set HIGH, the SRAM enters Power Down State (“Sleep”). In the “Sleep” state, the SRAM internal state is preserved. When ZZ is set LOW again, the SRAM resumes normal operation.

The μPD4382161, μPD4382181, μPD4382321 and μPD4382361 are packaged in 100-pin plastic LQFP with a 1.4 mm package thickness for high density and low capacitive loading.

Features

- 3.3 V (Chip) / 3.3 V or 2.5 V (I/O) Supply
- Synchronous Operation
- Internally self-timed Write control
- Burst Read / Write: Interleaved Burst and Linear Burst Sequence
- Fully Registered Inputs for Flow Through Operation
- All Registers triggered off Positive Clock Edge
- 3.3 V or 2.5 V LVTTL Compatible: All Inputs and Outputs
- Fast Clock Access Time: 8.5 ns (100 MHz), 9 ns (90 MHz)
- Asynchronous Output Enable: /G
- Burst Sequence Selectable: MODE
- Sleep Mode: ZZ (ZZ = Open or Low: Normal Operation)
- Separate Byte Write Enable: /BW1 - /BW4 (μPD4382321, μPD4382361), /BW1 - /BW2 (μPD4382161, μPD4382181), /BWE
  Global Write Enable: /GW
- Three Chip Enables for Easy Depth Expansion
- Common I/O Using Three State Outputs

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The mark ★ shows major revised points.

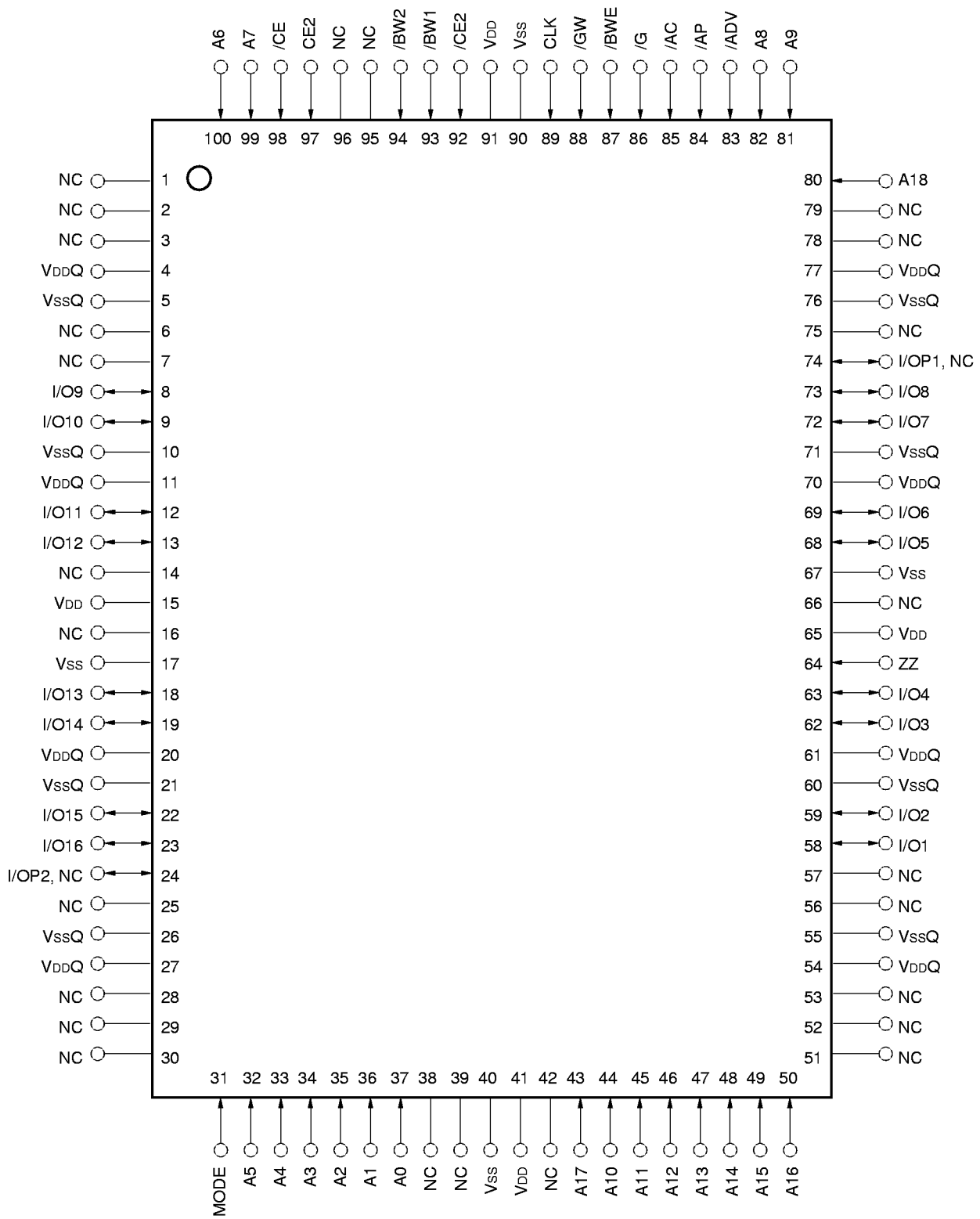
★ Ordering Information

Part number	Access Time	Clock Frequency	Core Supply Voltage	I/O Interface	Package
μPD4382161GF-A85	8.5 ns	100 MHz	3.3 ± 0.165 V	3.3 V or 2.5 V LVTTL	100-pin plastic LQFP (14x20 mm)
μPD4382161GF-A90	9.0 ns	90 MHz			
μPD4382181GF-A85	8.5 ns	100 MHz			
μPD4382181GF-A90	9.0 ns	90 MHz			
μPD4382321GF-A85	8.5 ns	100 MHz			
μPD4382321GF-A90	9.0 ns	90 MHz			
μPD4382361GF-A85	8.5 ns	100 MHz			
μPD4382361GF-A90	9.0 ns	90 MHz			

Pin Configuration (Marking Side)

/xxx indicates active low signal.

100-pin plastic LQFP (14 x 20 mm)
[μPD4382161GF, μPD4382181GF]



Pin Identification

[μPD4382161GF, μPD4382181GF]

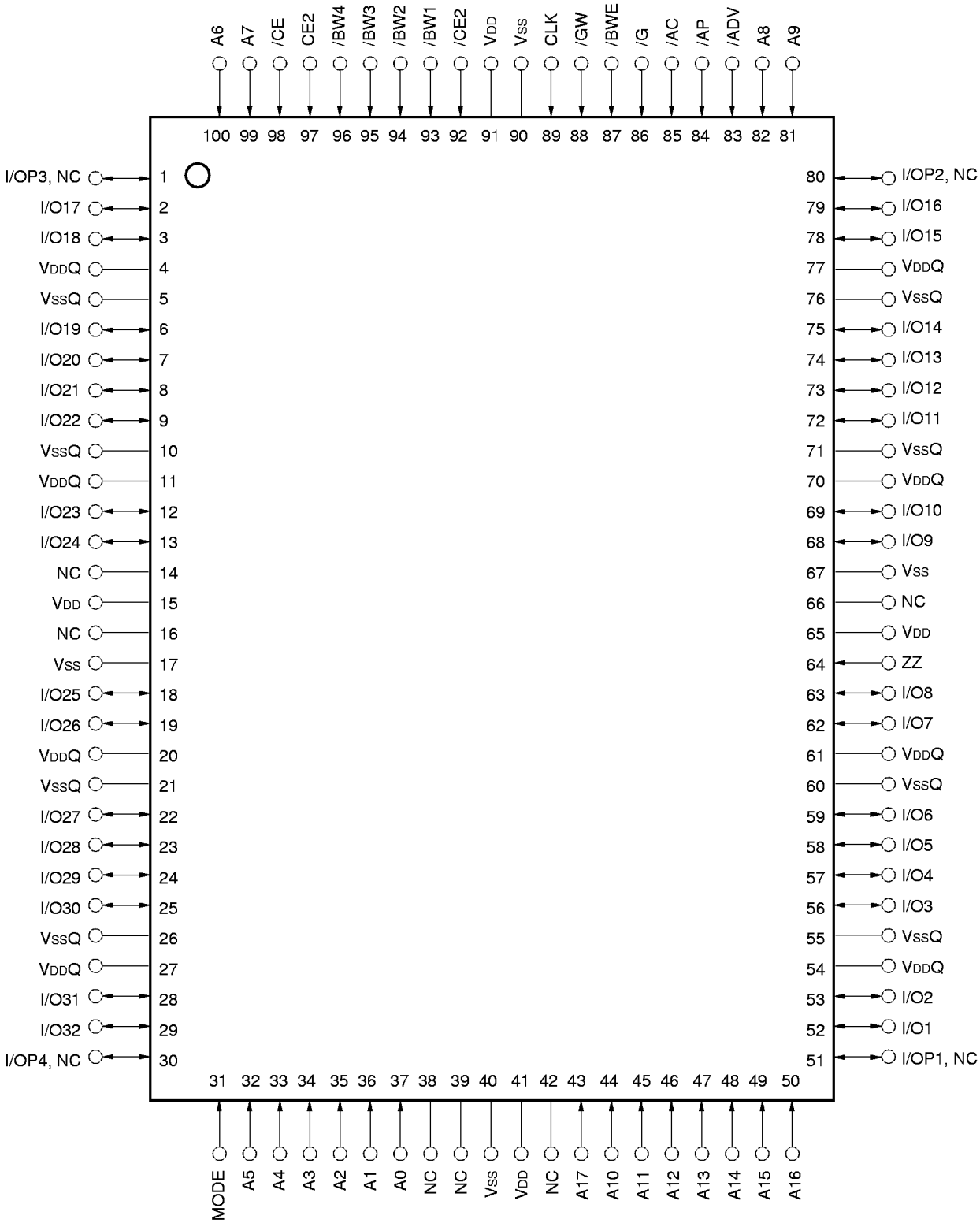
Symbol	Pin No.	Description
A0 - A18	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 43, 80	Synchronous Address Input
I/O1 - I/O16	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, NC Note	74	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
I/OP2, NC Note	24	
/ADV	83	Synchronous Burst Address Advance Input
/AP	84	Synchronous Address Status Processor Input
/AC	85	Synchronous Address Status Controller Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/BW1, /BW2, /BWE	93, 94, 87	Synchronous Byte Write Enable Input
/GW	88	Synchronous Global Write Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
MODE	31	Asynchronous Burst Sequence Select Input Do not change state during normal operation
ZZ	64	Asynchronous Power Down State Input
V_{DD}	15, 41, 65, 91	Power Supply
V_{SS}	17, 40, 67, 90	Ground
$V_{DD}Q$	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
$V_{SS}Q$	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	No Connection

Note NC (No Connection) is used in the μPD4382161GF.

I/OP1 - I/OP2 is used in the μPD4382181GF.

100-pin plastic LQFP (14 x 20 mm)

[μPD4382321GF, μPD4382361GF]



[μPD4382321GF, μPD4382361GF]

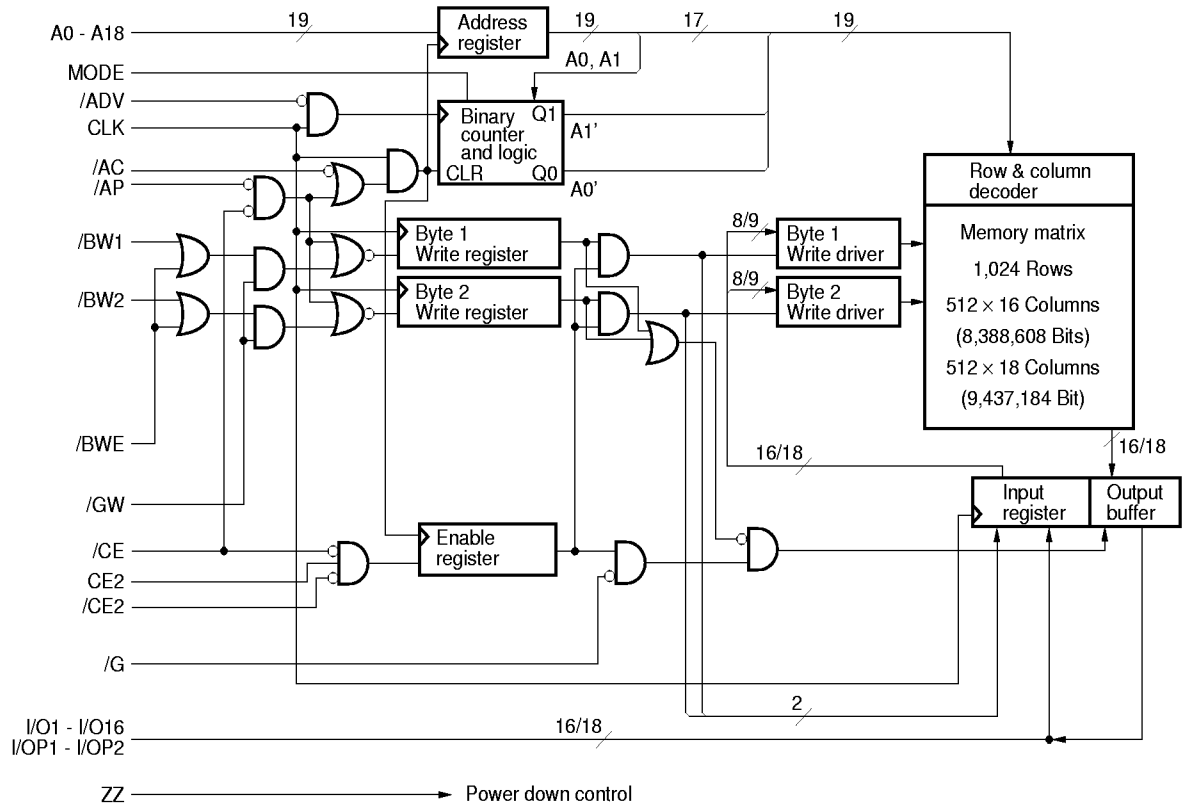
Symbol	Pin No.	Description
A0 - A17	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	Synchronous Address Input
I/O1 - I/O32	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, NC Note	51	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
I/OP2, NC Note	80	
I/OP3, NC Note	1	
I/OP4, NC Note	30	
/ADV	83	Synchronous Burst Address Advance Input
/AP	84	Synchronous Address Status Processor Input
/AC	85	Synchronous Address Status Controller Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/BW1 - /BW4, /BWE	93, 94, 95, 96, 87	Synchronous Byte Write Enable Input
/GW	88	Synchronous Global Write Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
MODE	31	Asynchronous Burst Sequence Select Input Do not change state during normal operation
ZZ	64	Asynchronous Power Down State Input
V_{DD}	15, 41, 65, 91	Power Supply
V_{SS}	17, 40, 67, 90	Ground
$V_{DD}Q$	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
$V_{SS}Q$	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	14, 16, 38, 39, 42, 43, 49, 50, 66	No Connection

Note NC (No Connection) is used in the μPD4382321GF.

I/OP1 - I/OP4 is used in the μPD4382361GF.

Block Diagram

[μPD4382161, μPD4382181]



Burst Sequence

[μPD4382161, μPD4382181]

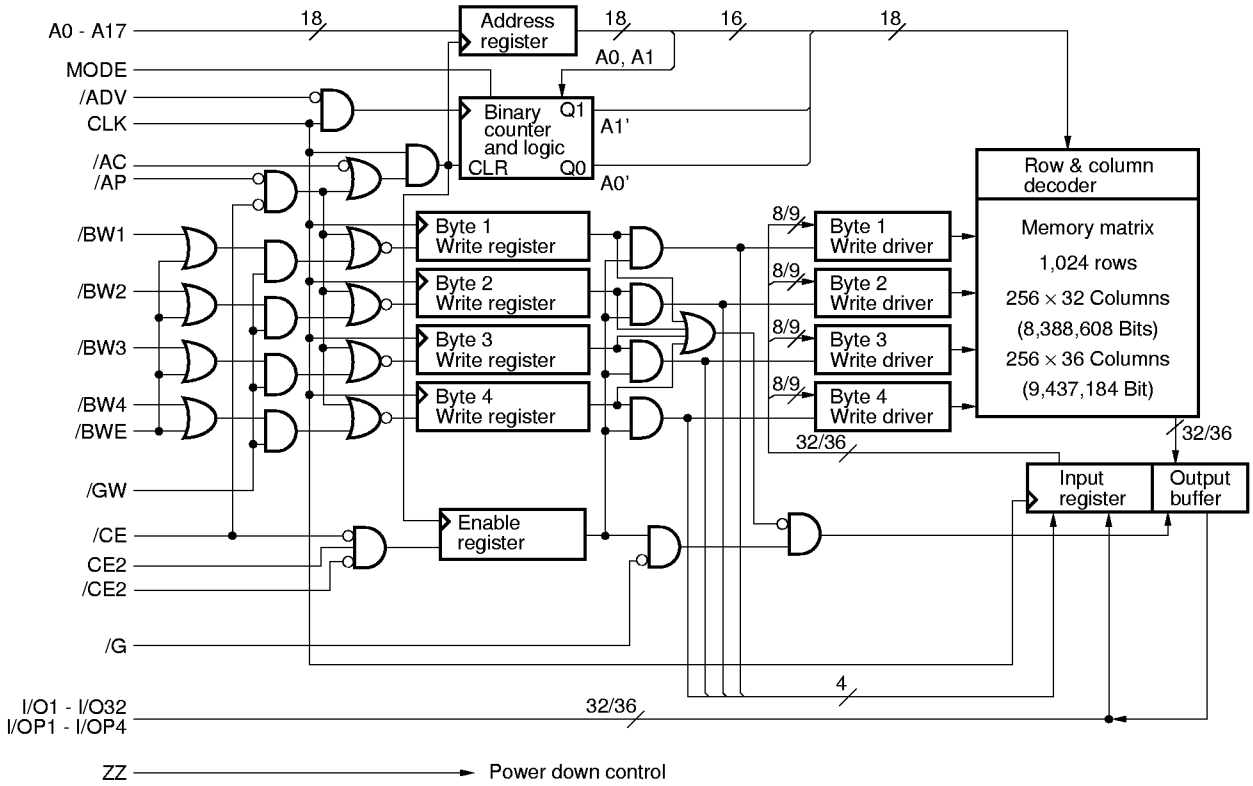
Interleaved Burst Sequence Table (MODE = Open or V_{DD})

External Address	A18 - A2, A1, A0
1st Burst Address	A18 - A2, A1, /A0
2nd Burst Address	A18 - A2, /A1, A0
3rd Burst Address	A18 - A2, /A1, /A0

Linear Burst Sequence Table (MODE = V_{SS})

External Address	A18 - A2, 0, 0	A18 - A2, 0, 1	A18 - A2, 1, 0	A18 - A2, 1, 1
1st Burst Address	A18 - A2, 0, 1	A18 - A2, 1, 0	A18 - A2, 1, 1	A18 - A2, 0, 0
2nd Burst Address	A18 - A2, 1, 0	A18 - A2, 1, 1	A18 - A2, 0, 0	A18 - A2, 0, 1
3rd Burst Address	A18 - A2, 1, 1	A18 - A2, 0, 0	A18 - A2, 0, 1	A18 - A2, 1, 0

[μPD4382321, μPD4382361]



Burst Sequence

[μPD4382321, μPD4382361]

Interleaved Burst Sequence Table (MODE = Open or V_{DD})

External Address	A17 - A2, A1, A0
1st Burst Address	A17 - A2, A1, /A0
2nd Burst Address	A17 - A2, /A1, A0
3rd Burst Address	A17 - A2, /A1, /A0

Linear Burst Sequence Table (MODE = V_{SS})

External Address	A17 - A2, 0, 0	A17 - A2, 0, 1	A17 - A2, 1, 0	A17 - A2, 1, 1
1st Burst Address	A17 - A2, 0, 1	A17 - A2, 1, 0	A17 - A2, 1, 1	A17 - A2, 0, 0
2nd Burst Address	A17 - A2, 1, 0	A17 - A2, 1, 1	A17 - A2, 0, 0	A17 - A2, 0, 1
3rd Burst Address	A17 - A2, 1, 1	A17 - A2, 0, 0	A17 - A2, 0, 1	A17 - A2, 1, 0

Asynchronous Truth Table

Operation	/G	I/O
Read Cycle	L	Dout
Read Cycle	H	Hi-Z
Write Cycle	X	Hi-Z, Din
Deselected	X	Hi-Z

Remark X means "don't care."

Synchronous Truth Table

Operation	/CE	CE2	/CE2	/AP	/AC	/ADV	/WRITE	CLK	Address
Deselected Note	H	X	X	X	L	X	X	L → H	None
Deselected Note	L	L	X	L	X	X	X	L → H	None
Deselected Note	L	X	H	L	X	X	X	L → H	None
Deselected Note	L	L	X	H	L	X	X	L → H	None
Deselected Note	L	X	H	H	L	X	X	L → H	None
Read Cycle / Begin Burst	L	H	L	L	X	X	X	L → H	External
Read Cycle / Begin Burst	L	H	L	H	L	X	H	L → H	External
Read Cycle / Continue Burst	X	X	X	H	H	L	H	L → H	Next
Read Cycle / Continue Burst	H	X	X	X	H	L	H	L → H	Next
Read Cycle / Suspend Burst	X	X	X	H	H	H	H	L → H	Current
Read Cycle / Suspend Burst	H	X	X	X	H	H	H	L → H	Current
Write Cycle / Begin Burst	L	H	L	H	L	X	L	L → H	External
Write Cycle / Continue Burst	X	X	X	H	H	L	L	L → H	Next
Write Cycle / Continue Burst	H	X	X	X	H	L	L	L → H	Next
Write Cycle / Suspend Burst	X	X	X	H	H	H	L	L → H	Current
Write Cycle / Suspend Burst	H	X	X	X	H	H	L	L → H	Current

Note Deselect status is held until new "Begin Burst" entry.

Remarks 1. X means "don't care."

2. /WRITE=L means any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) and /BWE are LOW or /GW is LOW.

/WRITE=H means the following two cases.

(1) /BWE and /GW are HIGH.

(2) /BW1, /BW2, /BW3, /BW4 and /GW are HIGH, and /BWE is LOW.

Partial Truth Table for Write Enables

[μPD4382161, μPD4382181]

Operation	/GW	/BWE	/BW1	/BW2
Read Cycle	H	H	X	X
Read Cycle	H	L	H	H
Write Cycle / Byte 1 Only	H	L	L	H
Write Cycle / All Bytes	H	L	L	L
Write Cycle / All Bytes	L	X	X	X

Remark X means "don't care."

[μPD4382321, μPD4382361]

Operation	/GW	/BWE	/BW1	/BW2	/BW3	/BW4
Read Cycle	H	H	X	X	X	X
Read Cycle	H	L	H	H	H	H
Write Cycle / Byte 1 Only	H	L	L	H	H	H
Write Cycle / All Bytes	H	L	L	L	L	L
Write Cycle / All Bytes	L	X	X	X	X	X

Remark X means "don't care."

ZZ (Sleep) Truth Table

ZZ	Chip Status
≤ 0.2 V	Active
Open	Active
≥ V_{DD} – 0.2 V	Sleep

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		–0.5		+4.0	V	
Output supply voltage	V_{DDQ}		–0.5		V_{DD}	V	
Input voltage	V_{IN}		–0.5		V_{DD} + 0.5	V	1, 2
Input / Output voltage	$V_{I/O}$		–0.5		V_{DDQ} + 0.5	V	1, 2
Operating ambient temperature	T_A		0		70	°C	
Storage temperature	T_{stg}		–55		+125	°C	

Notes 1. –2.0 V (MIN.)(Pulse width : 2 ns)

2. V_{DDQ} + 2.3 V (MAX.)(Pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.135	3.3	3.465	V
2.5 V LVTTL interface						
Output supply voltage	V_{DDQ}		2.375	2.5	2.9	V
High level input voltage	V_{IH}		1.7		V_{DDQ} + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		+0.7	V
3.3 V LVTTL interface						
Output supply voltage	V_{DDQ}		3.135	3.3	3.465	V
High level input voltage	V_{IH}		2.0		V_{DDQ} + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		+0.8	V

Note –0.8 V (MIN.)(Pulse width : 2 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			4	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			7	pF
Clock input capacitance	C_{clk}	V_{clk} = 0 V			4	pF

Remark These parameters are periodically sampled and not 100% tested.

DC Characteristics (T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.165 V)

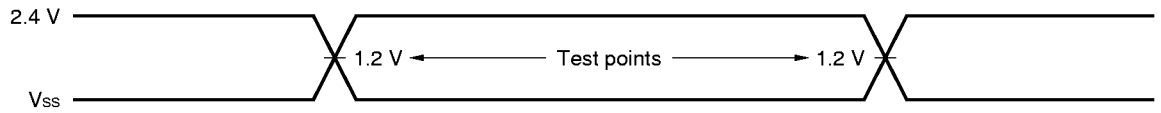
	Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit	Note
	Input leakage current	I_{LI}	V_{IN} (except ZZ, MODE) = 0 V to V_{DD}		–2		+2	μA	
	I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{DDQ}, Outputs are disabled.		–2		+2	μA	
★	Operating supply current	I_{DD}	Device selected, Cycle = MAX.	μPD4382161-A85			260	mA	
				μPD4382181-A85					
			$V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA	μPD4382161-A90			250		
				μPD4382181-A90					
				μPD4382321-A85			350		
				μPD4382361-A85					
				μPD4382321-A90			330		
				μPD4382361-A90					
★		I_{DD1}	Suspend cycle, Cycle = MAX. /AC, /AP, /ADV, /GW, /BWEs ≥ V_{IH} $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $I_{I/O}$ = 0 mA				120		
	Standby supply current	I_{SB}	Device deselected, Cycle = 0 MHz $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, All inputs are static.				30	mA	
		I_{SB1}	Device deselected, Cycle = 0 MHz $V_{IN} \leq$ 0.2 V or $V_{IN} \geq V_{DD}$ – 0.2 V $V_{I/O} \leq$ 0.2 V, All inputs are static.				10		
★		I_{SB2}	Device deselected, Cycle = MAX. $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$				150		
	Power down supply current	I_{SBZZ}	ZZ ≥ V_{DD} – 0.2 V, $V_{I/O} \leq V_{DDQ}$ + 0.2 V				10	mA	
	2.5 V LVTTL interface								
★	High level output voltage	V_{OH}	I_{OH} = –2.0 mA		1.7			V	
			I_{OH} = –1.0 mA		2.1				
★	Low level output voltage	V_{OL}	I_{OL} = +2.0 mA				0.7	V	
			I_{OL} = +1.0 mA				0.4		
	3.3 V LVTTL interface								
	High level output voltage	V_{OH}	I_{OH} = –4.0 mA		2.4			V	
	Low level output voltage	V_{OL}	I_{OL} = +8.0 mA				0.4	V	

AC Characteristics (T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.165 V)

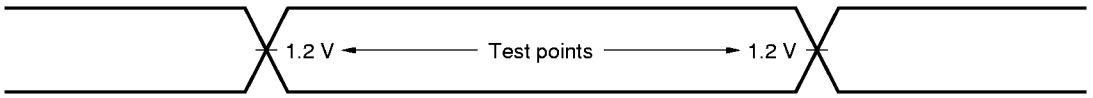
AC Test Conditions

2.5 V LVTTL Interface

Input waveform (Rise / Fall time ≤ 2.4 ns)

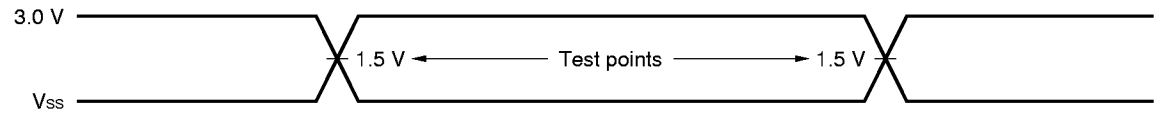


Output waveform

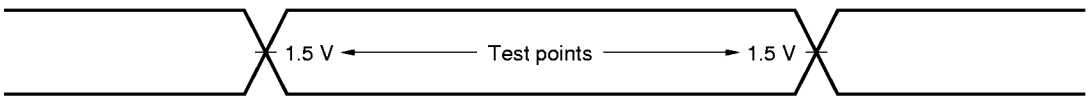


3.3 V LVTTL Interface

Input waveform (Rise / Fall time ≤ 3.0 ns)



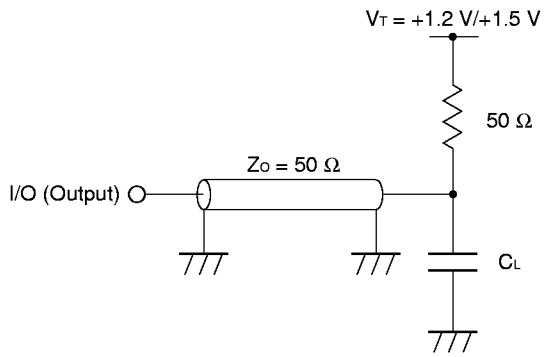
Output waveform



★ **Output load condition**

C_L : 30 pF
5 pF (TKHQX1, TKHQX2, TGLQX, TGHQZ, TKHQZ)

Figure1 External load at test



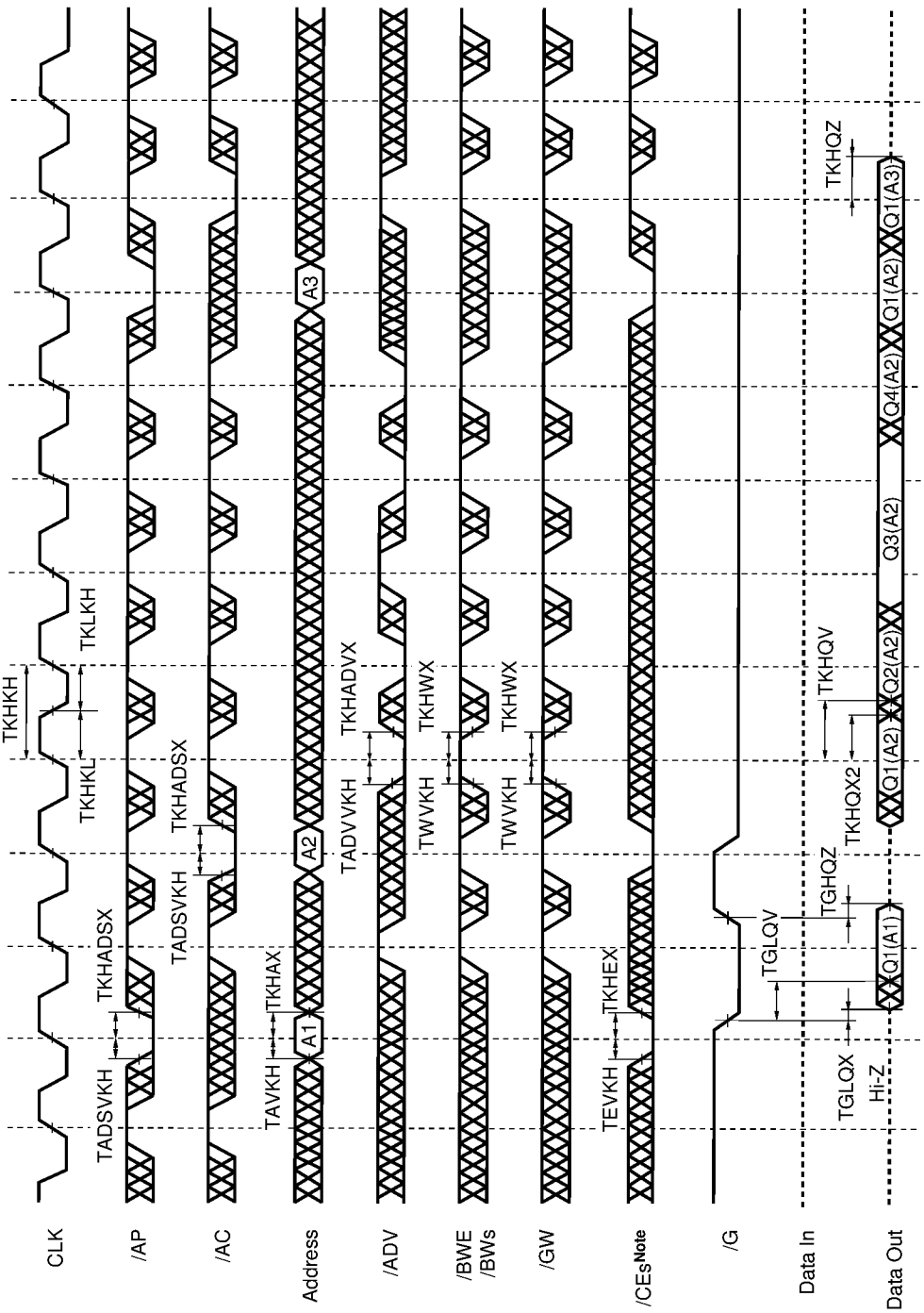
Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle

Parameter		Symbol		-A85 (100 MHz)		-A90 (90 MHz)		Unit	Note
		Standard	Alias	MIN.	MAX.	MIN.	MAX.		
Cycle time		TKHKH	TCYC	10	–	11	–	ns	
Clock access time		TKHQV	TCD	–	8.5	–	9	ns	
Output enable access time		TGLQV	TOE	–	3.5	–	3.5	ns	
Clock high to output active		TKHQX1	TDC1	2	–	2	–	ns	
Clock high to output change		TKHQX2	TDC2	3	–	3	–	ns	
Output enable to output active		TGLQX	TOLZ	0	–	0	–	ns	
Output disable to output high-Z		TGHQZ	TOHZ	0	3.5	0	3.5	ns	
Clock high to output high-Z		TKHQZ	TCZ	2	4	2	4	ns	
Clock high pulse width		TKHKL	TCH	2.5	–	2.5	–	ns	
Clock low pulse width		TKLKH	TCL	2.5	–	2.5	–	ns	
Setup times	Address	TAVKH	TAS	2	–	2	–	ns	
	Address status	TADSVKH	TSS						
	Data in	TDVKH	TDS						
	Write enable	TWVKH	TWS						
	Address advance	TADVVKH	–						
	Chip enable	TEVKH	–						
Hold times	Address	TKHAX	TAH	0.5	–	0.5	–	ns	
	Address status	TKHADSX	TSH						
	Data in	TKHDX	TDH						
	Write enable	TKHWX	TWH						
	Address advance	TKHADVX	–						
	Chip enable	TKHEX	–						
Power down entry setup		TZZES	TZZES	5	–	5	–	ns	1
Power down entry hold		TZZEH	TZZEH	1	–	1	–	ns	1
Power down recovery setup		TZZRS	TZZRS	6	–	6	–	ns	1
Power down recovery hold		TZZRH	TZZRH	0	–	0	–	ns	1

Note 1. Although ZZ signal input is asynchronous, the signal must meet specified setup and hold times in order to be recognized.

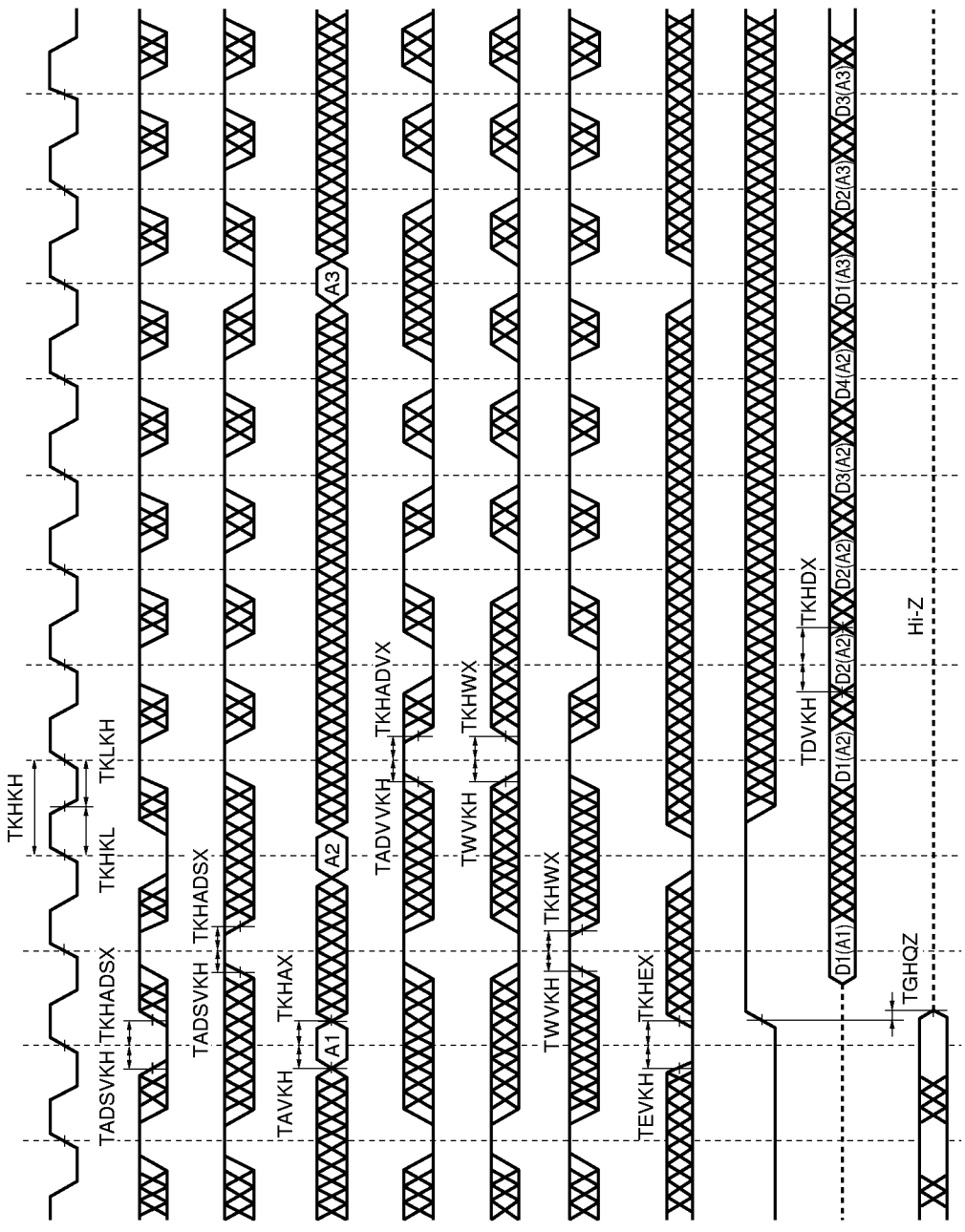
READ CYCLE



Note /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

Remark Qn(A2) refers to output from address A2. Q1-Q4 refer to outputs according to burst sequence.

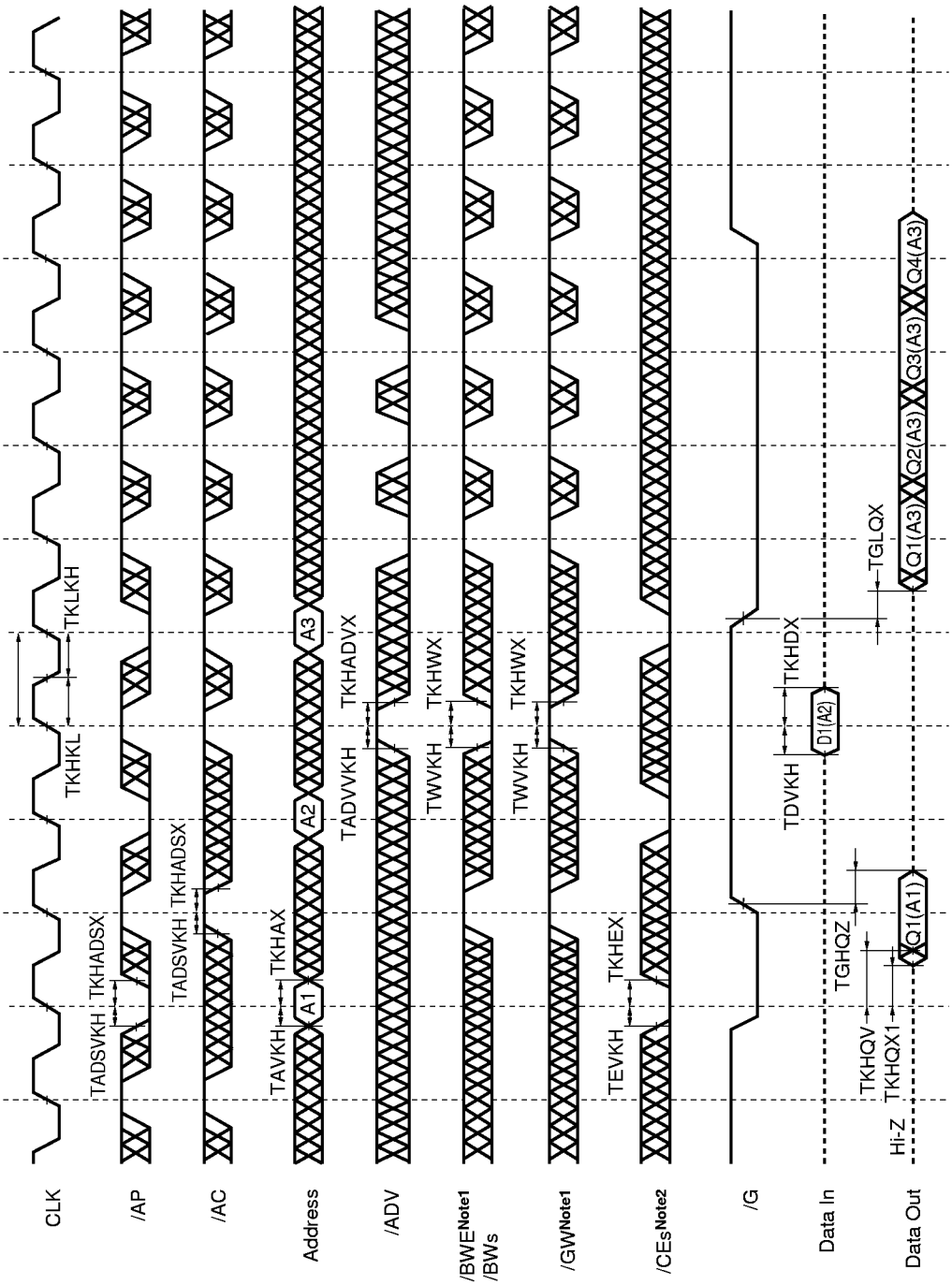
WRITE CYCLE



Notes 1. All bytes WRITE can be initiated by /GW LOW or /GW HIGH and /BWE, /BW1-/BW4 LOW.

2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

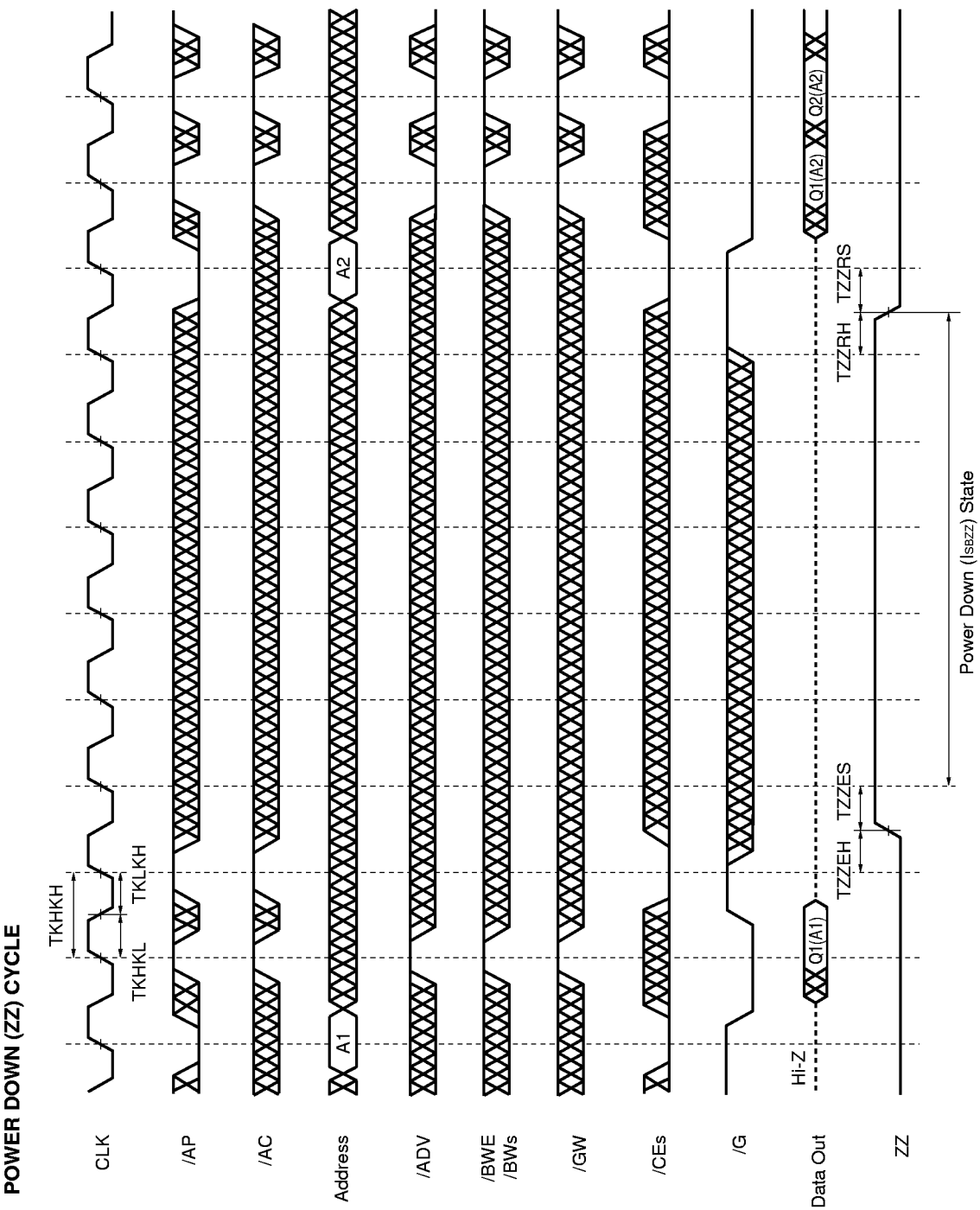
READ / WRITE CYCLE



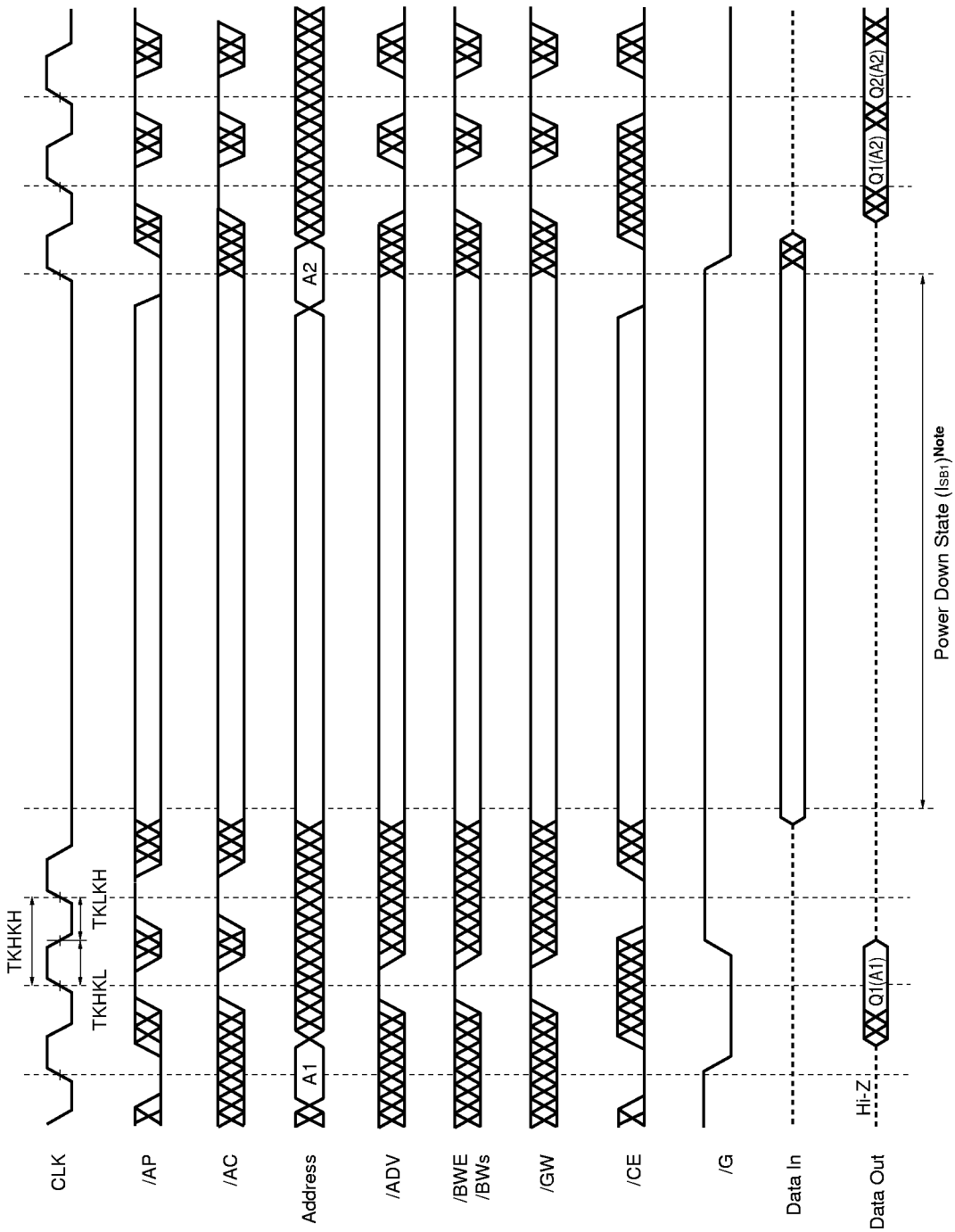
Notes 1. All bytes WRITE can be initiated by /GW LOW or /GW HIGH and /BWE, /BW1-/BW4 LOW.

2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

POWER DOWN (ZZ) CYCLE



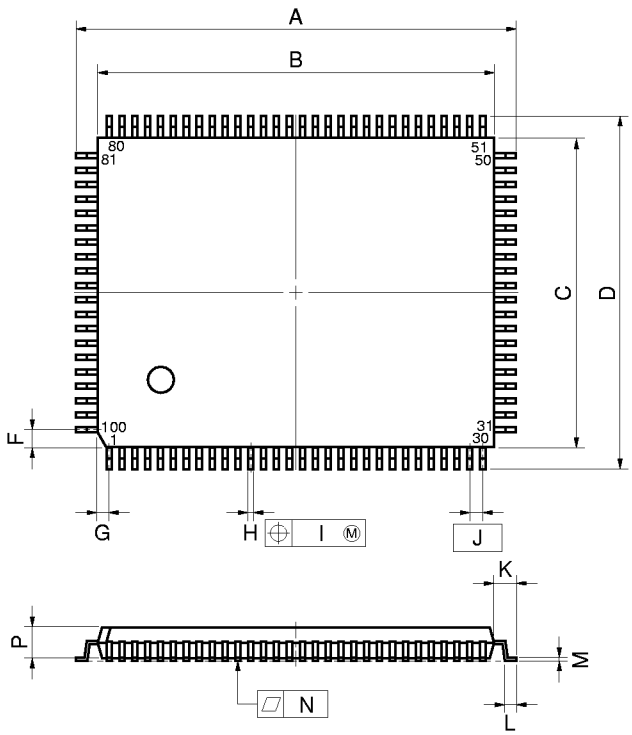
STOP CLOCK CYCLE

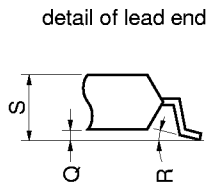


Note $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{DD} - 0.2$ V, $V_{I/O} \leq 0.2$ V

Package Drawing

100 PIN PLASTIC LQFP (14×20)





NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0 ± 0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	0.825	0.032
G	0.575	0.023
H	$0.32^{+0.08}_{-0.07}$	0.013±0.003
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.06}_{-0.05}$	0.007±0.002
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.	0.067 MAX.

S100GF-65-8ET

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD4382161, 4382181, 4382321 and 4382361.

Type of Surface Mount Devices

μPD4382161GF : 100-pin plastic LQFP (14 x 20 mm)

μPD4382181GF : 100-pin plastic LQFP (14 x 20 mm)

μPD4382321GF : 100-pin plastic LQFP (14 x 20 mm)

μPD4382361GF : 100-pin plastic LQFP (14 x 20 mm)