Military Standard Products

UT7156 Radiation-Hardened 32K x 8 SRAM

Advanced Data Sheet

March 1997

FEATURES

- 40ns, 55ns, and 70ns maximum address access time
- Asynchronous operation for compatibility with industry-standard 32K x 8 SRAM
- CMOS compatible inputs/outputs
- Three-state bidirectional data bus
- Low operating and standby current
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 1.0E6 rads(Si)
  - Error Rate: 1.0E-10 errors/bit-day
  - Latchup immune
- QML Q and V compliant part
- Packaging options:
  - 36-pin 50-mil center flatpack (0.7 x 1.0)
  - 28-pin 100-mil center DIP (0.600 x 1.4)
- 5-volt operation
- Standard Microcircuit Drawing available 5962-92153

INTRODUCTION

The UT7156 SRAM is a high performance, asynchronous, radiation-hardened, 32K x 8 random access memory conforming to industry-standard fit, form, and function. The UT7156 SRAM features fully static operation requiring no external clocks or timing strobes. Implemented using an advanced radiation-hardened process and a device enable/ disable function the UT7156 is a high performance, power-saving SRAM. The combination of radiation-hardness, fast access time, and low power consumption make UT7156 ideal for high-speed systems designed for operation in radiation environments.

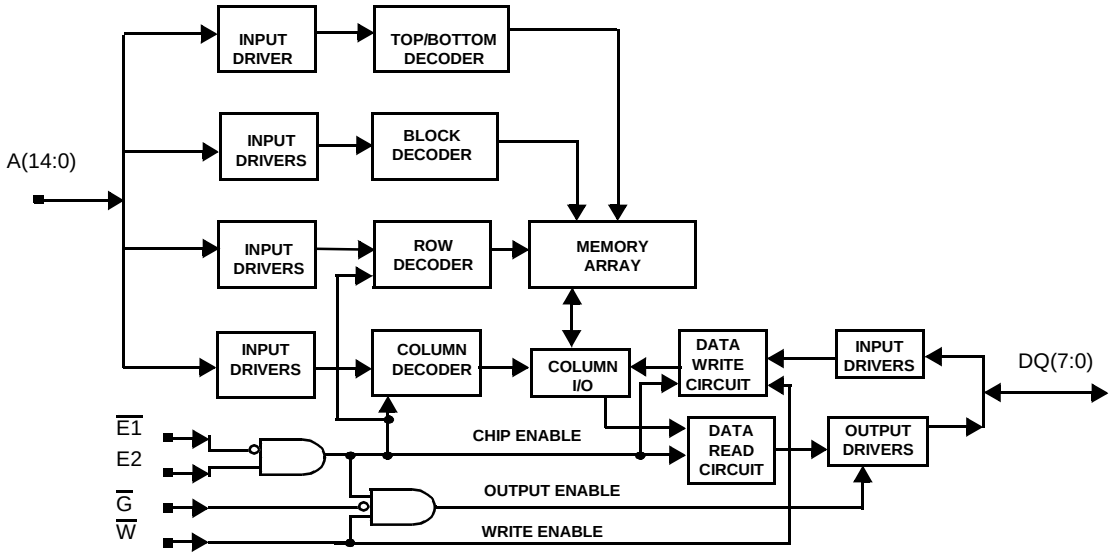


Figure 1. SRAM Functional Block Diagram

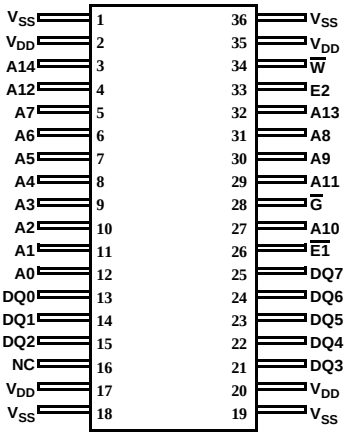


Figure 2a. SRAM Pinout (36)

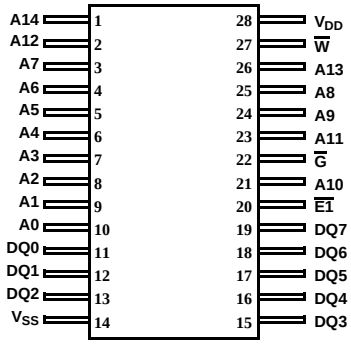


Figure 2b. SRAM Pinout (28)

PIN NAMES

A(14:0)	Address	$\overline{W}$	Write
DQ(7:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{E1}$	Enable 1	V_{DD}	Power
E2[1]	Enable 2	V_{SS}	Ground

1. 36-lead flatpack only.

DEVICE OPERATION

The UT7156 has four control inputs called Enable 1 ($\overline{E1}$), Enable 2 (E2), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 15 address inputs, A(14:0); and eight bidirectional data lines, DQ(7:0). $\overline{E1}$ and E2 are device enable inputs that control device selection, active, and standby modes. Asserting both $\overline{E1}$ and E2 enables the device, causes I_{DD} to rise to its active value, and decodes the 15 address inputs to select one of 32,768 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}$	$\overline{E1}$	E2[3]	I/O Mode	Mode
X[1]	X	X	0	3-state	Standby
X	X	1	X	3-state	Standby
X	0	0	1	Data in	Write
1	1	0	1	3-state	Read[2]
0	1	0	1	Data out	Read

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.
3. Tied active (i.e., logic 1) in the 28-pin DIP package.

READ CYCLE

A combination of $\overline{W}$ greater than V_{IH} (min), $\overline{E1}$ less than V_{IL} (max), and E2 greater than V_{IH} (min) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

Read Cycle 1, the Address Access read in figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

Read Cycle 2, the Chip Enable-controlled Access in figure 3b, is initiated by the latter of $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(14:0) is accessed and appears at the data outputs DQ(7:0).

Read Cycle 3, the Output Enable-controlled Access in figure 3c, is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}$ less than V_{IL}(max), $\overline{E1}$ less than V_{IL}(max), and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access shown in figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by the latter of $\overline{E1}$ or E2. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access shown in figure 4b, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by the latter of $\overline{E1}$ or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

RADIATION HARDNESS

The UT7156 SRAM incorporates special design and layout features which allow operation in high-level radiation environments.

Table 2. Radiation Hardness Design Specifications[1]

Total Dose	1.0E6	rads(Si)
Error Rate[2]	1.0E-10	Errors/Bit-Day

Notes:
1. The SRAM will not latchup during radiation exposure under recommended operating conditions.
2. 10% worst case particle environment, Geosynchronous orbit, 0.025 mils of Aluminum.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.5 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.5 to (V_{DD} + 0.3)V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	2.0W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	4.5 to 5.5V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

(V_{DD} = 5.0V±10%) (-55°C to +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage	(CMOS)	3.5		V
V_{IL}	Low-level input voltage	(CMOS)		1.5	V
V_{OL}	Low-level output voltage	I_{OL} = 200µA, V_{DD} = 4.5V (CMOS)		0.05	V
V_{OH}	High-level output voltage	I_{OH} = -200µA, V_{DD} = 4.5V (CMOS)	V_{DD}-0.05		V
V_{OH}	High-level output voltage	I_{OH} = -4mA, V_{DD} = 4.5V (CMOS)	4.2		V
C_{IN}[1]	Input capacitance	f = 1MHz @ 0V		4	pF
C_{IO}[1]	Bidirectional I/O capacitance	f = 1MHz @ 0V		7	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}	-5	5	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V $\overline{G}$ = 5.5V	-10	10	µA
I_{OS}[2, 3]	Short-circuit output current	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	-90	+90	mA mA
I_{DD}(OP)	Supply current operating @1MHz	CMOS inputs (I_{OUT} = 0) V_{DD} = 5.5V		50	mA
I_{DD1}(OP)	Supply current operating @ 25MHz	CMOS inputs (I_{OUT} = 0) V_{DD} = 5.5V		120	mA
I_{DD3}(SB)[4]	Supply current standby @ 0Hz	CMOS inputs (I_{OUT} = 0) $\overline{E1}$ = V_{DD} - 0.5, V_{DD} = 5.5V		1.2	mA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 5.0E5 rads(Si).

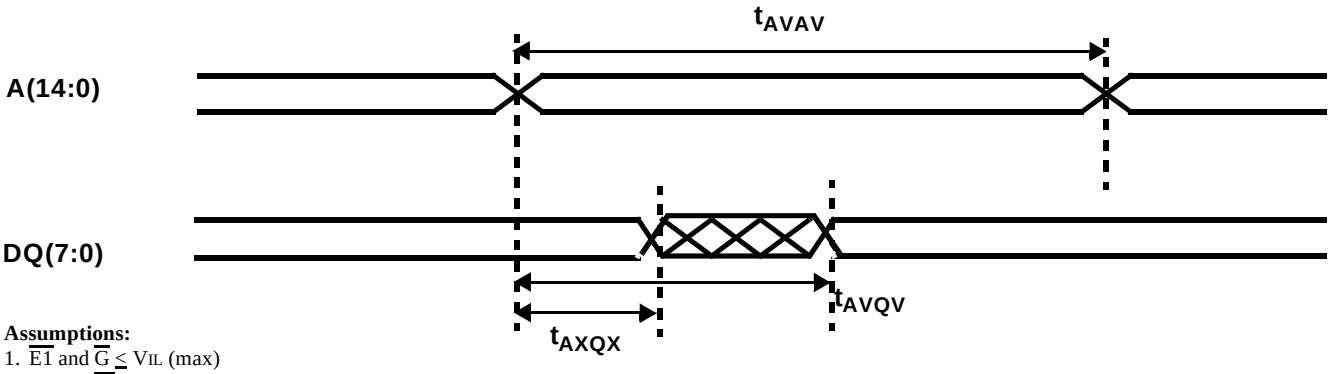
1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. V_{IH} = 5.5V, V_{IL} = 0V.

AC CHARACTERISTICS READ CYCLE (Post-Radiation)*

(V_{DD} = 5.0V±10%) (-55°C to +125°C)

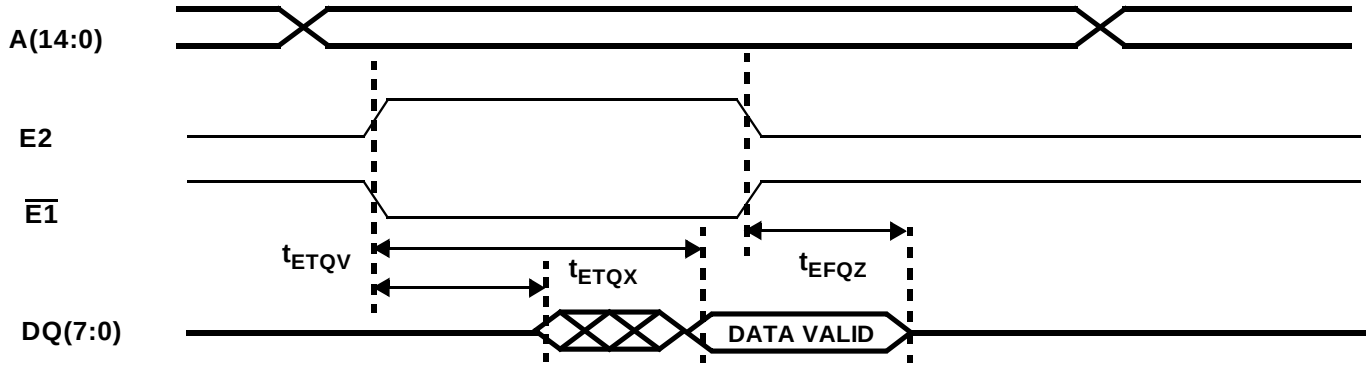
SYMBOL	PARAMETER	7156-40		7156-55		7156-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}[1]	Read cycle time	40		55		70		ns
t_{AVQV}	Read access time		40		55		70	ns
t_{AXQX}[2]	Output hold time	5		5		5		ns
t_{GLQX}[2]	$\overline{G}$-controlled output enable time	3		0		0		ns
t_{GLQV}	$\overline{G}$-controlled output enable time (Read Cycle 3)		15		15		15	ns
t_{GHQZ}[2]	$\overline{G}$-controlled output three-state time		15		15		15	ns
t_{ETQX}[2,3]	E-controlled output enable time	3		0		0		ns
t_{ETQV}[3]	E-controlled access time		40		55		70	ns
t_{EFQZ}[1,4]	E-controlled output three-state time[2]		15		20		20	ns

Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Functional test.
2. Three-state is defined as a 500mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the rising edge of E2 or the falling edge of $\overline{E1}$, whichever comes last. SEU immunity does not affect the read parameters.
4. The EF (enable false) notation refers to the falling edge of E2 or the rising edge of $\overline{E1}$, whichever comes first. SEU immunity does not affect the read parameters.



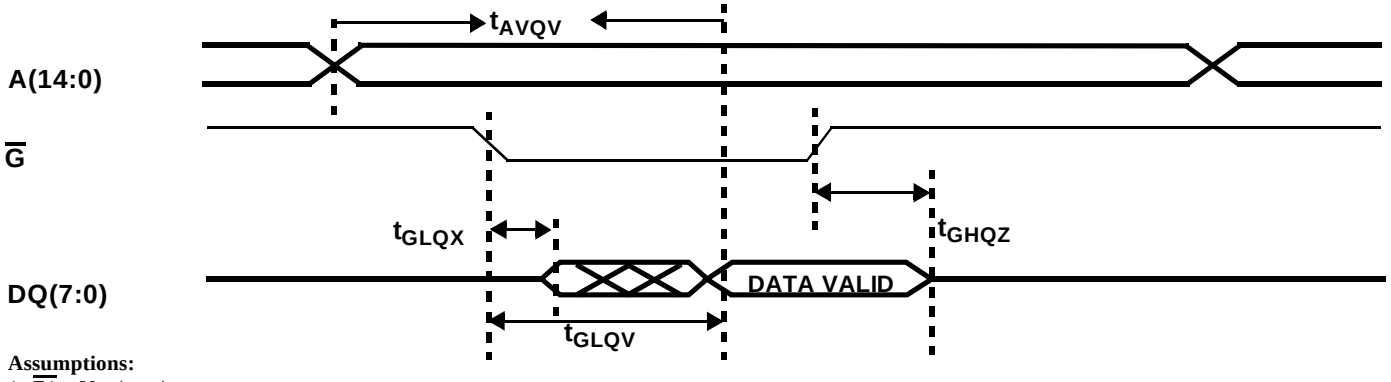
Assumptions:
1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max)
2. E2 and $\overline{W} \geq V_{IH}$ (min)

Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:
1. $\overline{E1} \leq V_{IL}$ (max)
2. E2 and $\overline{W} \geq V_{IH}$ (min)

Figure 3c. SRAM Read Cycle 3: Output Enable Access

AC CHARACTERISTICS WRITE CYCLE (Post-Radiation)*

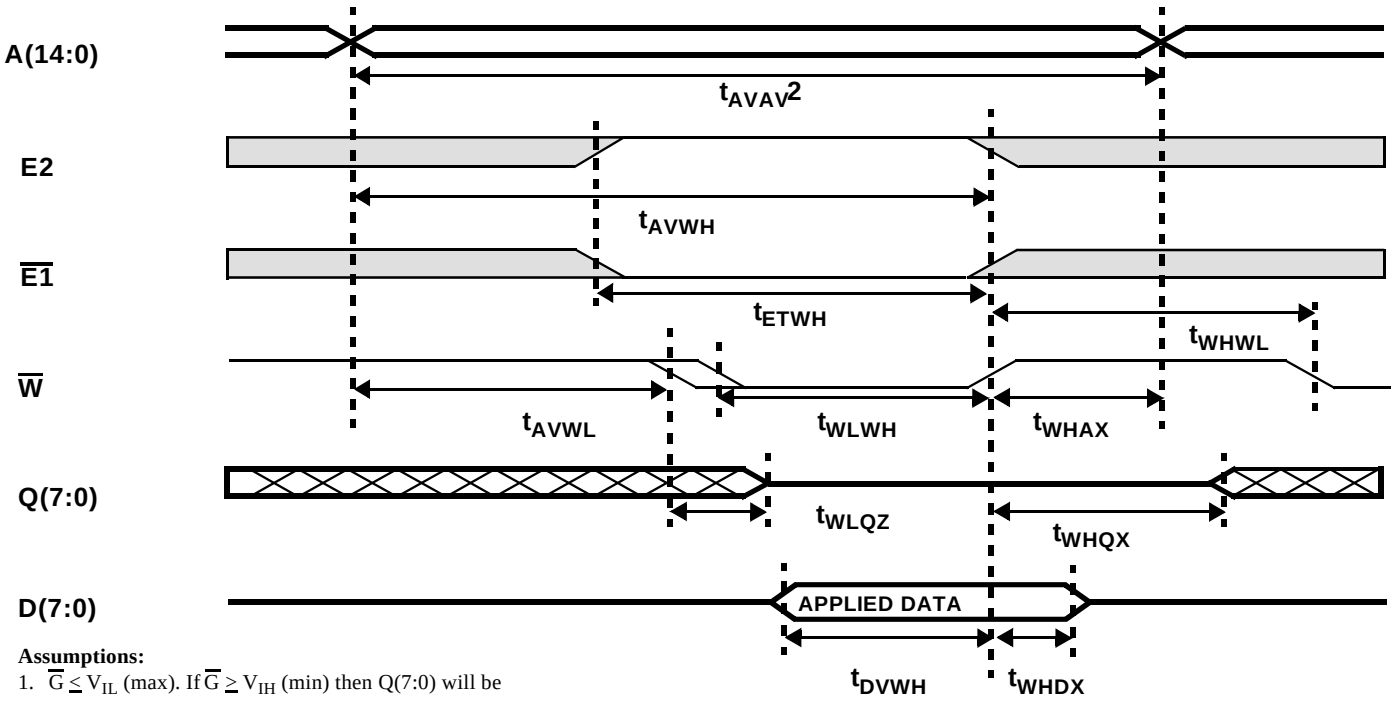
(V_{DD} = 5.0V ±10%) (-55°C to +125°C)

SYMBOL	PARAMETER	7156-40		7156-55		7156-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}[1]	Write cycle time	40		55		70		ns
t_{ETWH}	Device enable to end of write	35		50		65		ns
t_{AVET}	Address setup time for write ($\overline{E1}$ or E2 - controlled)	0		0		0		ns
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		0		0		ns
t_{WLWH}	Write pulse width	35		40		50		ns
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	0		0		0		ns
t_{EFAX}	Address hold time for device enable ($\overline{E1}$ or E2 - controlled)	0		0		0		ns
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		15		20		25	ns
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	1		0		0		ns
t_{ETEF}	Device enable pulse width ($\overline{E1}$ or E2 - controlled)	35		50		65		ns
t_{DVWH}	Data setup time	30		40		50		ns
t_{WHDX}	Data hold time	3		5		0		ns
t_{WLEF}	Device enable controlled write pulse width	35		40		65		ns
t_{DVEF}	Data setup time	35		40		50		ns
t_{EFDX}	Data hold time	0		0		0		ns
t_{AVWH}	Address valid to end of write	35		40		50		ns
t_{WHWL}[1]	Write disable time	5		5		5		ns

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.

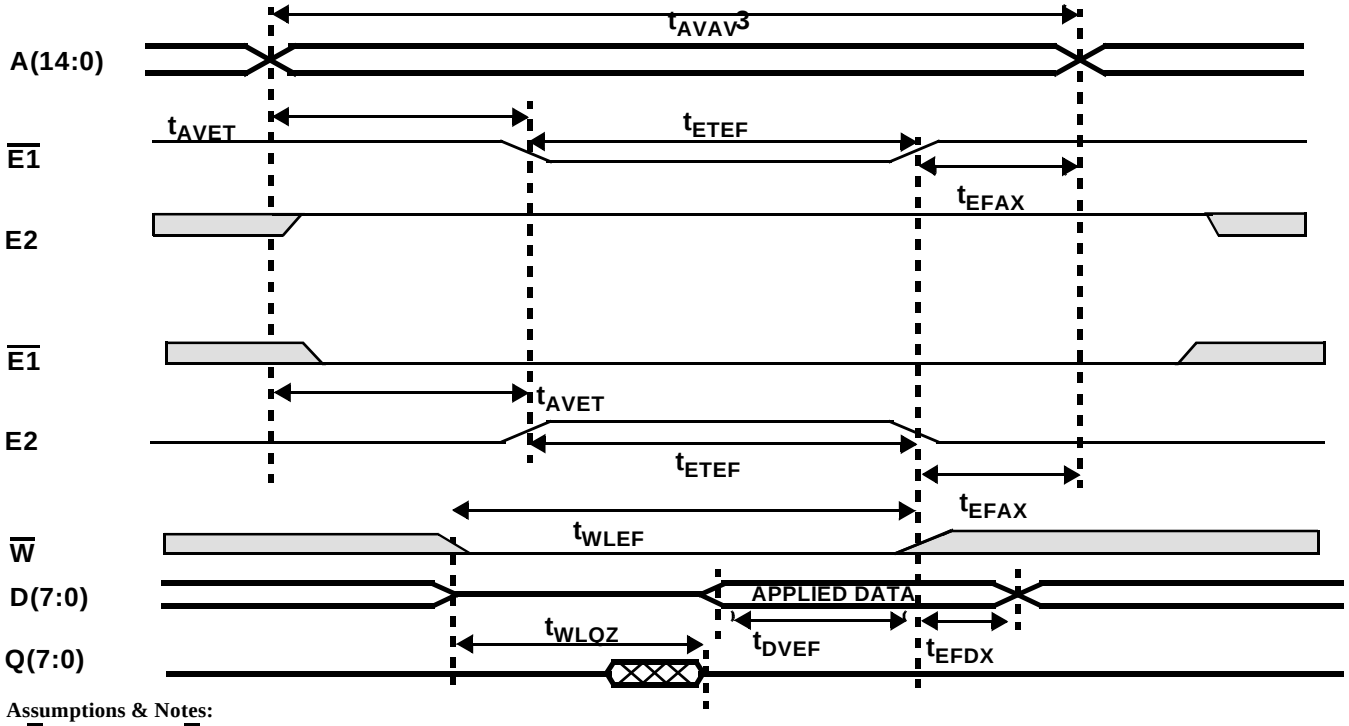
1. Functional test performed with outputs disabled ($\overline{G}$ high).
2. Three-state is defined as 500mV change from steady-state output voltage.



Assumptions:

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(7:0) will be in three-state for the entire cycle.
2. $\overline{G}$ high for t_{AVAV} cycle.

Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access



Assumptions & Notes:

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(7:0) will be in three-state for the entire cycle.
2. Either $\overline{E1}$/E2 scenario above can occur.
3. $\overline{G}$ high for t_{AVAV} cycle.

Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access

DATA RETENTION CHARACTERISTICS (Pre-Radiation)
(T_C = 25°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM V_{DD} @ 2.5V	UNIT
V_{DR}	V_{DD} for data retention	2.5	--	V
I_{DDR} [1]	Data retention current	--	.4	mA
t_{EFR} [1,2]	Chip deselect to data retention time	0		ns
t_R [1,2]	Operation recovery time	t_{AVAV}		ns

Notes:
1. $\overline{E1}$ = V_{DR} or E2 = V_{SS}, all other inputs = V_{DR} or V_{SS}.
2. Guaranteed but not tested.

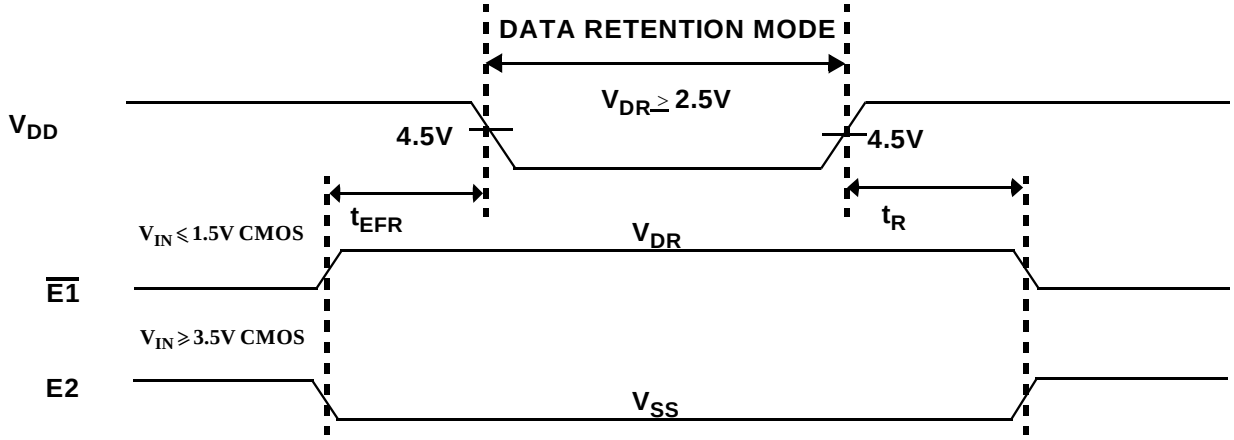
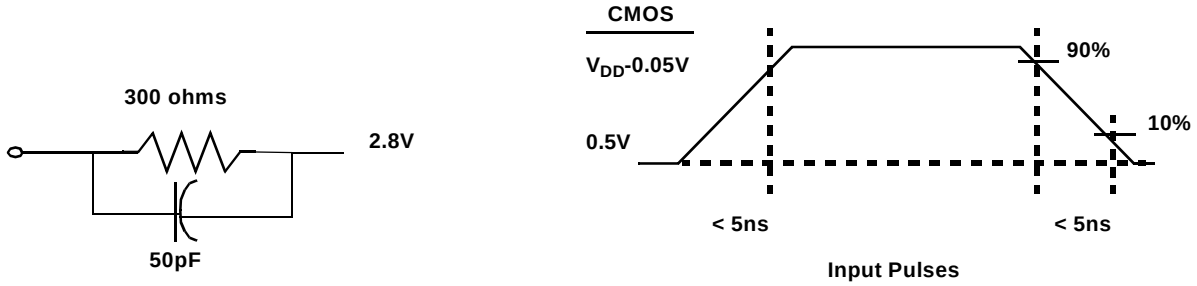


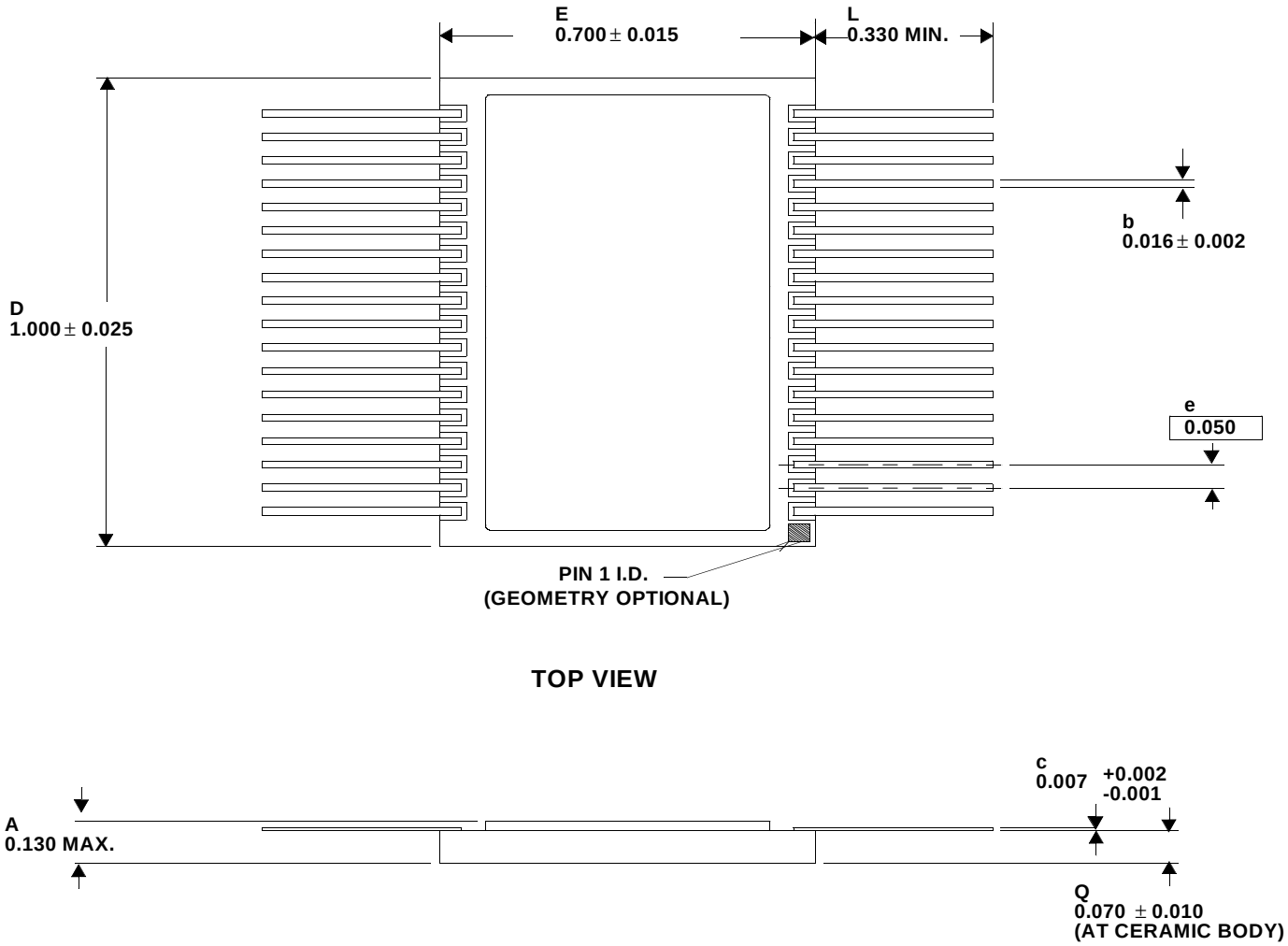
Figure 5. Low V_{DD} Data Retention Waveform



Notes:
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = V_{DD}/2).

Figure 6. AC Test Loads and Input Waveforms

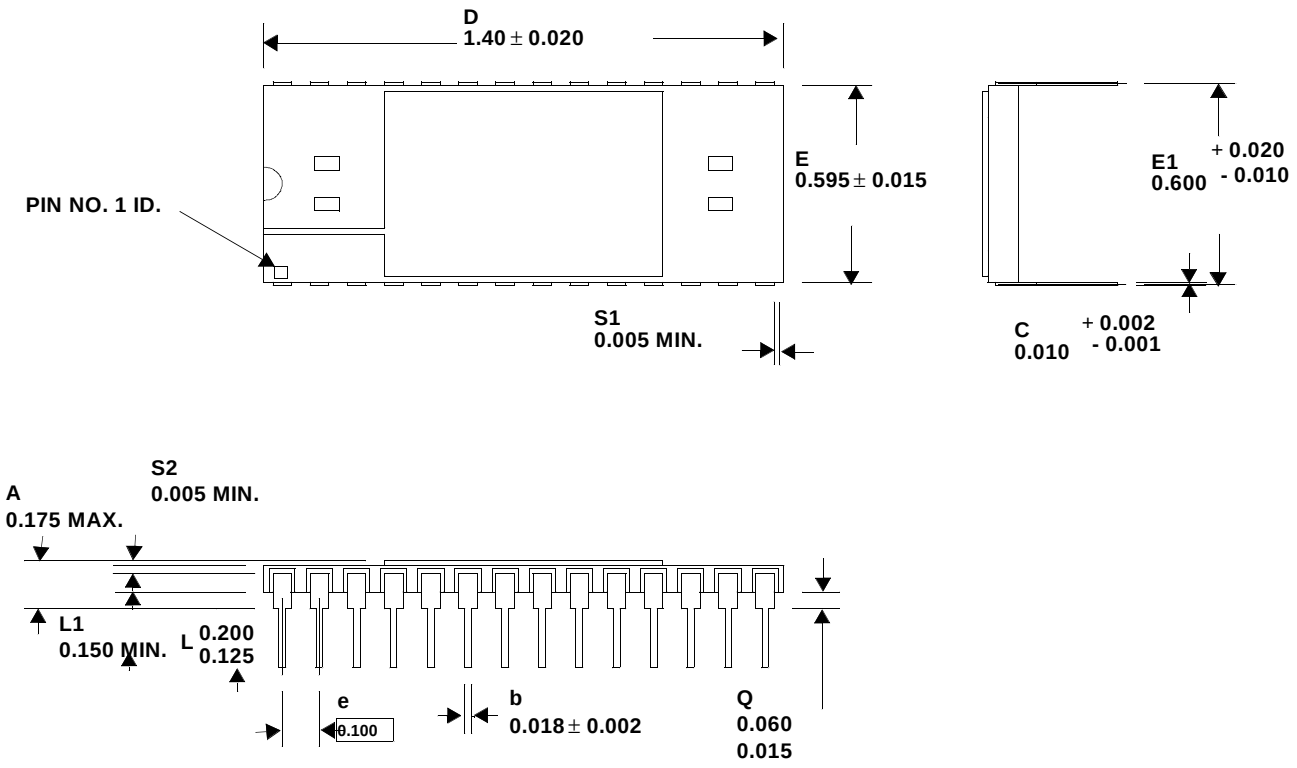
PACKAGING



Notes:

1. All package finishes are per MIL-PRF-38535.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-STD-1835.

Figure 7a. 36-pin Ceramic FLATPACK



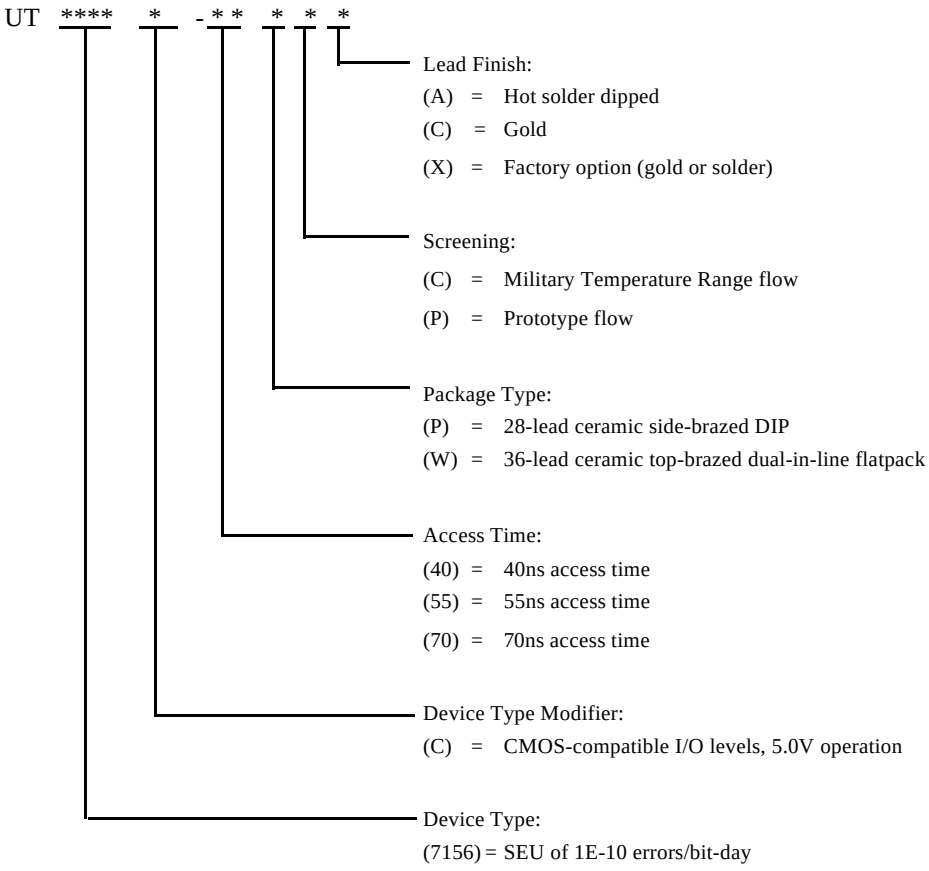
Notes:

1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-PRF-38535.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-STD-1835.

Figure 7b. 28-pin Ceramic DIP Package

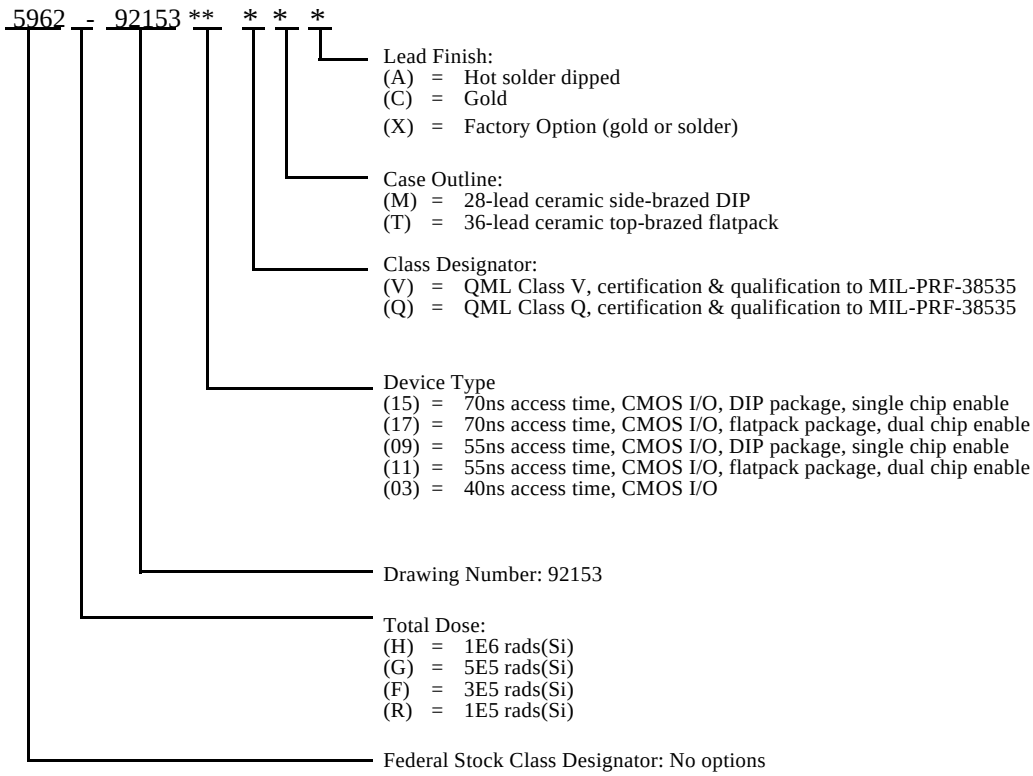
ORDERING INFORMATION

256K SRAM:



Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

256K SRAM: SMD



Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering then the part marking is at the factory's option and will match the lead finish "A" (solder) or "C" (gold).

Notes