PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

M5M51004CJ-12,-15,-20

1048576-BIT (262144-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M51004CJ are a family of 262144-word by 4-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high speed application.

The M5M51004CJ are offered in a 28-pin plastic small outline J-lead package (SOJ).

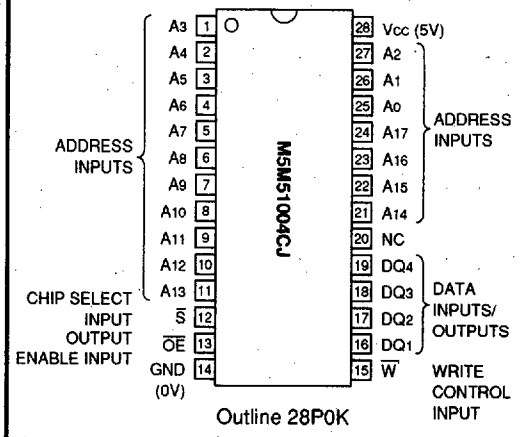
These devices operate on a single 5V supply, and are directly TTL compatible. They include a power down feature as well.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	stand-by (max)
M5M51004CJ-12	12ns	150mA	10mA
M5M51004CJ-15	15ns	140mA	
M5M51004CJ-20	20ns	130mA	

- Single +5V power supply
- Fully staric operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by $\overline{S}$
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

PIN CONFIGURATION (TOP VIEW)



Outline 28P0K

NC:NO CONNECTION

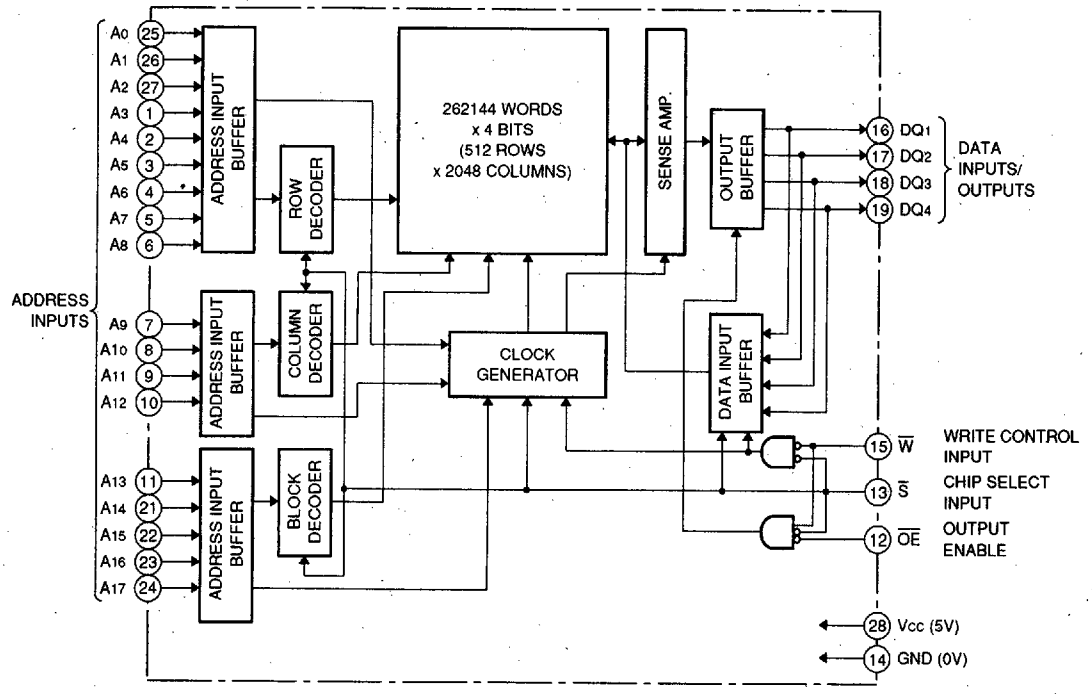
APPLICATION

High-speed memory units

PACKAGE

28pin 400mil SOJ

BLOCK DIAGRAM



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1048576-BIT (262144-WORD BY 4-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M51004C series is determined by a combination of the device control inputs $\overline{S}$ and $\overline{W}$. Each mode is summarized in the function table shown in next page.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$ whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state ($\overline{S}$=L).

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and write are disabled. In this mode the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$.

Signal-S controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	DIN	Active
L	H	L	Read	DOUT	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-3.5*~7	V
V_I	Input voltage	With respect to GND	-3.5*~Vcc+0.3	V
V_O	Output voltage	With respect to GND	-3.5*~7	V
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0~85	°C
T_{stg}	Storage temperature		-65~150	°C

* -0.5V in case of DC (Pulse width≦20ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			-0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=-4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA				0.4	V
I_I	Input current	V_I=0~Vcc				2	μA
I_{OZ}	Output current in off-state	$\overline{S}$=V_{IH}, $V_{I/O}$=0~Vcc				10	μA
I_{CC1}	Active supply current (TTL level)	$\overline{S}$=V_{IL}, Other inputs=V_{IH} or V_{IL}, Output-open, (duty 100%)	AC (12ns cycle)			150	mA
			AC (15ns cycle)			140	
			AC (20ns cycle)			130	
			DC		70	90	
I_{CC2}	Stand-by supply current (TTL level)	$\overline{S}$=V_{IH}	AC (12/15ns cycle)			50	mA
			AC (20ns cycle)			40	
			DC			30	
I_{CC3}	Stand-by current (MOS level)	$\overline{S}$≧Vcc-0.2V, Other inputs V_I≦0.2V or V_I≧Vcc-0.2V			1	10	mA

* -3.0V in case of AC (Pulse width≦20ns)

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V, Ta=25°C
3: CI, Co are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level ..... V_{IH}=3.0V, V_{IL}=0.0V
Input rise and fall time 3ns
Input timing reference level ..... V_{IH}=1.5V, V_{IL}=1.5V
Reference level ..... V_{OH}=1.5V, V_{OL}=1.5V
Output loads ..... Fig. 1, Fig. 2

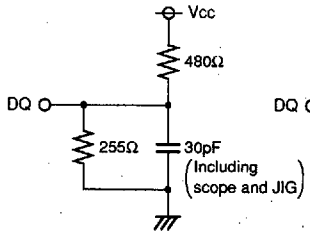


Fig.1 Output load

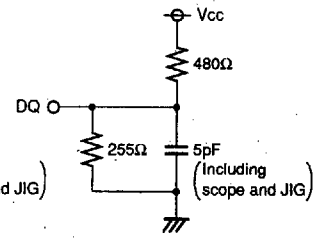


Fig.2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

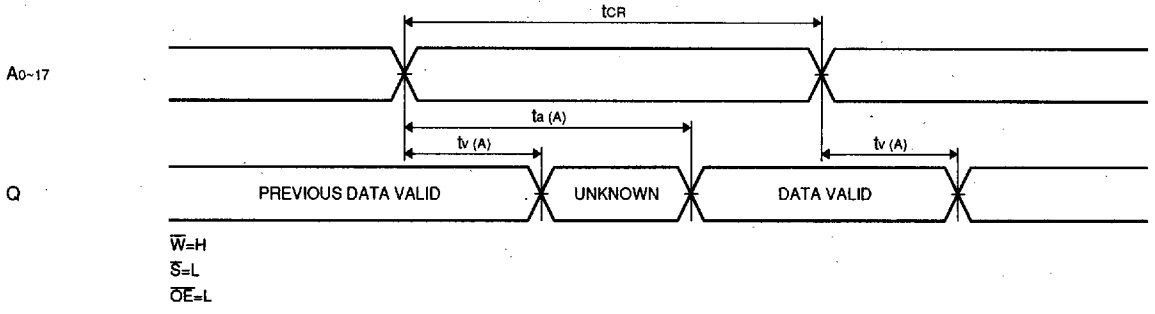
Symbol	Parameter	Limits						Unit
		M5M51004CJ-12		M5M51004CJ-15		M5M51004CJ-20		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	12		15		20		ns
$t_{a(A)}$	Address access time		12		15		20	ns
$t_{a(S)}$	Chip select 1 access time		12		15		20	ns
$t_{a(OE)}$	Output enable access time		6		8		10	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	7	0	7	0	10	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	4		4		5		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{v(A)}$	Data valid time after address change	4		4		5		ns
t_{PU}	Power-up time after $\overline{S}$ low	0		0		0		ns
t_{PD}	Power-down time after $\overline{S}$ high		12		15		20	ns

(3) WRITE CYCLE

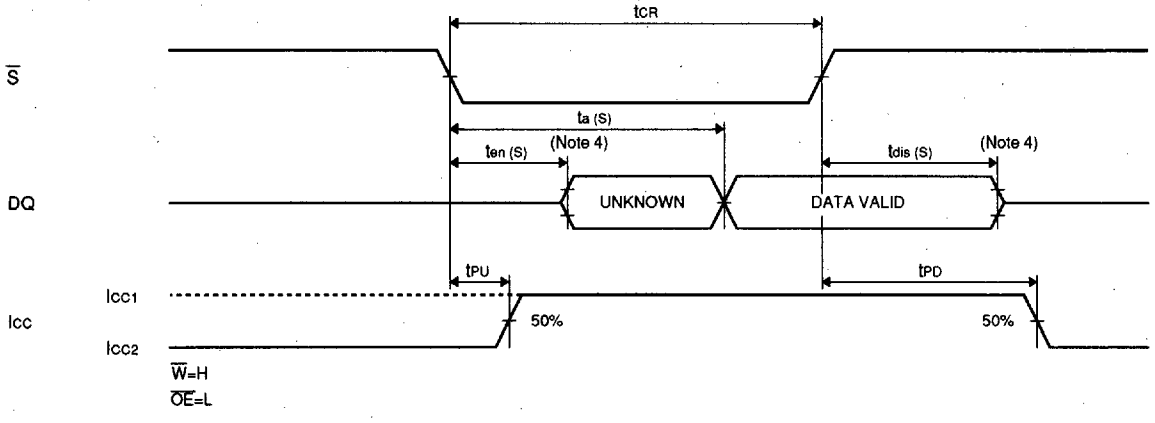
Symbol	Parameter	Limits						Unit
		M5M51004CJ-12		M5M51004CJ-15		M5M51004CJ-20		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	12		15		20		ns
$t_{w(W)}$	Write pulse width	10		12		15		ns
$t_{su(A)}$	Address setup time	0		0		0		ns
$t_{su(A-\overline{WH})}$	Address setup time with respect to $\overline{W}$	10		12		15		ns
$t_{su(S)}$	Chip select 1 setup time	10		12		15		ns
$t_{su(D)}$	Data setup time	6		8		12		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	6	0	7	0	10	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	6	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns

(4) TIMING DIAGRAMS

Read cycle 1

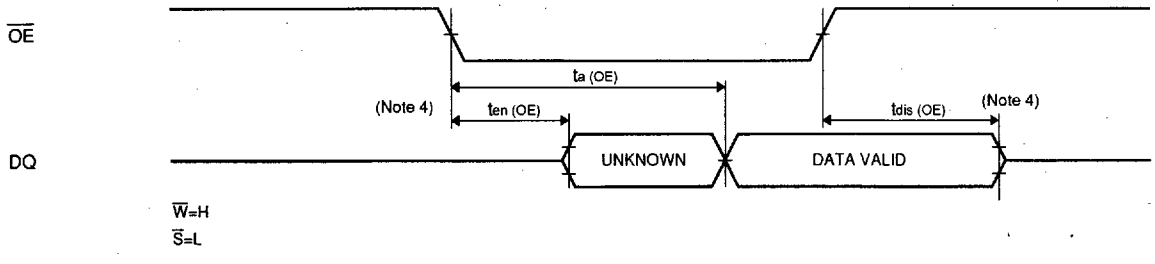


Read cycle 2 (Note 4)



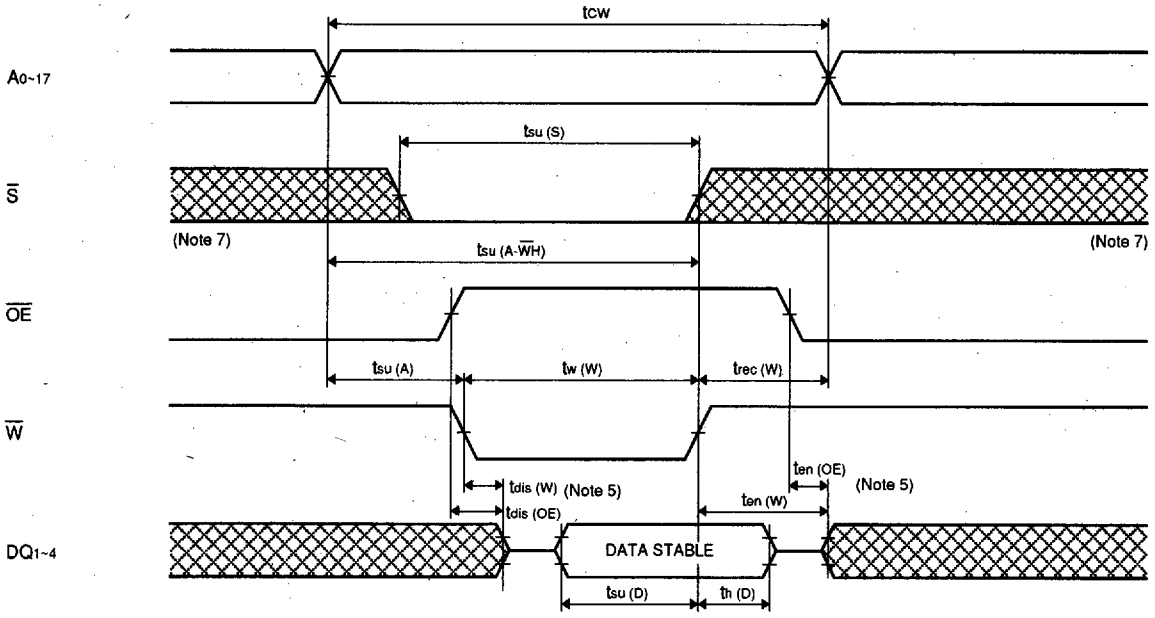
Note 4: Addresses valid prior to or coincident with $\overline{S}$ transition low.
5: Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 6)

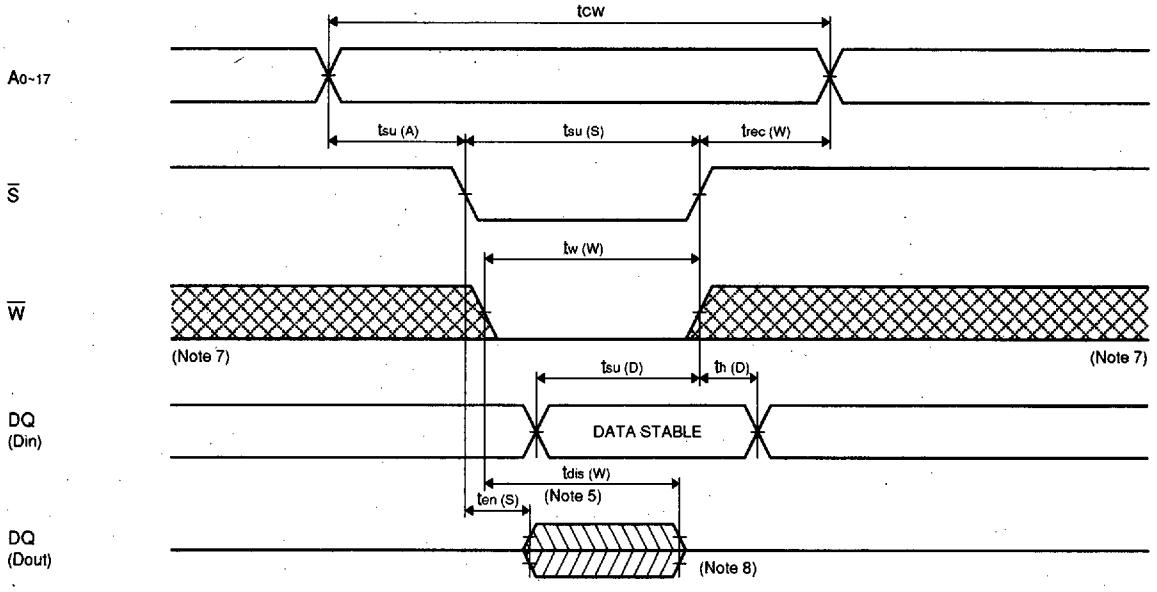


Note 6: Addresses and $\overline{S}$ valid prior to $\overline{OE}$ transition low by (ta (A)-ta (OE)), (ta (S)-ta (OE)).

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 7: Hatching indicates the state is don't care.
8: When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.
9: ten, tdis are periodically sampled and are not 100% tested.