Synchronous 512 x 9 FIFO
Synchronous 2K x 9 FIFO

Features

- **512 x 9 (CY7C441) and 2K x 9 (CY7C442) FIFO buffer memory**
- **Ultra-high-speed 70 MHz operation**
- **Supports free-running 50% (±10%) duty cycle clock inputs**
- **Empty, almost empty, and almost full status flags**
- **Width-expandable**
- **Fully asynchronous and simultaneous read and write operation**
- **Rising-edge triggered clock inputs**
- **Independent read and write enable pins**
- **Registered data inputs and outputs**
- **Available in 300-mil 28-pin DIP, PLCC, LCC, and SOJ packages**
- **Center power and ground pins for reduced noise**
- **Dual-port RAM cell**
- **Proprietary 0.8μ CMOS technology**
- **TTL compatible**

Functional Description

The CY7C441 and CY7C442 are ultra-high-speed low-power first-in first-out (FIFO) memories with registered (synchronous) interfaces and status flags. The CY7C441 has a 512 x 9-bit memory array, while the CY7C442 has a 2048 x 9-bit wide array. These devices provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces and communications buffering.

Both FIFOs have 9-bit input and output ports. The input port is controlled by a free-running 50% (±10%) duty-cycle clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is low, data is written into the synchronous FIFO on the rising edge of CKW. The output port is controlled in a similar manner by a free-running read clock (CKR) and the read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write operations. Clock frequencies up to 70 MHz are acceptable.

The synchronous FIFOs have two fixed status flags, F1 and F2, which indicate empty, almost empty, and almost full states. The empty and almost empty status is updated exclusively by RCK while almost full is updated exclusively by WCK. This architecture guarantees that the flags maintain their status for a minimum of one clock cycle.

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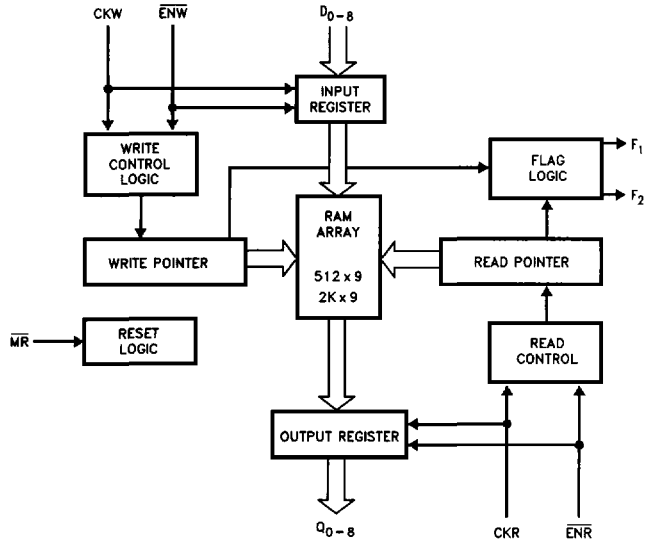
Logic Block Diagram



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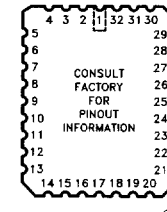
Pin Configurations

PLCC/LCC
Top View



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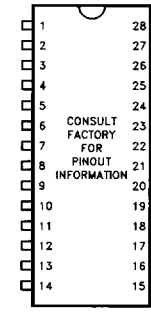
DIP
Top View



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