10231B,F

FEATURES

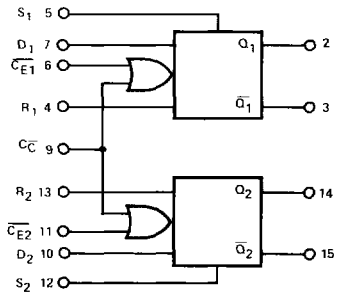
- f_{TOG} = 200 MHz MIN = 225 MHz TYP
- Fast propagation delay
  - = 2.0 ns TYP (set, reset)
  - = 2.0 ns TYP (clock)
- Low power dissipation = 270 mW/package TYP (no load)
- High fanout capability — can drive 50Ω lines
- High Z inputs — internal 50kΩ pulldowns
- High immunity from power supply variations V_{EE} = −5.2V ± 5% recommended
- Open emitter logic and bussing capability
- Pin compatible with 10130 and 10131

APPLICATIONS

- Control logic
- Status logic
- Counters
- Shift register
- Prescalers

LOGIC DIAGRAM

B, F PACKAGE



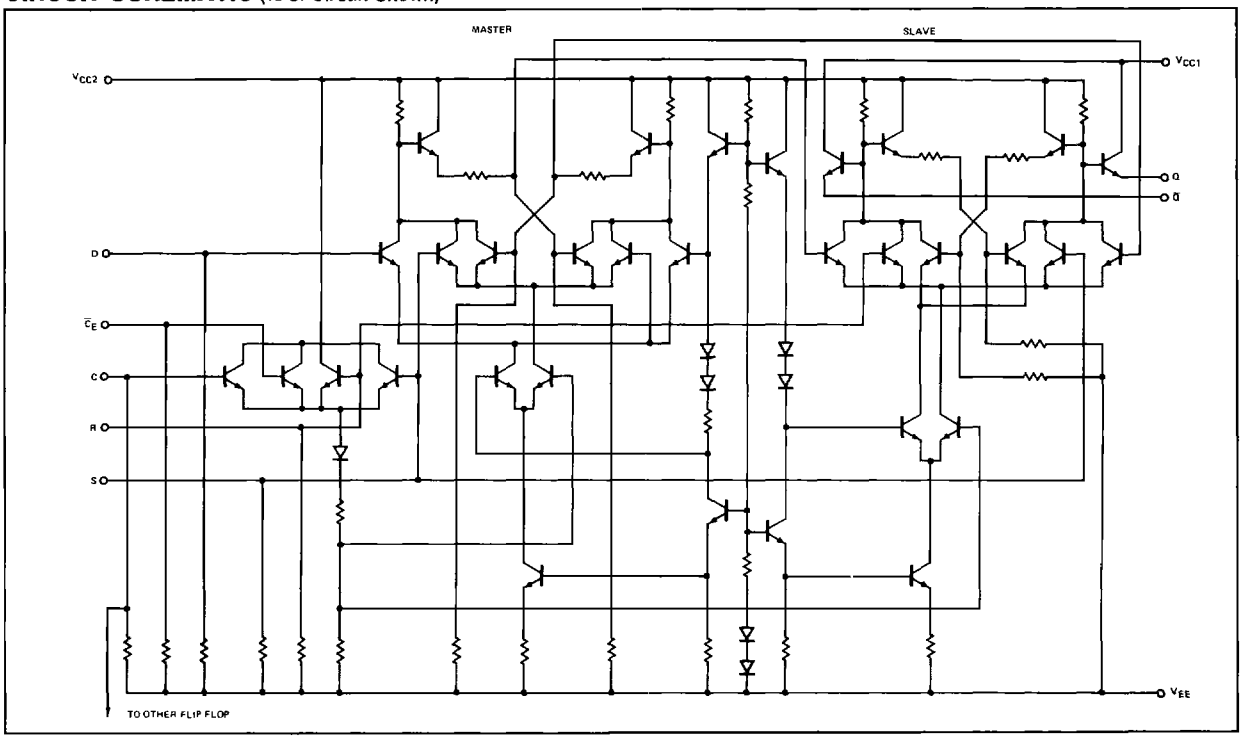
V_{CC1}=1, V_{CC}=16, V_{EE}=8
Positive logic: high level = "1"

TRUTH TABLE

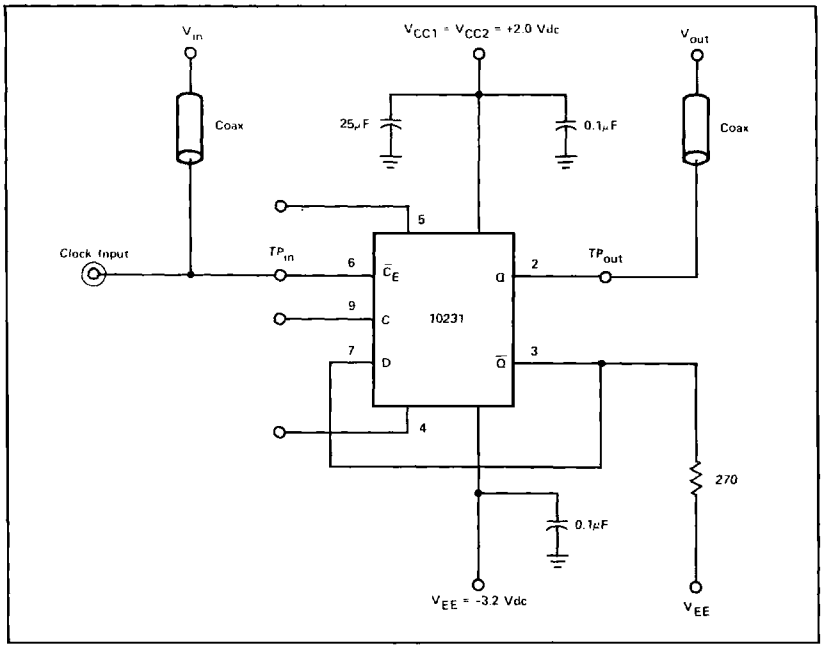
D	C*	S	R	Qn+1
ø	L	L	L	Qn
L	H	L	L	L
H	H	L	L	H
ø	*ø	H	L	H
ø	ø	L	H	L
ø	ø	H	H	N.D.

*An H represents a transition from L to H between t=n and t=n + 1
C = C_C + CE
N.D. = not defined

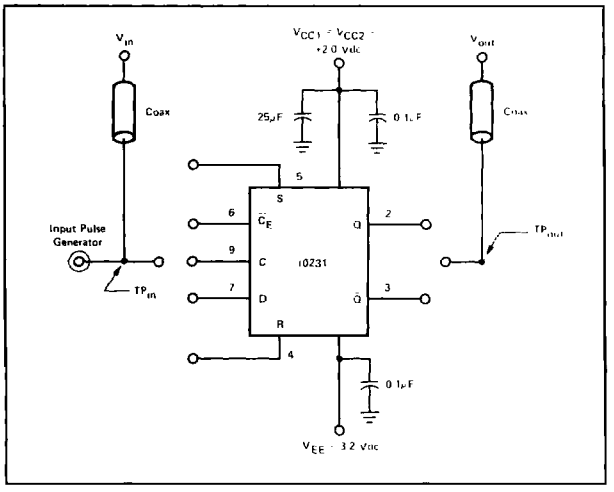
CIRCUIT SCHEMATIC (½ of Circuit Shown)



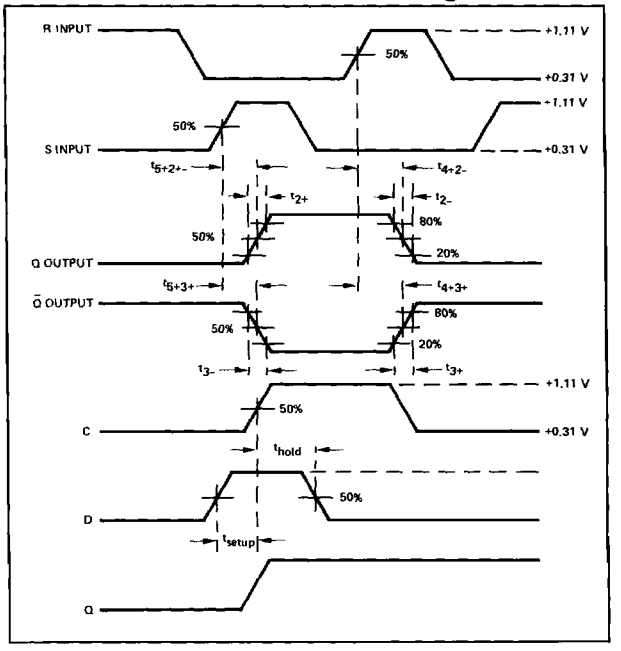
TOGGLE FREQUENCY TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTE:

Setup is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

Hold is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

LOGIC