Fast CMOS Bus Interface Registers

Product Features:

- PI74FCT821/823/825T have the same speed and drive of Bipolar FAST™ "F" series, at CMOS power levels.
  - "B" speeds at 7.5 ns max.
  - "C" speeds at 6.0 ns max.
  - "D" speeds are an industry first, at 4.2 to 5.0 ns max.
- TTL input and output levels, reducing problematic "ground bounce"
- High output drive, I_{OL} = 48 mA
- Extremely low static power (1 mW, typ.)
- Industry standard pinout, plug into existing "74F" sockets for speed enhancement at reduced power levels
- Positive edge triggered D-type flip-flops
- Buffered common clock and asynchronous Clear input
- Hysteresis on all inputs
- Packaged in 24-pin plastic DIP, surface mount SOIC, or the industry's new "1/4 size" surface mount QSOP

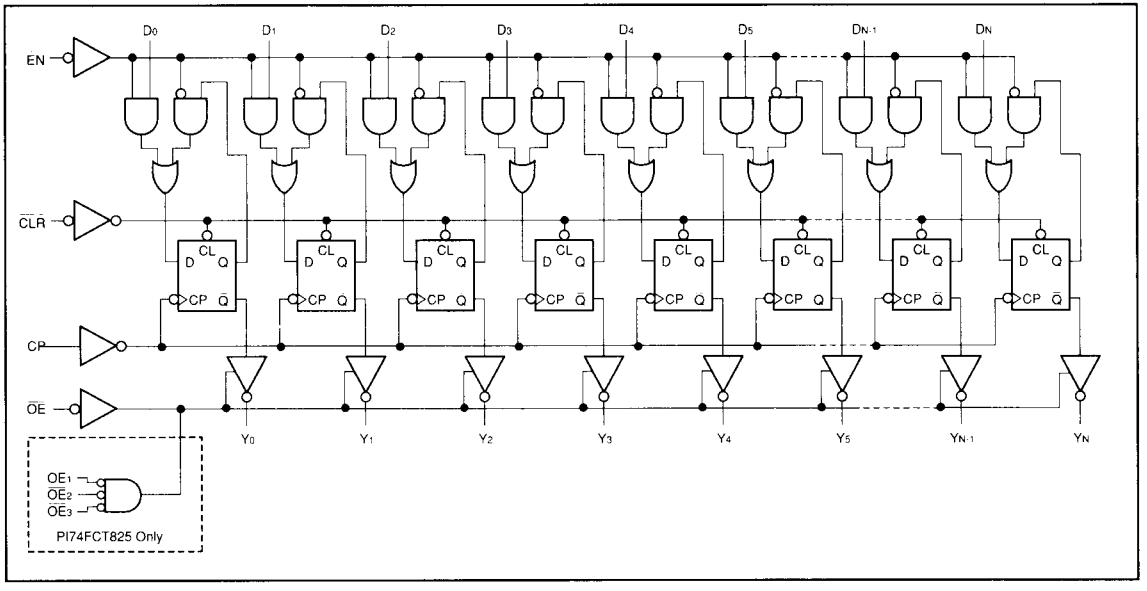
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

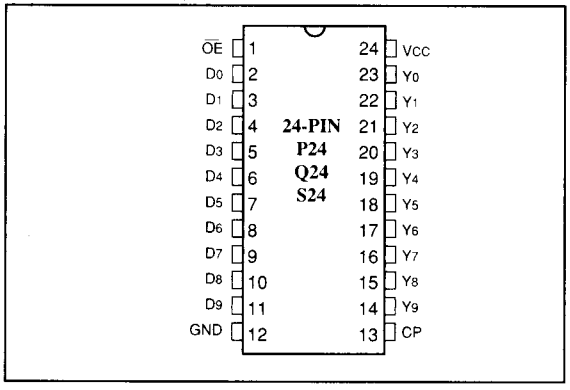
The PI74FCT821T is a 10-bit wide register designed with ten D-type flip-flops with a buffered common clock and buffered 3-state outputs. The PI74FCT823T is a 9-bit wide register designed with Clock Enable and Clear. The PI74FCT825T is an 8-bit wide register with all PI74FCT823T controls plus multiple enables. When output enable ($\overline{OE}$) is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

All products are available in three package types: 24-pin, 300 mil wide plastic DIP, 300 mil wide plastic SOIC, and the industry's new 150 mil wide QSOP (one quarter the size of an SOIC).

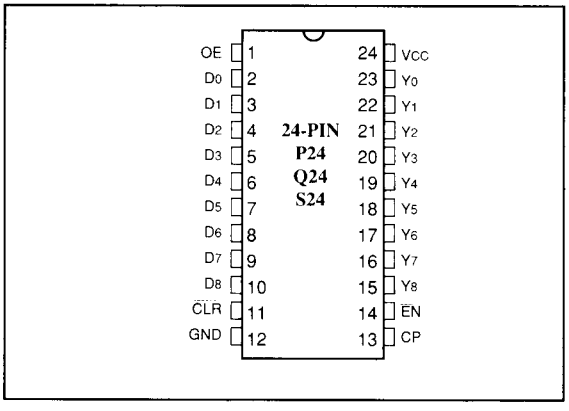
PI74FCT821/823/825 Logic Block Diagram



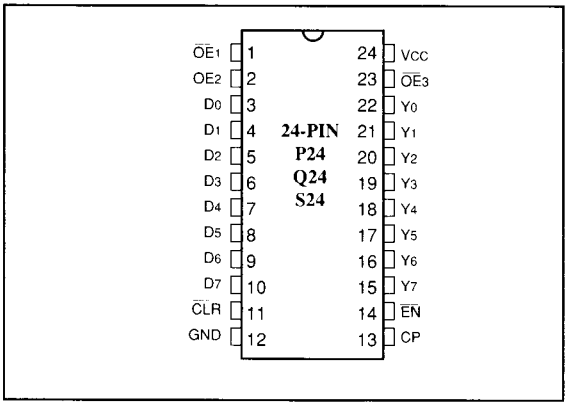
PI74FCT821T Product Pin Configuration



PI74FCT823T Product Pin Configuration



PI74FCT825T Product Pin Configuration



Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition
DN	Data Inputs
YN	3-State Outputs
CLR	Clear Input (Active LOW) (FCT823/5 Only)
EN	Clock Enable Input (Active LOW)
GND	Ground
VCC	Power

PI74FCT821/823/825T Truth Table[1]

	Inputs					Outputs	Internal
Function	CLR	EN	OE	CP	DN	YN	QN
High-Z	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
Clear	L	X	H	X	X	Z	L
	L	X	L	X	X	L	L
Hold	H	H	H	X	X	Z	NC
	H	H	L	X	X	NC	NC
Load	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
	H	L	L	↑	L	L	L
	H	L	L	↑	H	H	H

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to Vcc
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8.0 mA	2.4	3.3		V
			I_{OH} = –15.0 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.3	0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = 2.7 V			5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = 0.5 V			–5	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7 V			+10	µA
I_{OZL}	Output Current		V_{OUT} = 0.5 V			–10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} (Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5 V				100	µA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:
1. For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.2	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4 V[3]		0.5	2.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND f_i = 5 MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		1.7	4.0[5]	mA
			V_{IN} = 3.4 V V_{IN} = GND		2.2	6.0[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling f_i = 2.5 MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		4.0	7.8[5]	
			V_{IN} = 3.4 V V_{IN} = GND		6.2	16.8[5]	

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0 V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4 V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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PI74FCT821T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT821AT Com. Min	FCT821AT Com. Max	FCT821BT Com. Min	FCT821BT Com. Max	FCT821CT Com. Min	FCT821CT Com. Max	FCT821DT Com. Min	FCT821DT Com. Max	Unit
t_{PLH}	Propagation Delay	C_L = 50 pF	1.5	10.0	1.5	7.5	1.5	6.0	1.5	4.2	ns
t_{PHL}	CP to Y_N	R_L = 500Ω									
	($\overline{OE}$ = LOW)	C_L = 300 pF[3]	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.0	ns
		R_L = 500Ω									
t_{SU}	Set-up Time HIGH or	C_L = 50 pF	4.0	—	3.0	—	3.0	—	2.0	—	ns
	LOW, D_N to CP	R_L = 500Ω									
t_H	Hold Time HIGH or		2.0	—	1.5	—	1.5	—	1.0	—	ns
	LOW, D_N to CP										
t_{SU}	Set-up Time HIGH or		4.0	—	3.0	—	3.0	—	3.0	—	ns
	LOW, $\overline{EN}$ to CP										
t_H	Hold Time HIGH or		2.0	—	0	—	0	—	0	—	ns
	LOW, $\overline{EN}$ to CP										
t_{PHL}	Propagation Delay,		1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	ns
	$\overline{CLR}$ to Y_N										
t_{REM}	Recovery Time,		6.0	—	6.0	—	6.0	—	3.0	—	ns
	$\overline{CLR}$ to CP										
t_W	Clock Pulse Width		7.0	—	5.0	—	6.0	—	3.0	—	ns
	HIGH or LOW										
t_W	$\overline{CLR}$ Pulse Width		6.0	—	6.0	—	6.0	—	3.0	—	ns
	LOW										
t_{PZH}	Output Enable Time	C_L = 50 pF	1.5	11.5	1.5	8.0	1.5	7.0	1.5	4.8	ns
t_{PZL}	$\overline{OE}$ to Y_N	R_L = 500Ω									
		C_L = 300 pF[3]	1.5	23.0	1.5	15.0	1.5	12.5	1.5	9.0	ns
		R_L = 500Ω									
t_{PHZ}	Output Disable Time	C_L = 50 pF	1.5	7.0	1.5	6.5	1.5	6.2	1.5	4.0	ns
t_{PLZ}	$\overline{OE}$ to Y_N	R_L = 500Ω									
		C_L = 300 pF[3]	1.5	8.0	1.5	7.5	1.5	6.5	1.5	4.0	ns
		R_L = 500Ω									

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT823T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT823AT Com. Min	FCT823AT Com. Max	FCT823BT Com. Min	FCT823BT Com. Max	FCT823CT Com. Min	FCT823CT Com. Max	FCT823DT Com. Min	FCT823DT Com. Max	Unit
t_{PLH}	Propagation Delay	C_L = 50 pF	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	ns
t_{PHL}	CP to Y_N	R_L = 500Ω									
	($\overline{OE}$ = LOW)	C_L = 300 pF[3]	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	ns
		R_L = 500Ω									
t_{SU}	Set-up Time HIGH or	C_L = 50 pF	4.0	—	3.0	—	3.0	—	2.0	—	ns
	LOW, D_N to CP	R_L = 500Ω									
t_H	Hold Time HIGH or		2.0	—	1.5	—	1.5	—	1.0	—	ns
	LOW, D_N to CP										
t_{SU}	Set-up Time HIGH or		4.0	—	3.0	—	3.0	—	3.0	—	ns
	LOW, $\overline{EN}$ to CP										
t_H	Hold Time HIGH or		2.0	—	0	—	0	—	0	—	ns
	LOW, $\overline{EN}$ to CP										
t_{PHL}	Propagation Delay,		1.5	13.0	1.5	9.0	1.5	8.0	1.5	5.0	ns
	$\overline{CLR}$ to Y_N										
t_{REM}	Recovery Time,		6.0	—	6.0	—	6.0	—	3.0	—	ns
	$\overline{CLR}$ to CP										
t_W	Clock Pulse Width		7.0	—	5.0	—	6.0	—	3.0	—	ns
	HIGH or LOW										
t_W	$\overline{CLR}$ Pulse Width		6.0	—	6.0	—	6.0	—	3.0	—	ns
	LOW										
t_{PZH}	Output Enable Time	C_L = 50 pF	1.5	11.5	1.5	8.0	1.5	7.0	1.5	4.8	ns
t_{PZL}	$\overline{OE}$ to Y_N	R_L = 500Ω									
		C_L = 300 pF[3]	1.5	23.0	1.5	15.0	1.5	12.5	1.5	9.0	ns
		R_L = 500Ω									
t_{PHZ}	Output Disable Time	C_L = 50 pF	1.5	7.0	1.5	6.5	1.5	6.2	1.5	4.0	ns
t_{PLZ}	OE to Y_N	R_L = 500Ω									
		C_L = 300 pF[3]	1.5	8.0	1.5	7.5	1.5	6.5	1.5	4.0	ns
		R_L = 500Ω									

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

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PI74FCT825T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	FCT825AT Com. Min	FCT825AT Com. Max	FCT825BT Com. Min	FCT825BT Com. Max	FCT825CT Com. Min	FCT825CT Com. Max	FCT825DT Com. Min	FCT825DT Com. Max	Unit
tPLH tPHL	Propagation Delay CP to Yn ($\overline{OE}$ = LOW)	CL = 50 pF RL = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.5	ns
		CL = 300 pF[3] RL = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	9.6	ns
tSU	Set-up Time HIGH or LOW, Dn to CP	CL = 50 pF RL = 500Ω	4.0	—	3.0	—	3.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Dn to CP		2.0	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW, $\overline{EN}$ to CP		4.0	—	3.0	—	3.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, $\overline{EN}$ to CP		2.0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to Yn		1.5	13.0	1.5	9.0	1.5	8.0	1.5	5.5	ns
tREM	Recovery Time, $\overline{CLR}$ to CP		6.0	—	6.0	—	6.0	—	3.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	5.0	—	6.0	—	3.0	—	ns
tW	$\overline{CLR}$ Pulse Width LOW		6.0	—	6.0	—	6.0	—	3.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Yn	CL = 50 pF RL = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	1.5	4.8	ns
		CL = 300 pF[3] RL = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yn	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	4.0	ns
		CL = 300 pF[3] RL = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	6.1	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.