ICS8304-01

LOW SKEW, 1-TO-4 LVCMOS / LVTTL INVERTING FANOUT BUFFER

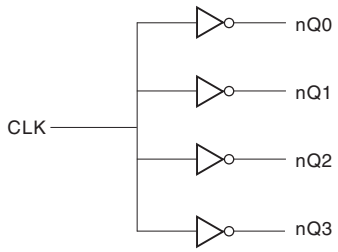
GENERAL DESCRIPTION

The ICS8304-01 is a low skew, 1-to-4 Inverting Fanout Buffer. The ICS8304-01 is characterized at full 3.3V for input V_{DD}, and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the ICS8304-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

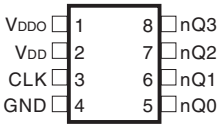
FEATURES

- 4 LVCMOS / LVTTL outputs
- LVCMOS/LVTTL clock input
- Maximum output frequency: 166MHz
- Output skew: 50ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V input, outputs may be either 3.3V or 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8304-01
8-Lead SOIC
3.8mm x 4.8mm x 1.47mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDO}	Power		Output supply pin.
2	V_{DD}	Power		Core supply pin.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4	GND	Power		Power supply ground.
5	nQ0	Output		Inverted version of clock input. LVCMOS / LVTTL interface levels.
6	nQ1	Output		Inverted version of clock input. LVCMOS / LVTTL interface levels.
7	nQ2	Output		Inverted version of clock input. LVCMOS / LVTTL interface levels.
8	nQ3	Output		Inverted version of clock input. LVCMOS / LVTTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V			15	pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			7		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_{DD}	-0.5V to V_{DD} + 0.5 V
Outputs, V_{DDO}	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				15	mA
I_{DDO}	Output Supply Current				8	mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information Section", "3.3V Output Load Test Circuit".

TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 166MHz	2.3		3.5	ns
*t*sk(o)	Output Skew; NOTE 2, 4				50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				600	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle	f ≤ 166MHz	40		60	%

All parameters measured at 166MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output. Measured from the rising edge of the input to the falling edge of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 3C. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				15	mA
I_{DDO}	Output Supply Current				8	mA

TABLE 3D. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		2.1			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

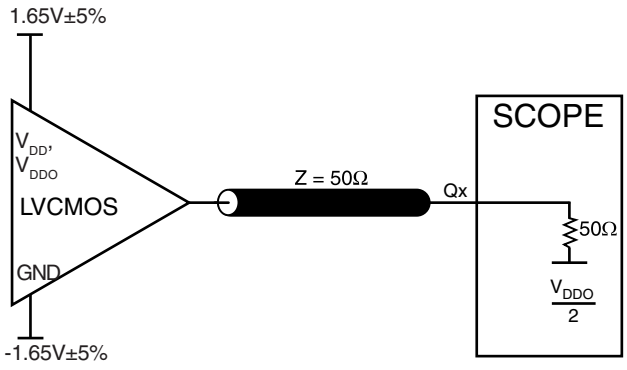
NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information Section, "3.3V/2.5V Output Load Test Circuit".

TABLE 4B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

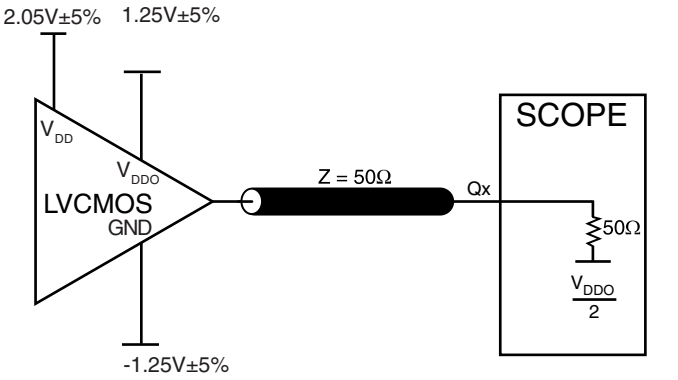
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				166	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 166MHz	2.5		3.6	ns
*t*sk(o)	Output Skew; NOTE 2, 4				50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				600	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle	f ≤ 166MHz	40		60	%

All parameters measured at 166MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output. Measured from the rising edge of the input to the falling edge of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

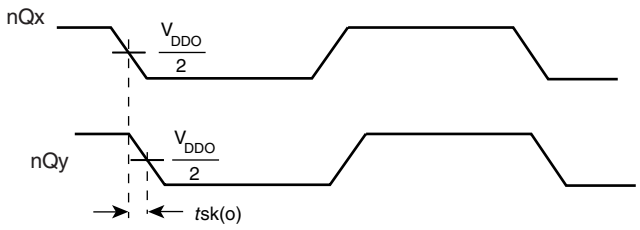
PARAMETER MEASUREMENT INFORMATION



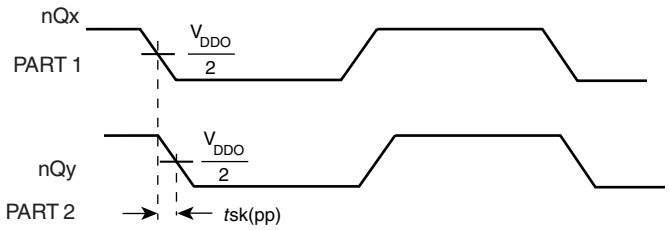
3.3V OUTPUT LOAD AC TEST CIRCUIT



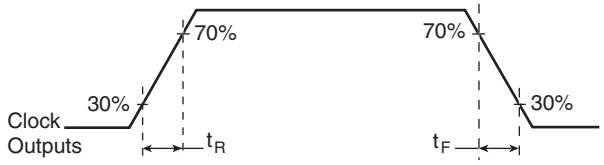
3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT



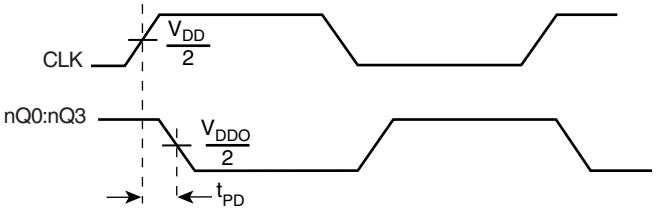
OUTPUT SKEW



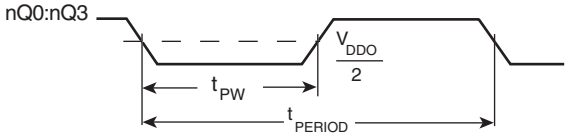
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



OUTPUT DUTY CYLE/PULSE WIDTH/PERIOD

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8304-01 is: 416

PACKAGE OUTLINE - SUFFIX M FOR 8 LEAD SOIC

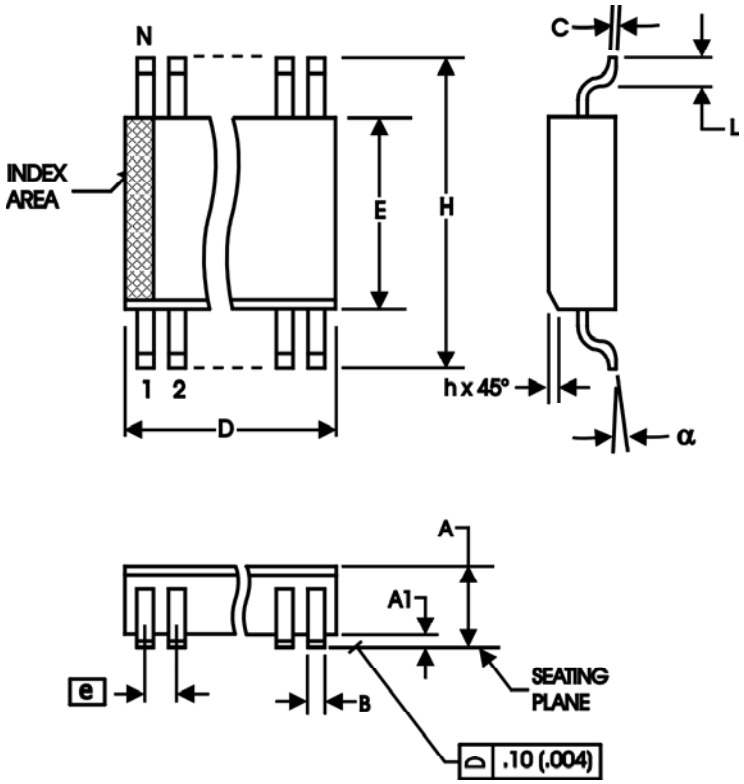


TABLE 6. PACKAGE DIMENSIONS - SUFFIX M

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 6. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8304AM-01	8304AM01	8 lead SOIC	tube	0°C to 70°C
8304AM-01T	8304AM01	8 lead SOIC	2500 tape & reel	0°C to 70°C
8304AM-01LF	8304A01L	8 lead "Lead-Free" SOIC	tube	0°C to 70°C
8304AM-01LFT	8304A01L	8 lead "Lead-Free" SOIC	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	4A 4B	3 4 6 & 7	AC Characteristics Table - revised tp_{LH} row to t_{PD} and revised NOTE 1. Deleted tp_{HL} row. AC Characteristics Table - revised tp_{LH} row to t_{PD} and revised NOTE 1. Deleted tp_{HL} row. Updated Figures.	4/9/02
C	4A 4B	3 4	AC Characteristics Table - changed tsk(pp) Part-to-Part Skew from 250ps Max. to 600ps Max. AC Characteristics Table - changed tsk(pp) Part-to-Part Skew from 250ps Max. to 600ps Max.	5/20/02
C	6	10	Ordering Information, updated marking from 8304-01 to 8304AM01	6/17/02
D	T1 T2 T6	2 2 10	Pin Descripiton Table - revised V_{DD} description to read "Core supply pin." (Also changed in Power Supply tables.) Deleted *Pullup* from note. Pin Characteristics Table -C_{IN} changed 4pF max. to 4pF typical. Deleted R_{PULLUP} row. Ordering Information Table - changed Part/Order number ICS8304M-01/-01T to ICS8304AM-01/-01T. Updated format throughout data sheet.	3/1/04
D	T6	1 8	Features Section - added Lead-Free bullet. Ordering Information Table - add Lead-Free parts.	5/23/05
D	T6	8 10	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	7/29/10

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