



M74HCT273

OCTAL D TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED :
 $f_{MAX} = 80 \text{ MHz (TYP.) at } V_{CC} = 4.5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu A(\text{MAX.}) \text{ at } T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS :
 $V_{IH} = 2V \text{ (MIN.) } V_{IL} = 0.8V \text{ (MAX)}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4mA \text{ (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH
 74 SERIES 273



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HCT273B1R	
SOP	M74HCT273M1R	M74HCT273RM13TR
TSSOP		M74HCT273TTR

DESCRIPTION

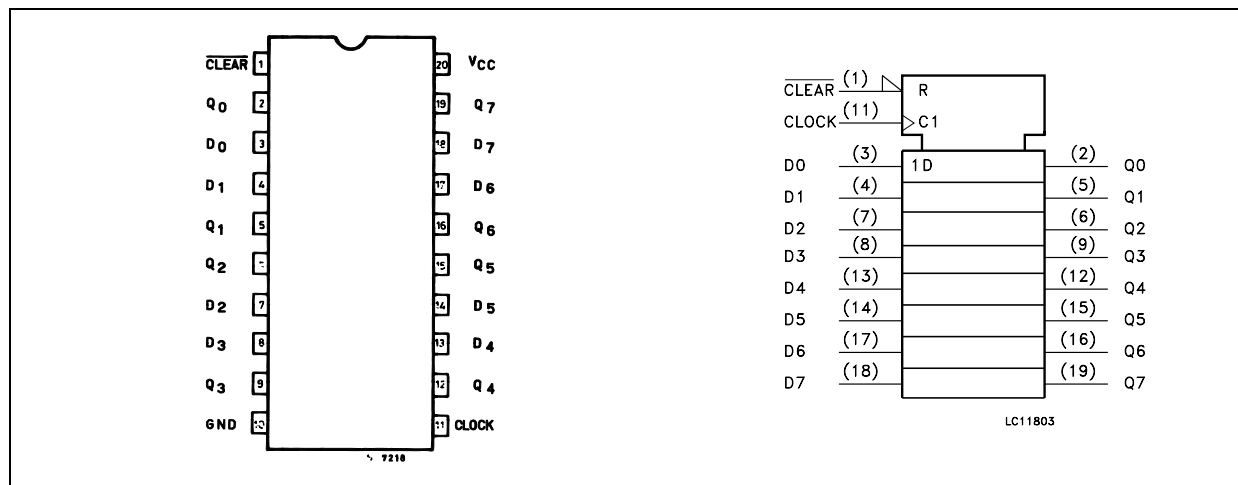
The M74HCT273 is an high speed CMOS OCTAL D TYPE FLIP FLOP WITH CLEAR fabricated with silicon gate C²MOS technology.

Information signals applied to D inputs are transferred to the Q outputs on the positive-going edge of the clock pulse.

When the $\overline{\text{CLEAR}}$ input is held low, the Q output are in the low logic level independent of the other inputs.

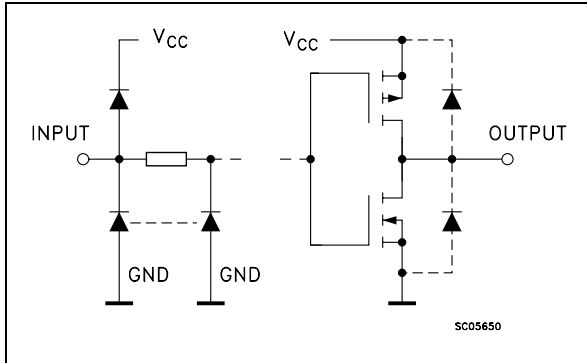
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



M74HCT273

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

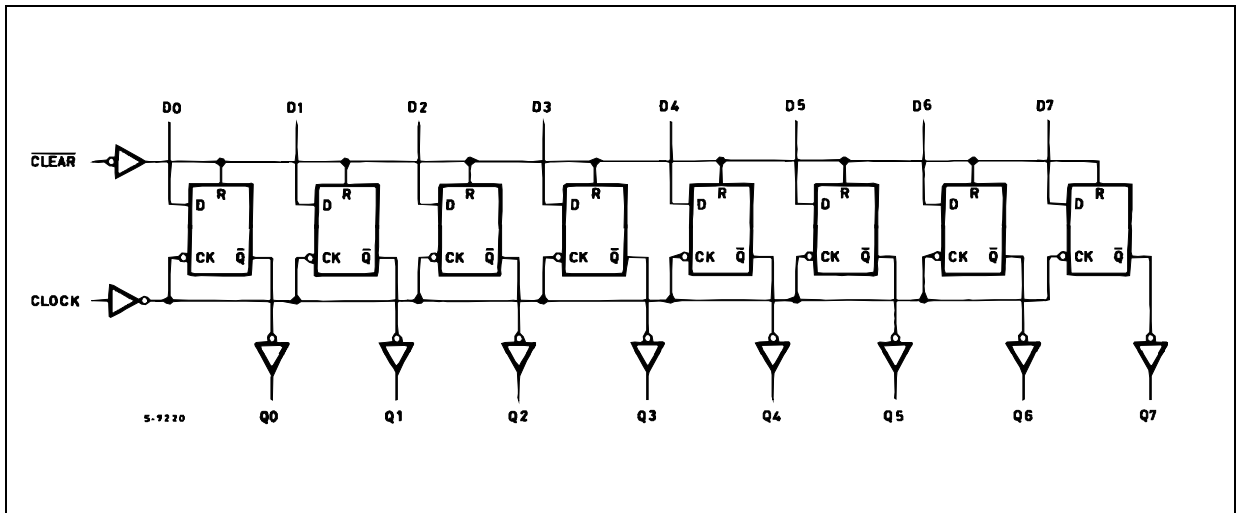
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Master Reset Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	Flip Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{\text{CLEAR}}$	CLOCK	D	Q	
L	X	X	L	CLEAR
H		L	L	
H		H	H	
H		X	Qn	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not been used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
t_r, t_f	Input Rise and Fall Time ($V_{CC} = 4.5$ to $5.5V$)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V_{IH}	High Level Input Voltage	4.5 to 5.5		2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	$I_O = -20 \mu\text{A}$	4.4	4.5		4.4		4.4		V
			$I_O = -4.0 \text{ mA}$	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	$I_O = 20 \mu\text{A}$		0.0	0.1		0.1		0.1	V
			$I_O = 4.0 \text{ mA}$		0.17	0.26		0.33		0.40	
I_I	Input Leakage Current	5.5	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	μA
I_{CC}	Quiescent Supply Current	5.5	$V_I = V_{CC}$ or GND			4		40		80	μA
ΔI_{CC}	Additional Worst Case Supply Current	5.5	Per Input pin $V_I = 0.5V$ or $V_I = 2.4V$ Other Inputs at V_{CC} or GND $I_O = 0$			2.0		2.9		3.0	mA

M74HCT273

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

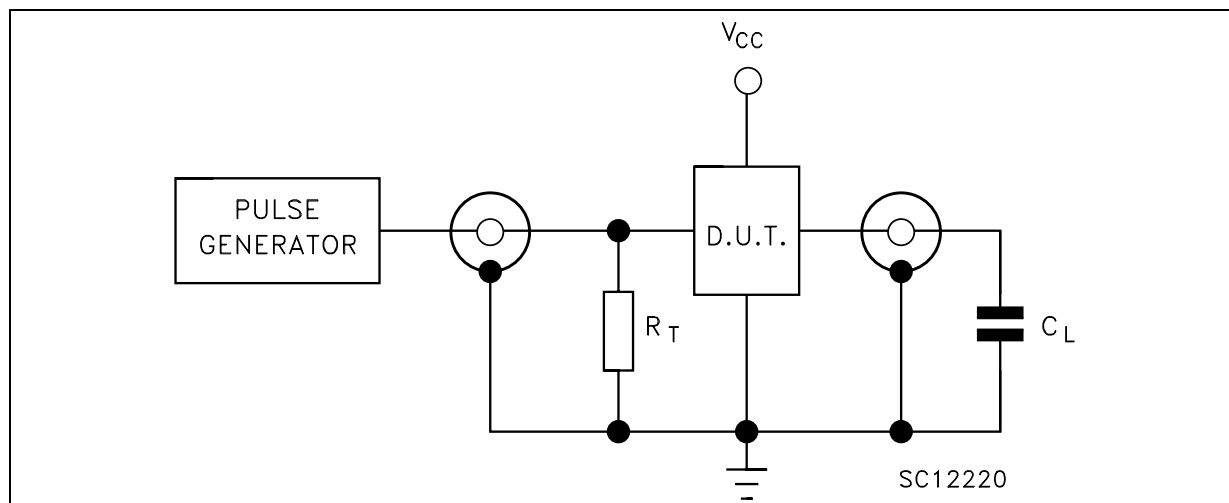
Symbol	Parameter	Test Conditions		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH} \ t_{THL}$	Output Transition Time	4.5			9	15		19		22	ns
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (CLOCK - Q)	4.5			19	30		38		45	ns
t_{PHL}	Propagation Delay Time (CLEAR - Q)	4.5			22	32		40		48	ns
f_{MAX}	Maximum Clock Frequency	4.5		30	80		24		20		MHz
$t_{W(H)} \ t_{W(L)}$	Minimum Pulse (CLOCK)	4.5			7	15		19		22	ns
$t_{W(L)}$	Minimum Pulse (CLEAR)	4.5			7	15		19		22	ns
t_s	Minimum Set-Up Time	4.5			4	15		19		22	ns
t_h	Minimum Hold Time	4.5				0		0		0	ns
t_{REM}	Minimum Removal Time (CLEAR)	4.5			4	10		13		15	ns

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			29						pF

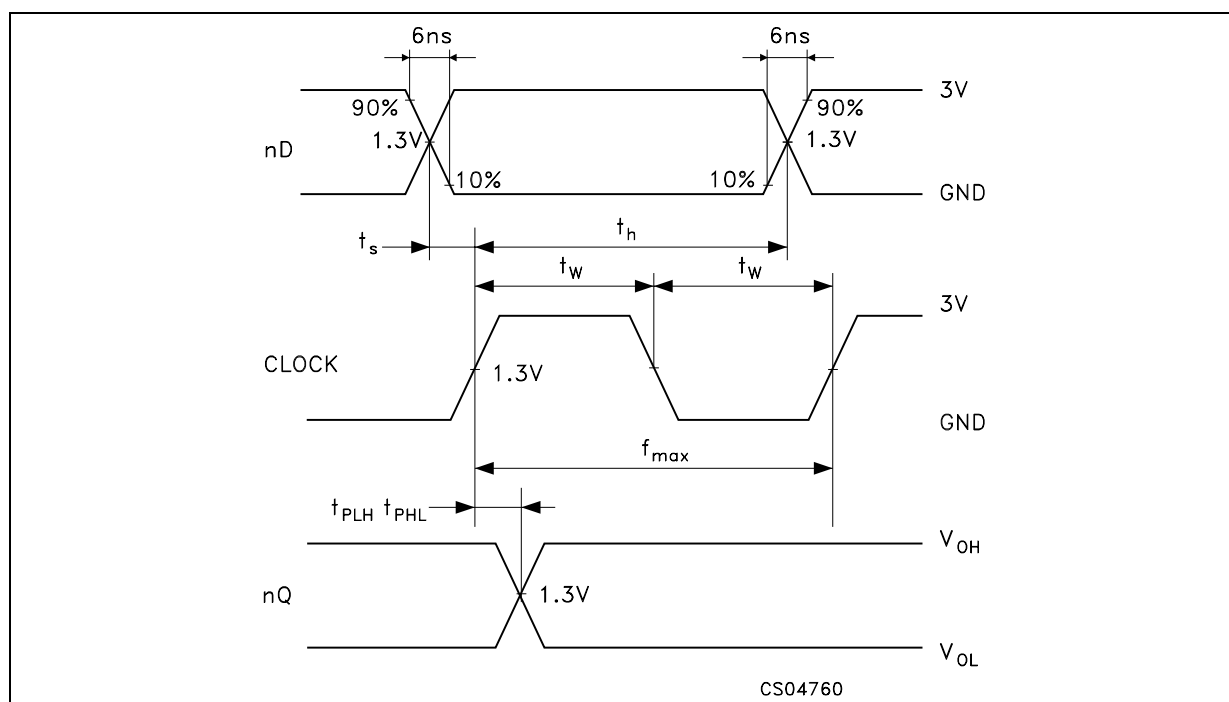
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per FLIP FLOP), and the total CPD when n pcs of FLIP FLOP operate can be gained by the following equations: $CPD(\text{total}) = 32 + 11 \times n$

TEST CIRCUIT

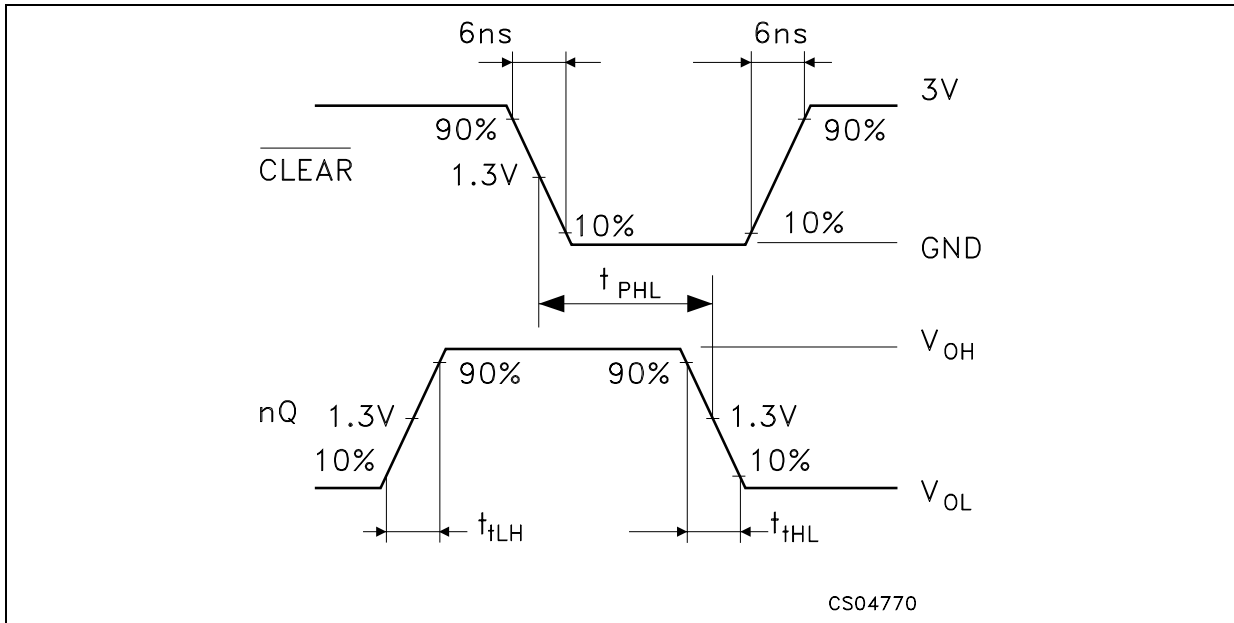


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

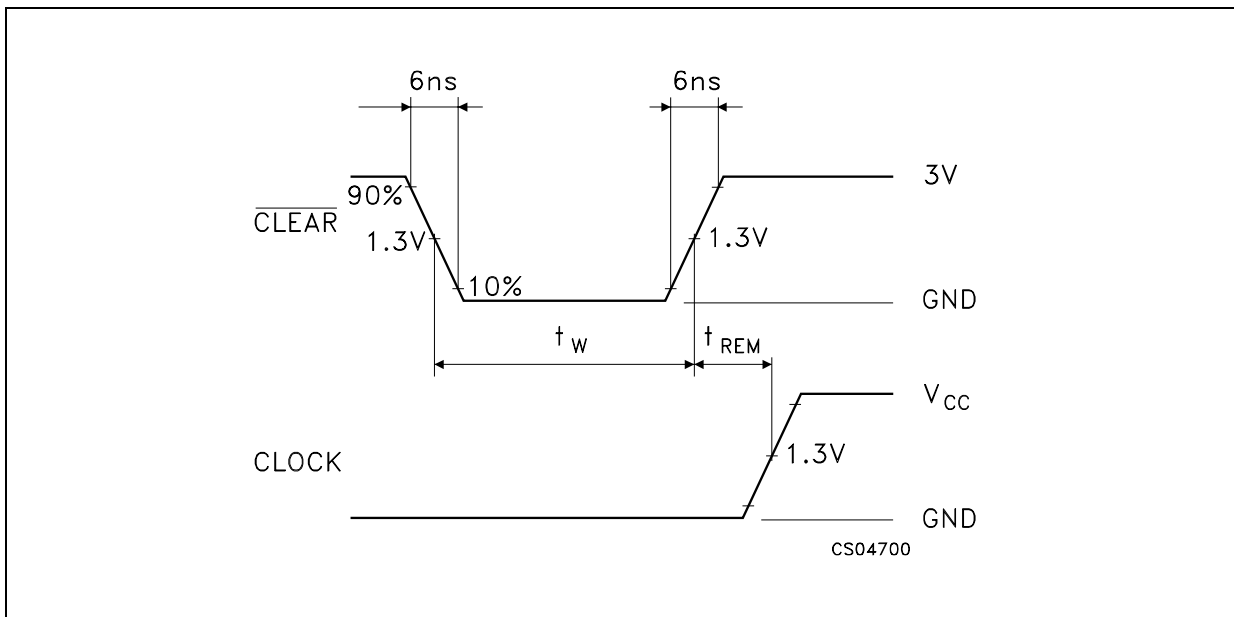
WAVEFORM 1: PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (CLOCK), SETUP AND HOLD TIME (nD TO CLOCK), CLOCK MAXIMUM FREQUENCY ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 2 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)

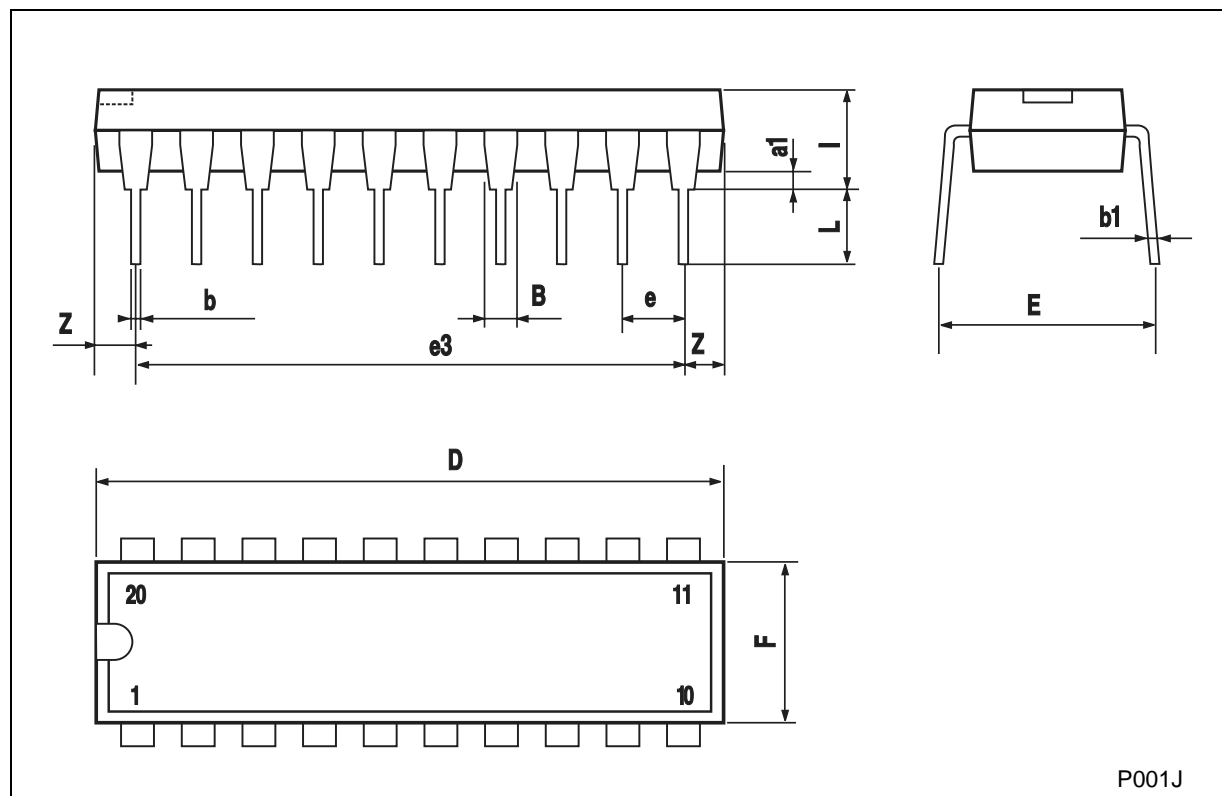


WAVEFORM 3 : MINIMUM PULSE WIDTH ($\overline{\text{CLEAR}}$), MINIMUM REMOVAL TIME ($\overline{\text{CLEAR}}$ TO CLOCK)(f=1MHz; 50% duty cycle)



Plastic DIP-20 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>