

MM54HC157/MM74HC157/MM54HC158/MM74HC158



T-67-21-51

MM54HC157/MM74HC157 Quad 2-Input Multiplexer MM54HC158/MM74HC158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed Quad 2-to-1 Line data selector/Multiplexers utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

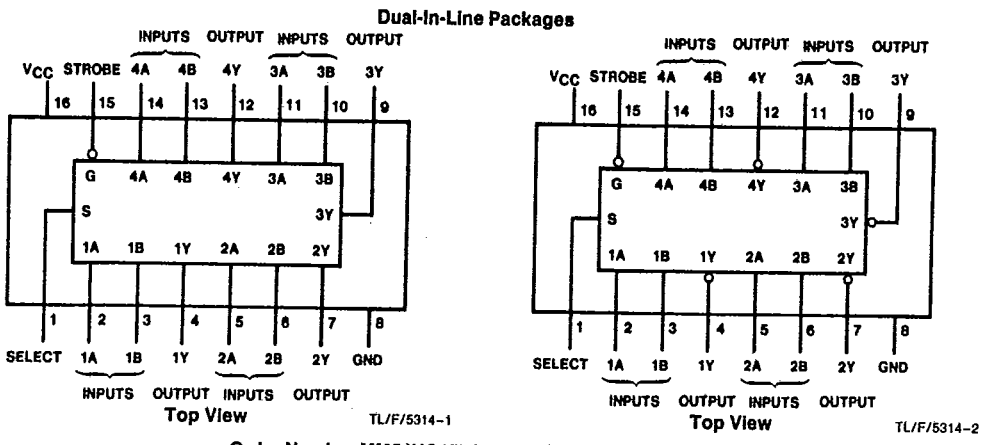
These devices each consist of four 2-input digital multiplexers with common select and STROBE inputs. On the MM54HC157/MM74HC157, when the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0". The MM54HC158/MM74HC158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns data to any output
- Wide power supply range: 2-6V
- Low power supply quiescent current: 80 μA maximum (74HC Series)
- Fan-out of 10 LS-TTL loads
- Low input current: 1 μA maximum

Connection Diagrams



Function Table

Strobe	Inputs		Output Y		
	Select	A	B	HC157	HC158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	L	L

H = High Level, L = Low Level, X = Irrelevant

T-67-21-51

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to V _{CC} + 1.5V
DC Output Voltage (V _{OUT})	-0.5 to V _{CC} + 0.5V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V _{CC} or GND Current, per pin (I _{CC})	±50 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T _L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage (V _{IN} , V _{OUT})	0	V _{CC}	V
Operating Temp. Range (T _A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t _r , t _f)			
V _{CC} =2.0V		1000	ns
V _{CC} =4.5V		500	ns
V _{CC} =6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C			74HC T _A = -40 to 85°C		54HC T _A = -55 to 125°C		Units
				Typ	Guaranteed Limits						
V _{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5			V	
			4.5V		3.15	3.15	3.15		V		
			6.0V		4.2	4.2	4.2		V		
V _{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5			V	
			4.5V		1.35	1.35	1.35		V		
			6.0V		1.8	1.8	1.8		V		
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9			V	
			4.5V	4.5	4.4	4.4	4.4		V		
			6.0V	6.0	5.9	5.9	5.9		V		
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.2	3.98	3.84	3.7		V		
			6.0V	5.7	5.48	5.34	5.2		V		
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	0.1			V	
			4.5V	0	0.1	0.1	0.1		V		
			6.0V	0	0.1	0.1	0.1		V		
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	0.4		V		
			6.0V	0.2	0.26	0.33	0.4		V		
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0		μA		
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		8.0	80	160		μA		

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

3

T-67-21-51

MM54HC157/MM74HC157/MM54HC158/MM74HC158

AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, C_L=15\text{ pF}, t_r=t_f=6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

AC Electrical Characteristics $C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$ (unless otherwise specified)

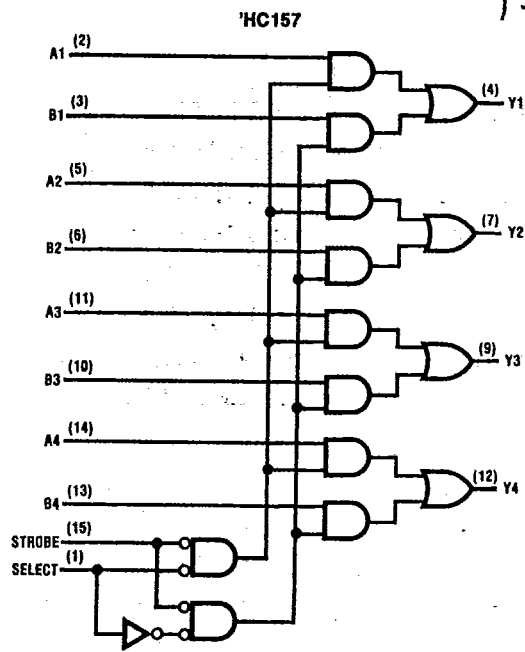
Symbol	Parameter	Conditions	V_{CC}	$T_A=25^{\circ}C$		74HC $T_A=-40\text{ to }85^{\circ}C$		54HC $T_A=-55\text{ to }125^{\circ}C$		Units
				Typ	Guaranteed Limits	Guaranteed Limits	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		2.0V	63	125	158	186	ns		
			4.5V	13	25	32	37	ns		
			6.0V	11	21	27	32	ns		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		2.0V	63	125	158	186	ns		
			4.5V	13	25	32	37	ns		
			6.0V	11	21	27	32	ns		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		2.0V	58	115	145	171	ns		
			4.5V	12	23	29	34	ns		
			6.0V	10	20	25	29	ns		
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns		
			4.5V	8	15	19	22	ns		
			6.0V	7	13	16	19	ns		
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF		
C_{PD}	Power Dissipation Capacitance (Note 5)	(per Multiplexer)		57				pF		

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

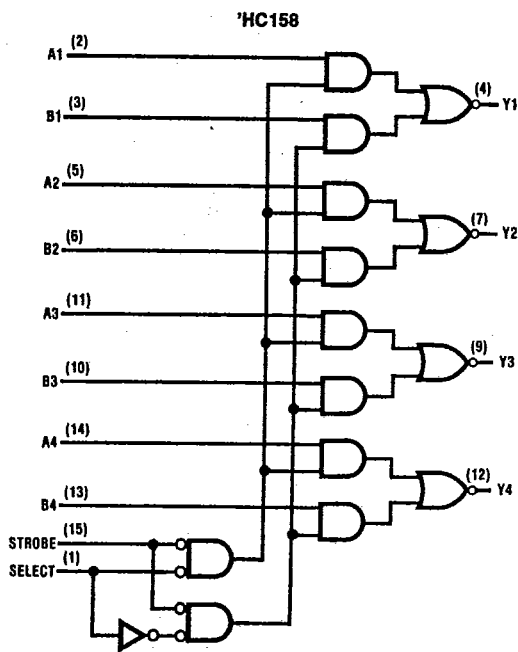
Logic Diagrams

T-67-21-51

MM54HC157/MM74HC157/MM54HC158/MM74HC158



TL/F/5314-3



TL/F/5314-4

3