

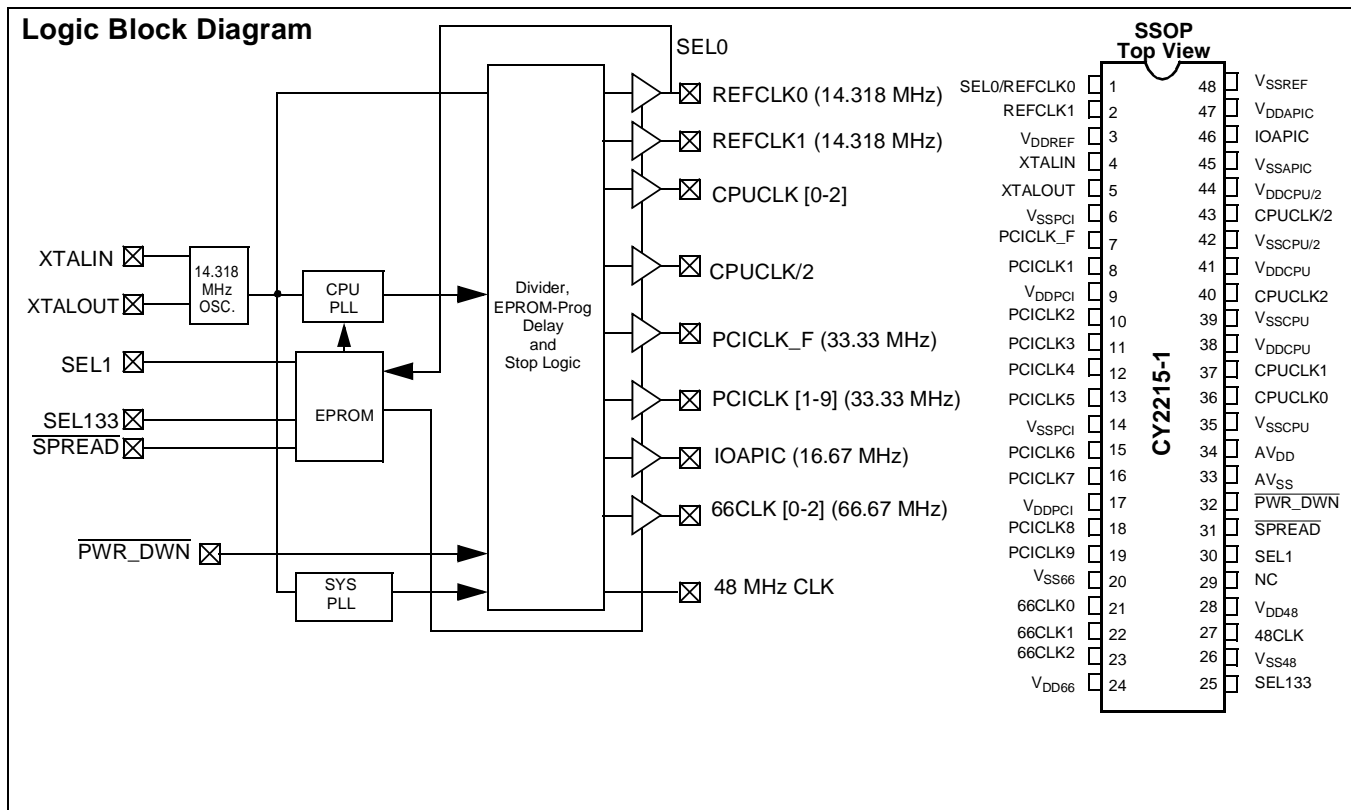


CYPRESS

CY2215

133-MHz Spread Spectrum Frequency Timing Generator

Features	Benefits
<ul style="list-style-type: none"> • Mixed 2.5V and 3.3V Operation 	Usable with Pentium® II, K6, and 6x86 Processors
<ul style="list-style-type: none"> • Multiple output clocks at different frequencies <ul style="list-style-type: none"> — Three CPU clocks, up to 133 MHz — Ten synchronous PCI clocks, 1 free-running — One CPU/2 clock, at one-half the CPU frequency — Three 66 MHz clocks — One synchronous IOAPIC clock, at 16.67 MHz — One 48 MHz clock — Two reference clocks at 14.318 MHz 	Single-chip main motherboard clock generator <ul style="list-style-type: none"> — Driven together, support 3 CPUs and a chipset — Support for 4 PCI slots and chipset — Drives up to two main memory clock generators, including DRCG — Support for multiple AGP slots — Support multiprocessing systems — Supports USB frequencies and I/O chip — Supports ISA slots and I/O chip
<ul style="list-style-type: none"> • Spread Spectrum clocking <ul style="list-style-type: none"> — 32.5 kHz modulation frequency at 133 MHz — 33.1 kHz modulation frequency at 100 MHz — EPROM programmable percentage of spreading. Default is -0.5%, which is recommended by Intel®. 	Enables reduction of EMI in some systems
<ul style="list-style-type: none"> • Power-down features 	Supports mobile systems
<ul style="list-style-type: none"> • Three Select inputs 	Supports up to eight CPU clock frequencies
<ul style="list-style-type: none"> • Low-skew and low-jitter outputs 	Meet tight system timing requirements at high frequency
<ul style="list-style-type: none"> • OE and Test Mode support 	Enables ATE and "bed of nails" testing
<ul style="list-style-type: none"> • 48-pin SSOP package 	Widely available, standard package enables lower cost



Intel and Pentium are registered trademarks of Intel Corporation.

Pin Summary

Name	Pins	Description
V _{SSREF}	48	3.3V Reference ground
V _{DDREF}	3	3.3V Reference voltage supply
V _{SSPCI}	6, 14	3.3V PCI ground
V _{DDPCI}	9, 17	3.3V PCI voltage supply
V _{SS66}	20	3.3V 66-MHz ground
V _{DD66}	24	3.3V 66-MHz voltage supply
V _{SS48}	26	3.3V 48-MHz ground
V _{DD48}	28	3.3V 48-MHz voltage supply
V _{SSCPU}	35, 39	2.5V CPU ground
V _{DDCPU}	38, 41	2.5V CPU voltage supply
V _{SSCPU/2}	42	2.5V CPU/2 ground
V _{DDCPU/2}	44	2.5V CPU/2 voltage supply
V _{SSAPIC}	45	2.5V IOAPIC ground
V _{DDAPIC}	47	2.5V IOAPIC voltage supply
AV _{DD}	34	Analog voltage supply to PLL and Core
AV _{SS}	33	Analog ground
XTALIN ^[1]	4	Reference crystal input
XTALOUT ^[1]	5	Reference crystal feedback
CPUCLK [0–2]	36, 37, 40	CPU clock outputs
PCICLK [1–9]	8, 10, 11, 12, 13, 15, 16, 18, 19	PCI clock outputs, synchronously running at 33.33 MHz
PCICLK_F	7	Free running PCI clock
CPUCLK/2	43	CPU/2 clock outputs, drive memory clock generator
66CLK [0-2]	21, 22, 23	66.67-MHz clock outputs
IOAPIC	46	IOAPIC clock output, running at 16.67 MHz
REFCLK [0–1]	1,2	Reference clock outputs, 14.318 MHz
48CLK	27	48-MHz clock output
PWR_DWN	32	Active LOW input, powers down part when asserted
SPREAD	31	Active LOW input, enables spread spectrum when asserted
SEL1	30	CPU frequency select input (See Function Table)
SEL0 ^[2]	1	CPU frequency select input (See Function Table). Internal 50K pull-up
SEL133	25	CPU frequency select input (See Function Table)
NC	29	No Connect pin, no internal connection

Notes:

1. For best accuracy, use a parallel-resonant crystal. C_{LOAD} = 18 pF. For crystals with different C_{LOAD}, please refer to the application note, "Crystal Oscillator Topics."
2. Pin 1, SEL0 Function, is only active at power-on.

Function Table

SEL133	SEL1	SEL0	CPUCLK (MHz)	CPUCLK/2 (MHz)	66CLK (MHz)	PCICLK (MHz)	48CLK (MHz)	REFCLK (MHz)	IOAPIC (MHz)
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0	1	0	100	50	66.67	33.33	OFF	14.318	16.67
0	1	1	100	50	66.67	33.33	48	14.318	16.67
1	0	0	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16
1	0	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A
1	1	0	133.33	66.67	66.67	33.33	OFF	14.318	16.67
1	1	1	133.33	66.67	66.67	33.33	48	14.318	16.67

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	100.0	TBD	TBD
CPUCLK	133.33	TBD	TBD
48CLK	48.0	48.008	167

Clock Enable Configuration

PWR_DWN	All Clocks	OSC.	VCOs
0	LOW	OFF	OFF
1	ON	ON	ON

Clock Driver Impedances

Buffer Name	V _{DD} Range	Buffer Type	Impedance		
			Minimum Ω	Typical Ω	Maximum Ω
CPU, CPU/2, IOAPIC	2.375–2.625	Type 1	13.5	29	45
48CLK, REF	3.135–3.465	Type 3	20	40	60
PCI, 66CLK	3.135–3.465	Type 5	12	30	55

Note:

3. TCLK is a test clock driven in on the XTALIN input in test mode.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5 to +7.0V
 Input Voltage -0.5V to $V_{DD}+0.5$

Storage Temperature (Non-Condensing) ... -65°C to +150°C
 Max. Soldering Temperature (10 sec) +260°C
 Junction Temperature +150°C
 Package Power Dissipation 1W
 Static Discharge Voltage
 (per MIL-STD-883, Method 3015) >2000V

Operating Conditions Over which Electrical Parameters are Guaranteed

Parameter	Description	Min.	Max.	Unit
V_{DDREF} , V_{DDPCI} , AV_{DD} , V_{DD66} , $V_{DD4848CLK}$	3.3V Supply Voltages	3.135	3.465	V
V_{DDCPU} , $V_{DDCPU/2}$	CPU and CPU/2 Supply Voltage	2.375	2.625	V
V_{DDAPIC}	IOAPIC Supply Voltage	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK, CPUCLK/2, 48CLK, REF PCICLK, 66CLK, IOAPIC		20 30	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit	
V_{IH}	High-level Input Voltage	Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$	2.0		V	
V_{IL}	Low-level Input Voltage	Except Crystal Pads		0.8	V	
I_{IH}	Input High Current	$0 \leq V_{IN} \leq V_{DD}$		10	μA	
I_{IL}	Input Low Current	$0 \leq V_{IN} \leq V_{DD}$		10	μA	
I_{OH}	High-level Output Current	CPU, CPU/2	$V_{OH} = 2.0V$	-16	-60	mA
		APIC	$V_{OH} = 2.0V$	-20	-72	
		USB, REF	$V_{OH} = 2.4V$	-15	-51	
		AGP, PCI	$V_{OH} = 2.4V$	-30	-100	
I_{OL}	Low-level Output Current	CPU, CPU/2	$V_{OL} = 0.4V$	19	49	mA
		APIC	$V_{OL} = 0.4V$	25	58	
		USB, REF	$V_{OL} = 0.4V$	10	24	
		AGP, PCI	$V_{OL} = 0.4V$	20	49	
I_{OZ}	Output Leakage Current	Three-state, excluding REF0		10	μA	
I_{OZ}	Output Leakage Current	Three-state, REF0		150	pA	
I_{DD2}	2.5V Power Supply Current	$AV_{DD}/V_{DD33} = 3.465V$, $V_{DD25} = 2.625V$, $F_{CPU} = 133$ MHz		90	mA	
I_{DD3}	3.3V Power Supply Current	$AV_{DD}/V_{DD33} = 3.465V$, $V_{DD25} = 2.625V$, $F_{CPU} = 133$ MHz		160	mA	
I_{DDPD2}	2.5V Shutdown Current	$AV_{DD}/V_{DD33} = 3.465V$, $V_{DD25} = 2.625V$		100	μA	
I_{DDPD3}	3.3V Shutdown Current	$AV_{DD}/V_{DDQ3} = 3.465V$, $V_{DD25} = 2.625V$		200	μA	

CY2215 Switching Characteristics^[4] Over the Operating Range

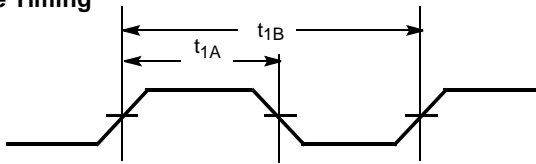
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t ₁	All	Output Duty Cycle ^[5]	t _{1A} /t _{1B}	45	55	%
t ₂	CPU, CPU/2, IOAPIC	Rising Edge Rate	Between 0.4V and 2.0V	1.0	4.0	V/ns
t ₂	48CLK, REF	Rising Edge Rate	Between 0.4V and 2.4V	0.5	2.0	V/ns
t ₂	PCI, 66CLK	Rising Edge Rate	Between 0.4V and 2.4V	1.0	4.0	V/ns
t ₃	CPU, CPU/2, IOAPIC	Falling Edge Rate	Between 2.0V and 0.4V	1.0	4.0	V/ns
t ₃	48CLK, REF	Falling Edge Rate	Between 2.4V and 0.4V	0.5	2.0	V/ns
t ₃	PCI, 66CLK	Falling Edge Rate	Between 2.4V and 0.4V	1.0	4.0	V/ns
t ₆	CPU	CPU-CPU Skew	Measured at 1.25V		175	ps
t ₉	66CLK	66CLK-66CLK Skew	Measured at 1.5V		250	ps
t ₁₀	PCI	PCI-PCI Skew	Measured at 1.5V		500	ps
t ₁₁	CPU, 66CLK	CPU-66CLK Clock Skew	CPU leads. Measured at 1.25V for 2.5V clocks and 1.5V for 3.3V clocks	0	1.5	ns
t ₁₂	66CLK, PCI	66CLK-PCI Clock Skew	66CLK leads. Measured at 1.5V	1.5	4.0	ns
t ₁₃	CPU, IOAPIC	IOAPIC-CPU Clock Skew	APIC leads. Measured at 1.25V	1.5	4.0	ns
	CPU	Cycle-Cycle Clock Jitter	With all outputs running		250	ps
	CPU	Cycle-Cycle Clock Jitter	With the 48CLK output turned off		200	ps
	CPU/2	Cycle-Cycle Clock Jitter			250	ps
	IOAPIC	Cycle-Cycle Clock Jitter			500	ps
	48CLK	Cycle-Cycle Clock Jitter			500	ps
	66CLK	Cycle-Cycle Clock Jitter			500	ps
	REF	Cycle-Cycle Clock Jitter			1000	ps
	CPU, PCI	Settle Time	CPU and PCI clock stabilization from power-up		3	ms

Notes:

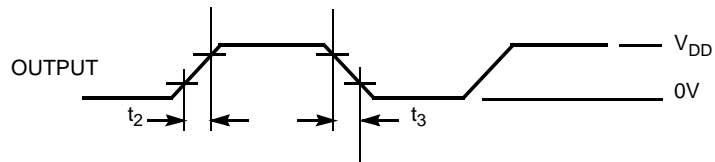
- All parameters specified with fully loaded outputs with the exception of PCI outputs where the sum of all loads on the PCI outputs are not to exceed 240 pF and AGP outputs should not exceed 75 pF total lump load.
- Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.

Switching Waveforms

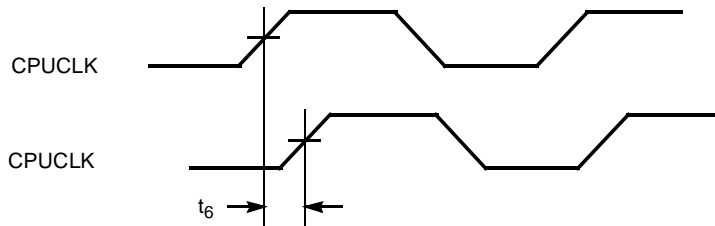
Duty Cycle Timing



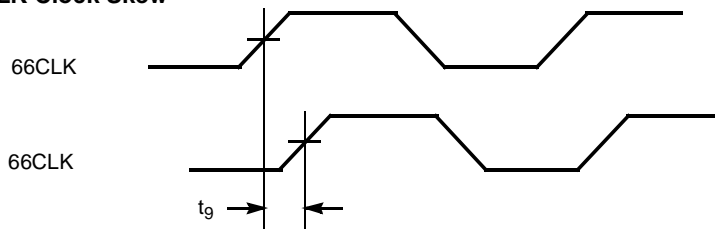
All Outputs Rise/Fall Time



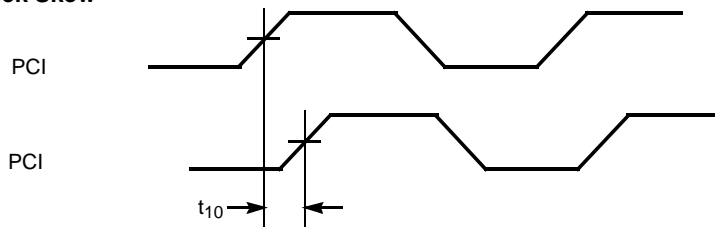
CPU-CPU Clock Skew

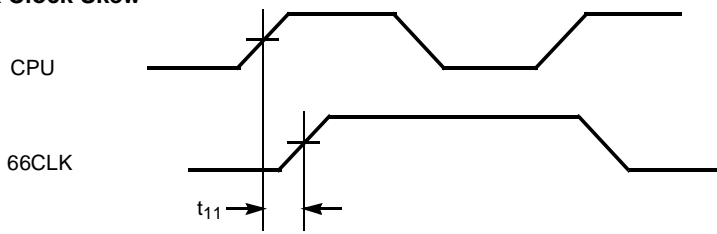
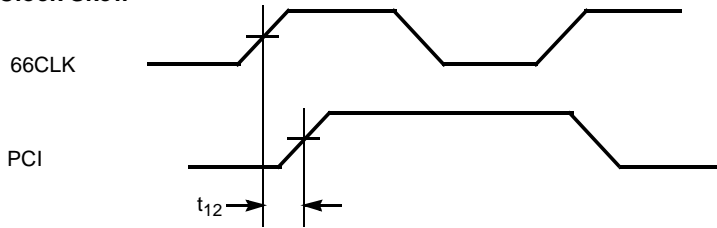
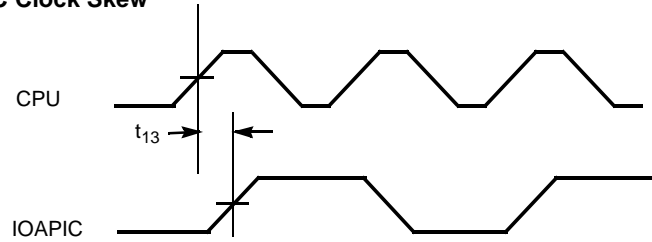
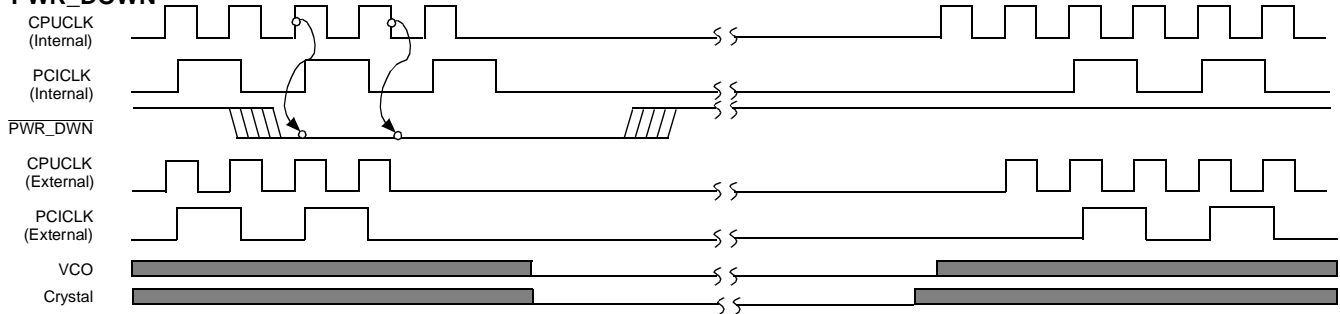


66CLK-66CLK Clock Skew



PCI-PCI Clock Skew

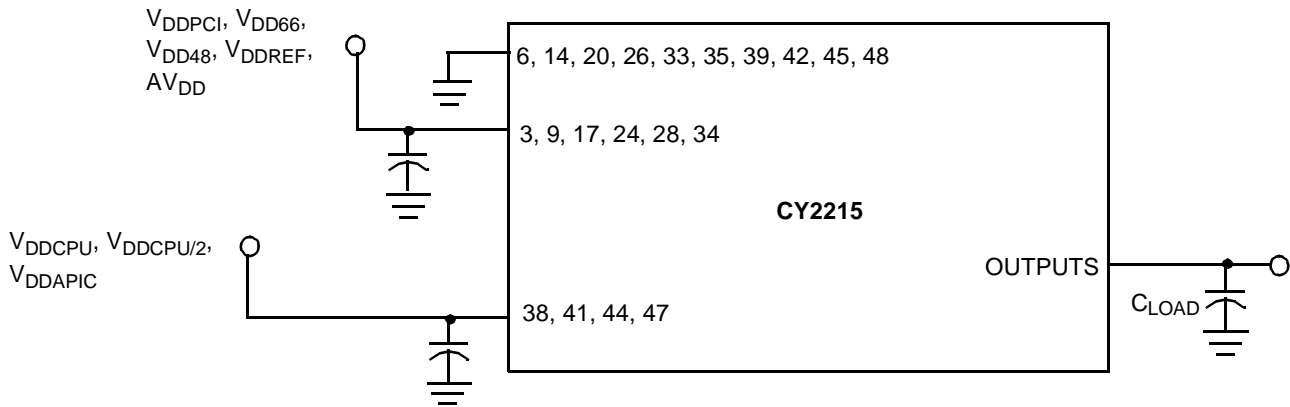


Switching Waveforms (continued)
CPU-66CLK Clock Skew

66CLK-PCI Clock Skew

CPU-IOAPIC Clock Skew

PWR_DOWN


Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Note:

6. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.

Test Circuit


Note: Each supply pin must have an individual decoupling capacitor.

Note: All Capacitors must be placed as close to the pins as is physically possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2215PVC-1	O48	48-Pin SSOP	Commercial

Document #: 38-00772-A

Package Diagram
48-Lead Shrunken Small Outline Package O48
