NEW PRODUCT

MITSUBISHI ASTTLs

M74AS74P

T-46-07-05

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74AS74P is a semiconductor integrated circuit consisting of two D-type positive-edge-triggered flip-flop circuits. Each of the circuits has independent inputs such as data D, clock T, direct set $\overline{S_D}$ and direct reset $\overline{R_D}$.

FEATURES

- Positive-edge-triggering
- Independent inputs and outputs for each flip-flop
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a=−20~+75℃)

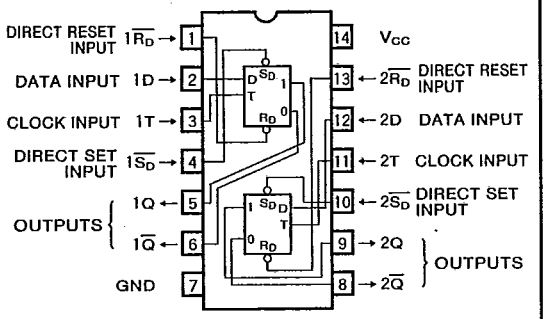
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

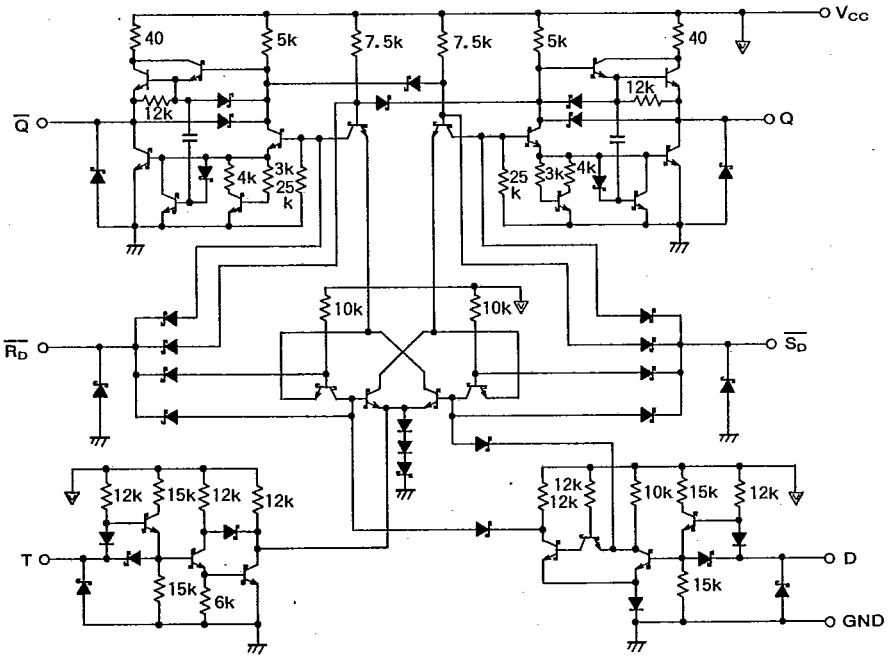
When T changes from low-level to high-level, the D signal just before the change appears at Q and $\overline{Q}$ outputs in accordance with the function table. Use of $\overline{S_D}$ and $\overline{R_D}$ allows direct R-S flip-flop operation. When $\overline{S_D}$ and $\overline{R_D}$ are low-level, Q and $\overline{Q}$ are high-level. But if $\overline{S_D}$ and $\overline{R_D}$ become high simultaneously from this condition, the state of Q and $\overline{Q}$ cannot be predicted. When used as a D-type flip-flop, $\overline{S_D}$ and $\overline{R_D}$ should be maintained in high-level.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH FLIP-FLOP)



UNIT : Ω

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

T-46-07-05

FUNCTION TABLE (Note 1)

Inputs				Outputs	
$\overline{S_D}$	$\overline{R_D}$	T	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	L	X	Q^0	$\overline{Q}^0$
H	H	↑	H	H	L
H	H	↑	L	L	H

Note 1 ↑ : Transition from low to high level (positive edge trigger)

Q^0 : Level of Q before the indicated steady-state input conditions were established.

$\overline{Q}^0$: Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

X : Irrelevant

* : If $\overline{S_D}$ and $\overline{R_D}$ simultaneously become high-level from this condition then the state of Q and $\overline{Q}$ cannot be predicted.

ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+7	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−2	mA
I_{OL}	Low-level output current	0		20	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

T-46-07-05

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ*	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5V∼5.5V, I_{OH}=−2mA	V_{CC}−2			V
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=20mA			0.5	V
I_I	Input current at maximum voltage		V_{CC}=5.5V, V_I=7V			0.1	mA
I_{IH}	High-level input current	D, T	V_{CC}=5.5V, V_I=2.7V			20	μA
		$\overline{S_D}$, $\overline{R_D}$				40	
I_{IL}	Low-level input current	D, T	V_{CC}=5.5V, V_I=0.4V			−0.5	mA
		$\overline{S_D}$, $\overline{R_D}$				−1.8	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V	−30		−112	mA
I_{CC}	Supply current		V_{CC}=5.5V (Note 2)		10.5	16	mA

*: All typical values are at V_{CC}=5V, T_a=25℃.

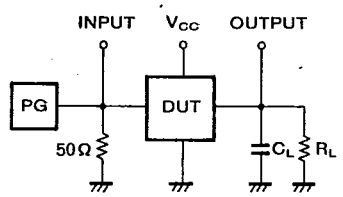
Note 2 : The supply current is measured alternately at D=T=$\overline{S_D}$=0V, $\overline{R_D}$=4.5V (Q=high-level) and D=T=$\overline{R_D}$=0V, $\overline{S_D}$=4.5V ($\overline{Q}$=high-level).

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits: V_{CC}=4.5∼5.5V (Note 3), C_L=50pF, R_L=500Ω						Unit
				T_a=0∼70℃			T_a=−20∼+75℃			
		Inputs	Outputs	Min	Typ*	Max	Min	Typ*	Max	
f_{max}	Maximum clock frequency	T	Q, $\overline{Q}$	105			95			MHz
t_{PLH}	Propagation time	$\overline{S_D}$, $\overline{R_D}$	Q, $\overline{Q}$	3		7.5	3		8.5	ns
t_{PHL}				3.5		10.5	3.5		11.5	
t_{PLH}		T	Q, $\overline{Q}$	3.5		8	3.5		9	ns
t_{PHL}				4.5		9	4.5		10	

*: All typical values are at V_{CC}=5V, T_a=25℃.

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR≦1MHz
t_r=2ns, t_f=2ns
V_{IH}=3.5V, V_{IL}=0.3V
duty cycle=50%
Z_O=50Ω

(2) C_L includes probe and jig capacitance.

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

T-46-07-05

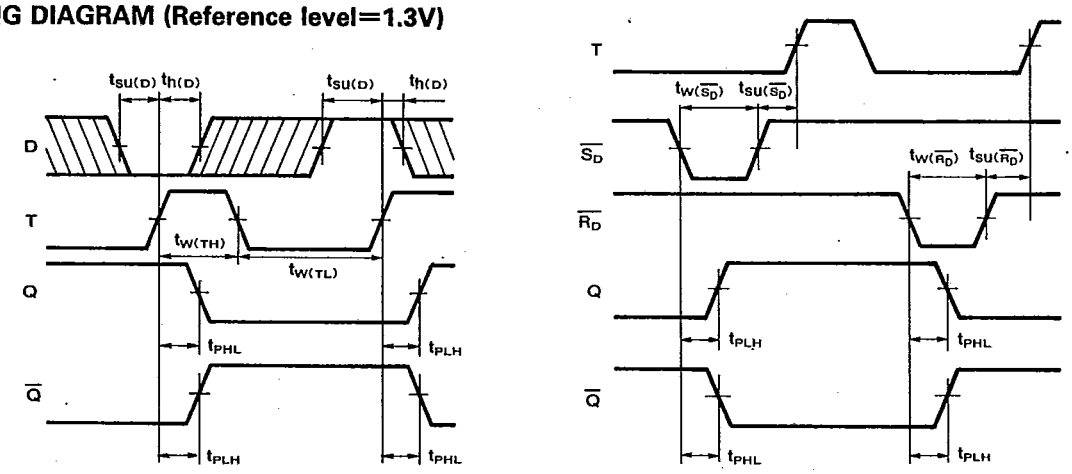
TIMING REQUIREMENTS (V_{CC}=4.5V~5.5V, C_L=50pF, R_L=500Ω)

Symbol	Parameter		Limits						Unit
			T_a=0~70℃			T_a=−20~+75℃			
			Min	Typ*	Max	Min	Typ*	Max	
$t_{w(TH)}$	Pulse width	T "H"	4			4			ns
$t_{w(TL)}$		T "L"	5.5			5.5			
$t_{w(\overline{S_D})}$		$\overline{S_D}$ "L"	4			4			
$t_{w(\overline{R_D})}$		$\overline{R_D}$ "L"	4			4			
$t_{su(D)}$	Setup time before T↑	D	4.5			4.5			ns
$t_{su(\overline{S_D})}$		$\overline{S_D}$ "H" (inactive)	2			2			
$t_{su(\overline{R_D})}$		$\overline{R_D}$ "H" (inactive)	2			2			
$t_{h(D)}$	Hold time after T↑	D	0			0			ns

*: All typical values are at V_{CC}=5V, T_a=25℃.

↑: Transition from low to high level (positive edge trigger)

TIMING DIAGRAM (Reference level=1.3V)

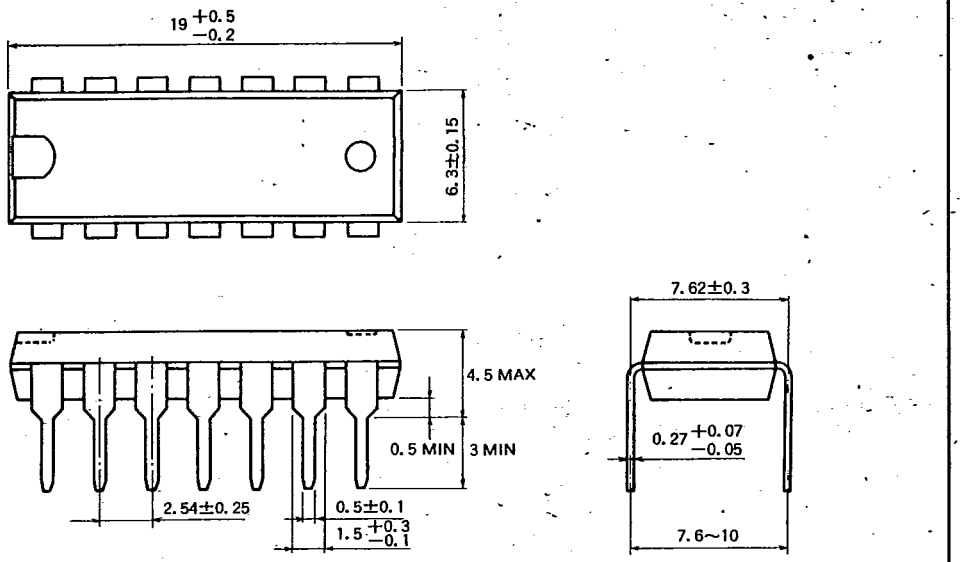


Note 4: The shaded areas indicate the period when the input is permitted to change for predictable output performance.

PACKAGE OUTLINES

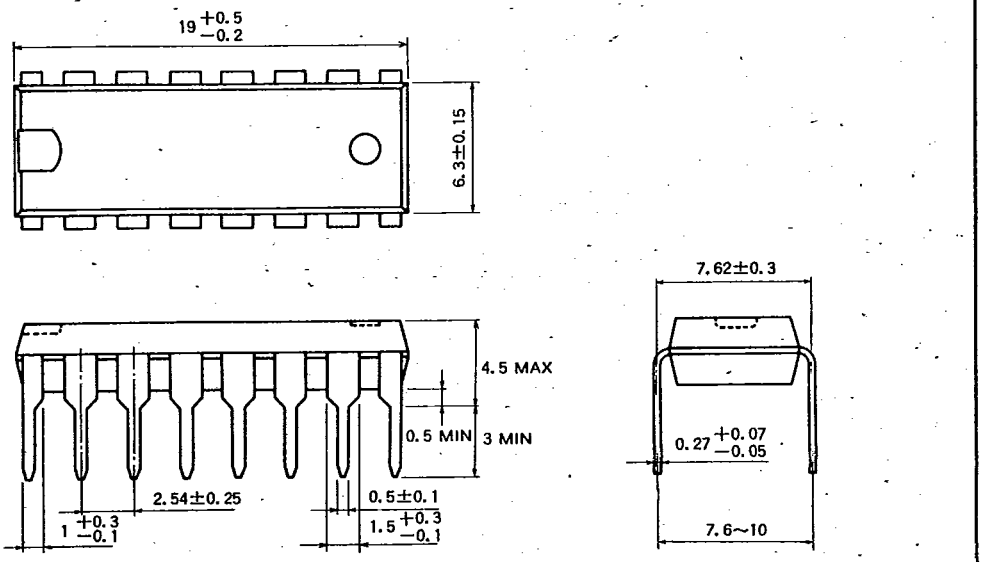
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



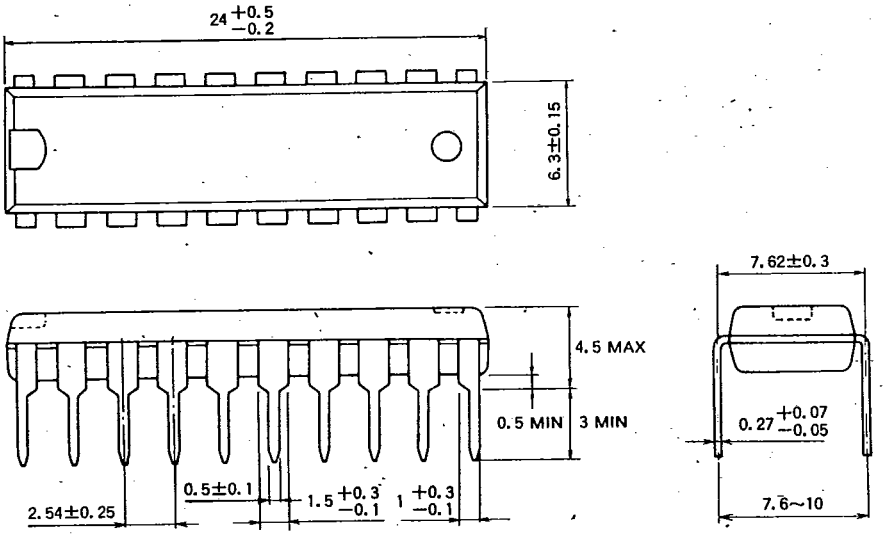
TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm