8-Bit Buffers

SN54/74LS210 SN54/74S210
SN54/74LS240 SN54/74S240
SN54/74LS241 SN54/74S241
SN54/74LS244 SN54/74S244

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '210 and '241 types combine multiplexer and driver functions

Description

These 8-bit buffers provide high speed and high current interface capability for bus organized digital systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} on the low-power Schottky buffers and 0.4 mA I_{IL} on the Schottky buffers.

The '240 and '244 provide inverting and noninverting outputs respectively, with assertive low enables. The '210 and '241 also provide inverting and noninverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceive or multiplexer operation.

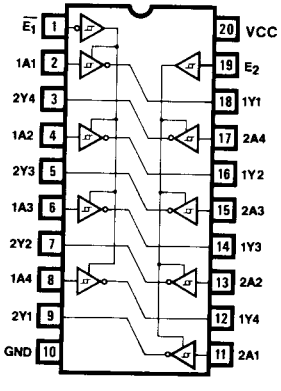
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Ordering Information

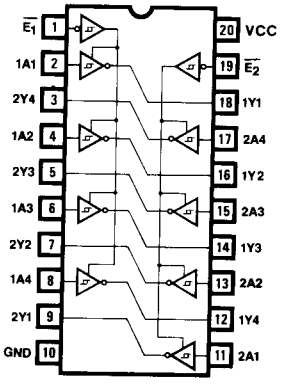
PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54LS210	J,L,W	Mil	High-Low	Invert	LS
SN74LS210	N,J	Com			
SN54LS240	J,L,W	Mil	Low		
SN74LS240	N,J	Com			
SN54LS241	J,L,W	Mil	High-Low	Non-Invert	
SN74LS241	N,J	Com			
SN54LS244	J,L,W	Mil	Low		
SN74LS244	N,J	Com			
SN54S210	J,L,W	Mil	High-Low	Invert	S
SN74S210	N,J	Com			
SN54S240	J,L,W	Mil	Low		
SN74S240	N,J	Com			
SN54S241	J,L,W	Mil	High-Low	Non-Invert	
SN74S241	N,J	Com			
SN54S244	J,L,W	Mil	Low		
SN74S244	N,J	Com			

Logic Symbols

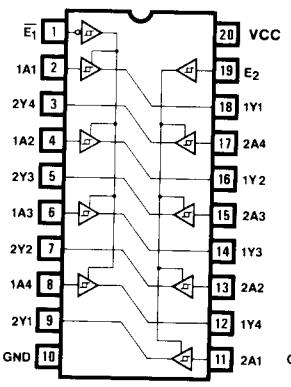
'210 8-Bit Buffer



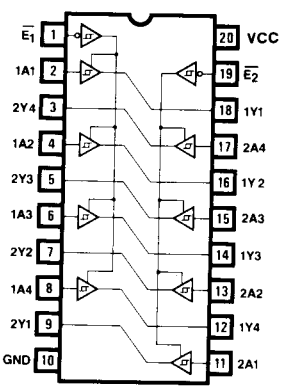
'240 8-Bit Buffer



'241 8-Bit Buffer



'244 8-Bit Buffer



11

SKINNYDIP® is a registered trademark of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Function Tables

'210

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	H	Z
L	L	H	X	L	Z
L	H	L	L	H	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	H	L	L
H	H	X	L	Z	H
H	H	X	H	Z	L
H	L	X	X	Z	Z

'240

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

'241

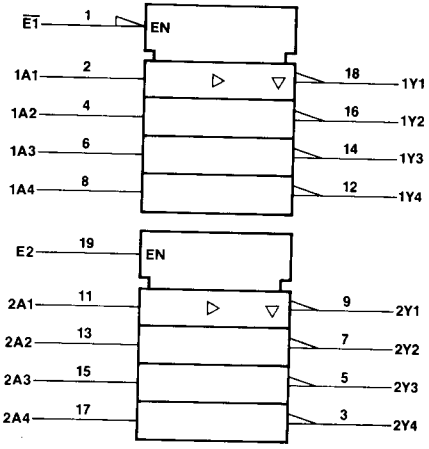
$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L	L	H	X	H	Z
L	H	L	L	L	L
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	H
H	H	X	L	Z	L
H	H	X	H	Z	H
H	L	X	X	Z	Z

'244

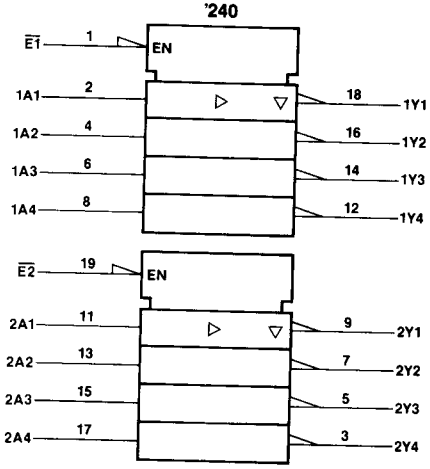
$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

IEEE Symbols

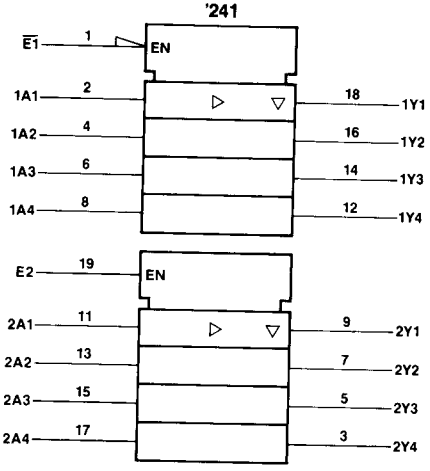
'210



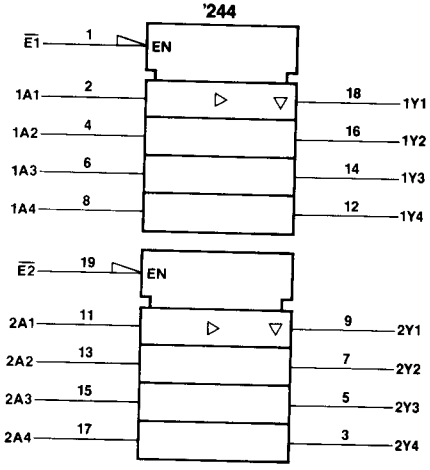
'240



'241



'244



11

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 7 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis ($V_{T_+} - V_{T_-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			−0.2			−0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current		V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA			0.4			0.4	V
				I_{OL} = 24mA						0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN,	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
			V_{IL} = 0.5V, V_{IH} = 2V	I_{OH} = −12mA	2						
				I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−20			−20	μA
I_{OZH}				V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	LS210, LS240		17	27		17	27	mA
				LS241, LS244		17	27		17	27	
		Outputs Low		LS210, LS240		26	44		26	44	
				LS241, LS244		27	46		27	46	
		Outputs Disabled		LS210, LS240		29	50		29	50	
				LS241, LS244		32	54		32	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	LS210, LS240 MIN	LS210, LS240 TYP	LS210, LS240 MAX	LS241, LS244 MIN	LS241, LS244 TYP	LS241, LS244 MAX	UNIT
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}	Output Enable delay			20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				10	18		10	18	ns

Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current	Any A	V_{CC} = MAX	V_I = 0.5V			−0.4			−0.4	mA
		Any E					−2			−2	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 48mA			0.55				V
				I_{OL} = 64mA						0.55	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −1mA				2.7			V
				I_{OH} = −3mA	2.4	3.4		2.4	3.4		
				I_{OH} = −12mA	2						
				I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}				V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current †		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	S210,S240		80	123		80	135	mA
				S241,S244		95	147		95	160	
		Outputs Low		S210,S240		100	145		100	150	
				S241,S244		120	170		120	180	
		Outputs Disabled		S210,S240		100	145		100	150	
				S241,S244		120	170		120	180	

† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

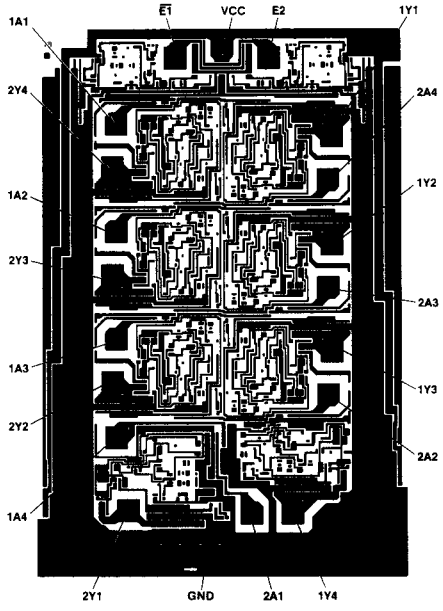
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S210, S240			S241, S244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 50pF R_L = 90Ω		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	ns
t_{PZL}	Output Enable delay			10	15		10	15	ns
t_{PZH}				6.5	10 *		8	12	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 90Ω		10	15		10	15	ns
t_{PHZ}				6	9		6	9	ns

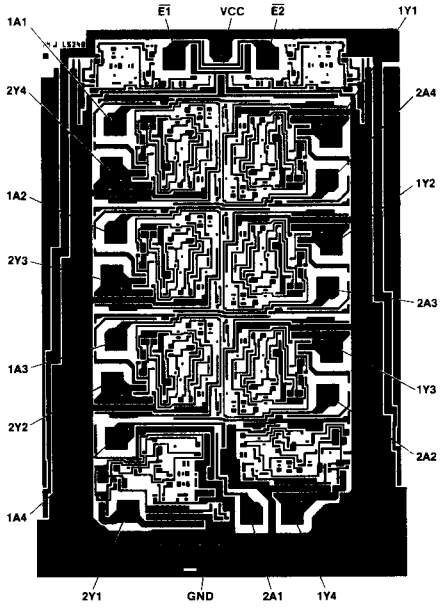
* For the S210 add 2 ns for the E_2 (Pin 19) enable

Die Configurations

'LS210

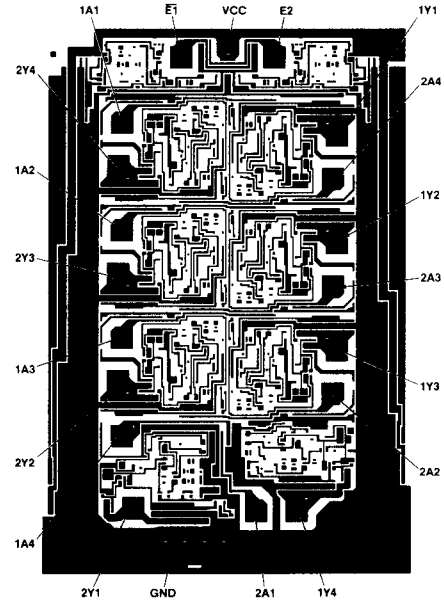


'LS240

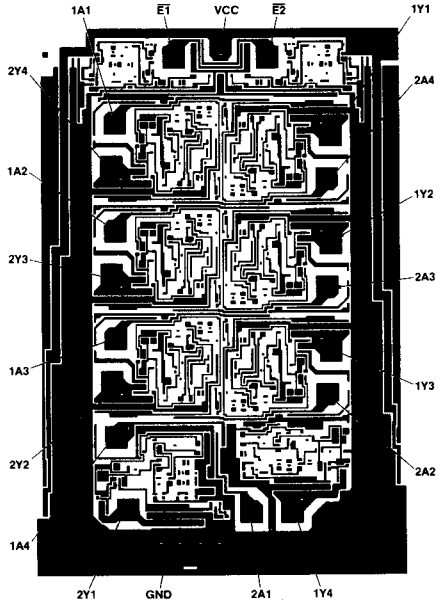


Die Size: 85x146 mil^2

'LS241

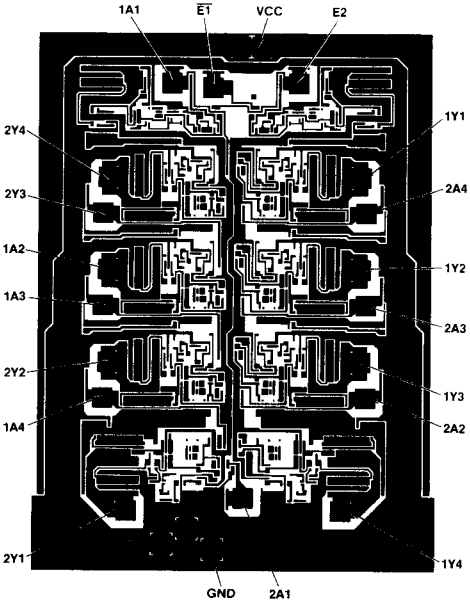


'LS244

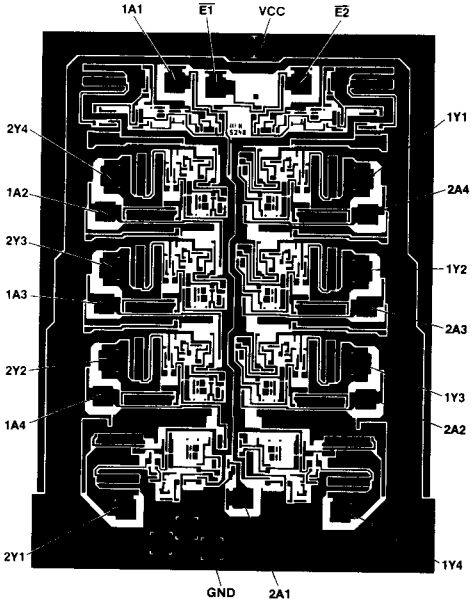


Die Configurations

'S210

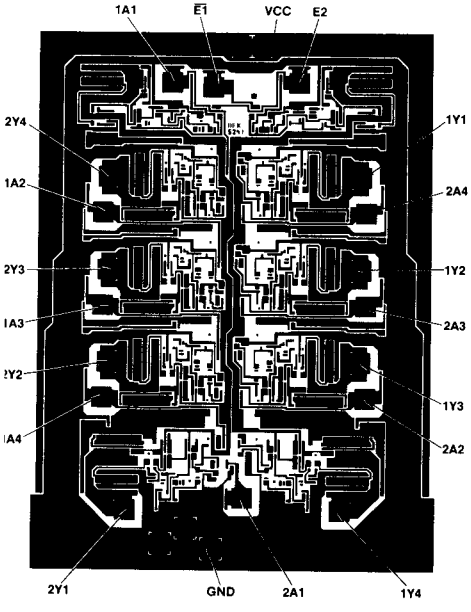


'S240

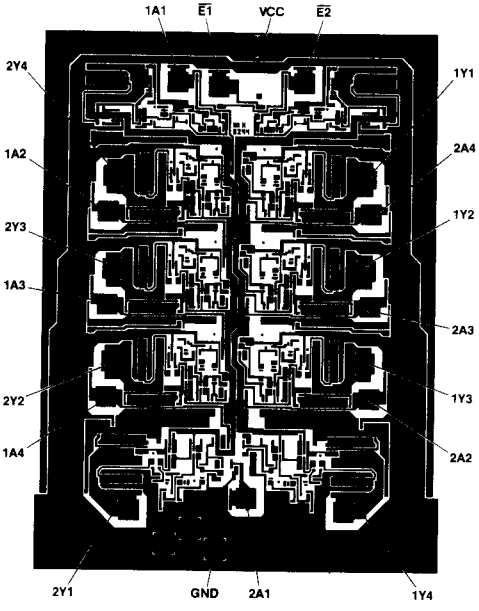


Die Size: 68x100 mil^2

'S241

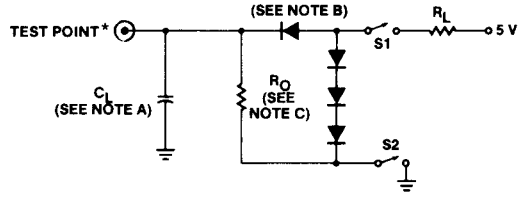


'S244



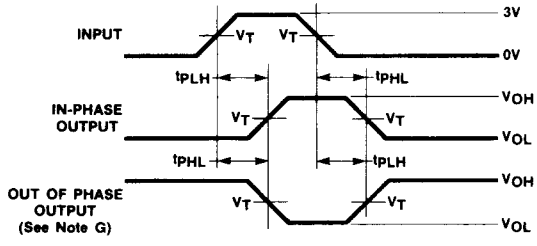
11

Test Load

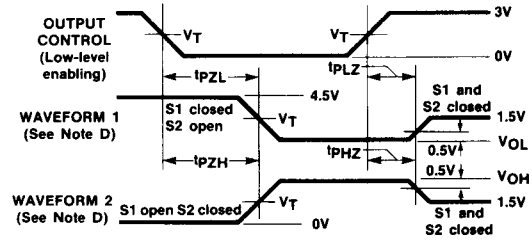


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay



Enable and Disable

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
For Series 54/74LS, R_O = 5K, V_T = 1.3 V.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.
For Series 54/74LS and PALs, $t_R \leq 15$ ns. $t_F \leq 6$ ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.