

Document Title

128Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Design target	September 9, 1998	Preliminary
1.0	Finalize - Change Icc1: 3 to 4mA	April 13, 1998	Final
2.0	Revised - Add reverse package type from TSOP package.	August 1, 2000	Final
2.01	Errata correction - Removed TTL Compatible from Features	October 24, 2001	Final
3.0	Revised - Added K6T1008V2E-YB55, K6T1008V2E-YF55 product.	November 6, 2001	Final

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128Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 128Kx8
- Power Supply Voltage
K6T1008V2E Family: 3.0V ~ 3.6V
K6T1008U2E Family: 2.7V ~ 3.3V
- Low Data Retention Voltage: 2V(Min)
- Three State Outputs
- Package Type: 32-SOP-525,
32-TSOP1-0820F/R, 32-TSOP1-0813.4F/R

GENERAL DESCRIPTION

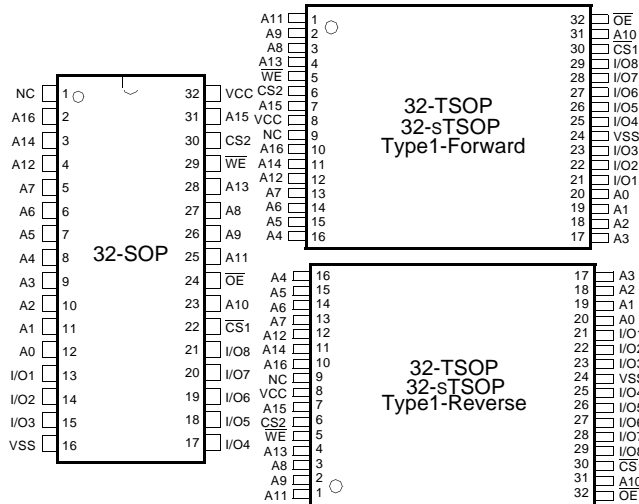
The K6T1008V2E and K6T1008U2E families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
K6T1008V2E-B	Commercial(0~70°C)	3.0~3.6V	55 ¹ /70 ¹ /100ns	10µA	30mA	32-SOP-525 32-TSOP1-0820F/R 32-TSOP1-0813.4F/R
K6T1008U2E-B		2.7~3.3V	70 ¹ /100ns			
K6T1008V2E-F	Industrial(-40~85°C)	3.0~3.6V	55 ¹ /70 ¹ /100ns			
K6T1008U2E-F		2.7~3.3V	70 ¹ /100ns			

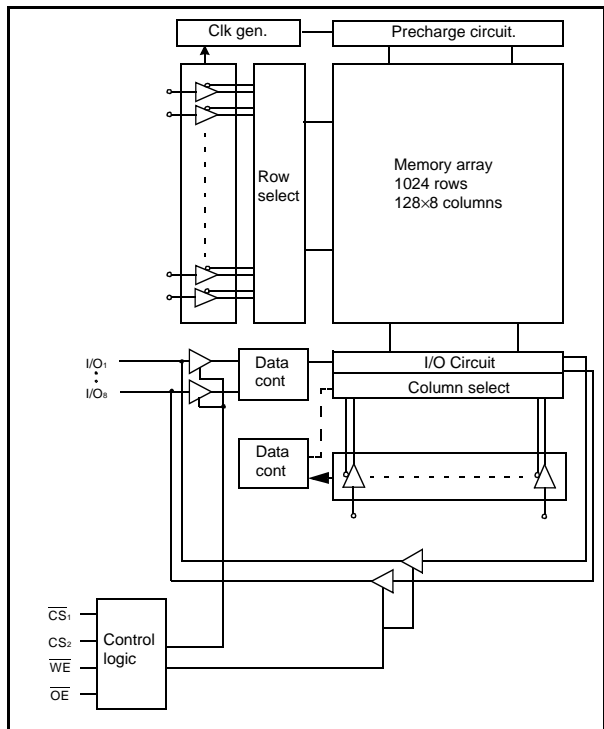
1. The parameters are tested with 30pF test load.

PIN DESCRIPTION



Name	Function
A0~A16	Address Inputs
\overline{WE}	Write Enable Input
$\overline{CS1}, \overline{CS2}$	Chip Select Input
\overline{OE}	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T1008V2E-GB70	32-SOP, 70ns, 3.3V	K6T1008V2E-GF70	32-SOP, 70ns, 3.3V
K6T1008V2E-GB10	32-SOP, 100ns, 3.3V	K6T1008V2E-GF10	32-SOP, 100ns, 3.3V
K6T1008V2E-TB70	32-TSOP-F, 70ns, 3.3V	K6T1008V2E-TF70	32-TSOP-F, 70ns, 3.3V
K6T1008V2E-TB10	32-TSOP-F, 100ns, 3.3V	K6T1008V2E-TF10	32-TSOP-F, 100ns, 3.3V
K6T1008V2E-RB70	32-TSOP-R, 70ns, 3.3V	K6T1008V2E-RF70	32-TSOP-R, 70ns, 3.3V
K6T1008V2E-RB10	32-TSOP-R, 100ns, 3.3V	K6T1008V2E-RF10	32-TSOP-R, 100ns, 3.3V
K6T1008V2E-YB55	32-sTSOP-F, 55ns, 3.3V	K6T1008V2E-YF55	32-sTSOP-F, 55ns, 3.3V
K6T1008V2E-YB70	32-sTSOP-F, 70ns, 3.3V	K6T1008V2E-YF70	32-sTSOP-F, 70ns, 3.3V
K6T1008V2E-YB10	32-sTSOP-F, 100ns, 3.3V	K6T1008V2E-YF10	32-sTSOP-F, 100ns, 3.3V
K6T1008V2E-NB70	32-sTSOP-R, 70ns, 3.3V	K6T1008V2E-NF70	32-sTSOP-R, 70ns, 3.3V
K6T1008V2E-NB10	32-sTSOP-R, 100ns, 3.3V	K6T1008V2E-NF10	32-sTSOP-R, 100ns, 3.3V
K6T1008U2E-GB70	32-SOP, 70ns, 3.0V	K6T1008U2E-GF70	32-SOP, 70ns, 3.0V
K6T1008U2E-GB10	32-SOP, 100ns, 3.0V	K6T1008U2E-GF10	32-SOP, 100ns, 3.0V
K6T1008U2E-TB70	32-TSOP-F, 70ns, 3.0V	K6T1008U2E-TF70	32-TSOP-F, 70ns, 3.0V
K6T1008U2E-TB10	32-TSOP-F, 100ns, 3.0V	K6T1008U2E-TF10	32-TSOP-F, 100ns, 3.0V
K6T1008U2E-RB70	32-TSOP-R, 70ns, 3.0V	K6T1008U2E-RF70	32-TSOP-R, 70ns, 3.0V
K6T1008U2E-RB10	32-TSOP-R, 100ns, 3.0V	K6T1008U2E-RF10	32-TSOP-R, 100ns, 3.0V
K6T1008U2E-YB70	32-sTSOP-F, 70ns, 3.0V	K6T1008U2E-YF70	32-sTSOP-F, 70ns, 3.0V
K6T1008U2E-YB10	32-sTSOP-F, 100ns, 3.0V	K6T1008U2E-YF10	32-sTSOP-F, 100ns, 3.0V
K6T1008U2E-NB70	32-sTSOP-R, 70ns, 3.0V	K6T1008U2E-NF70	32-sTSOP-R, 70ns, 3.0V
K6T1008U2E-NB10	32-sTSOP-R, 100ns, 3.0V	K6T1008U2E-NF10	32-sTSOP-R, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6T1008V2E-B, K6T1008U2E-B
		-40 to 85	°C	K6T1008V2E-F, K6T1008U2E-F

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6T1008V2E Family K6T1008U2E Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	K6T1008V2E, K6T1008U2E Family	2.2	-	V _{CC} +0.3	V
Input low voltage	V _{IL}	K6T1008V2E, K6T1008U2E Family	-0.3 ³⁾	-	0.6	V

Note:

- Commercial Product: T_A=0 to 70°C, otherwise specified
Industrial Product: T_A=-40 to 85°C, otherwise specified
- Overshoot: V_{CC}+2.0V in case of pulse width≤30ns
- Undershoot: -2.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

- Capacitance is sampled, not 100% tested

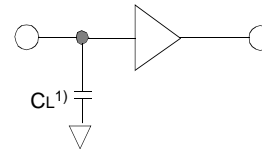
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, V _{IN} =V _{IH} or V _{IL} , Read	-	-	4	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS}_1\leq 0.2V$, $CS_2\geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	4	mA
	I _{CC2}	Cycle time=70ns, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, V _{IN} =V _{IH} or V _{IL}	-	25	30	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, $CS_2=V_{IL}$, Other inputs = V _{IH} or V _{IL}	-	-	0.3	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS}_1\geq V_{CC}-0.2V$, $CS_2\geq V_{CC}-0.2V$ or $CS_2\leq 0.2V$, Other inputs=0~V _{CC}	-	0.2	10	μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
 Input rising and falling time: 5ns
 Input and output reference voltage: 1.5V
 Output load(see right): $C_L=100\text{pF}+1\text{TTL}$
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS (K6T1008V2E Family: $V_{CC}=3.0\sim 3.6\text{V}$, K6T1008U2E Family: $V_{CC}=2.7\sim 3.3\text{V}$ Commercial Product: $T_A=0$ to 70°C , Industrial Product: $T_A=-40$ to 85°C)

Parameter List	Symbol	Speed Bins						Units	
		55ns		70ns		100ns			
		Min	Max	Min	Max	Min	Max		
Read	Read cycle time	t _{RC}	55	-	70	-	100	-	ns
	Address access time	t _{AA}	-	55	-	70	-	100	ns
	Chip select to output	t _{CO1} , t _{CO2}	-	55	-	70	-	100	ns
	Output enable to valid output	t _{OE}	-	25	-	35	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	25	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	25	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	10	-	15	-	ns
Write	Write cycle time	t _{WC}	55	-	70	-	100	-	ns
	Chip select to end of write	t _{CW}	45	-	60	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	80	-	ns
	Write pulse width	t _{WP}	40	-	55	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	25	0	30	ns
	Data to write time overlap	t _{DW}	20	-	30	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	5	-	ns

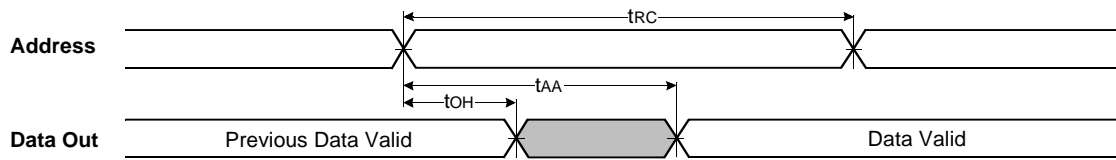
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}, \overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	-	0.2	10	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

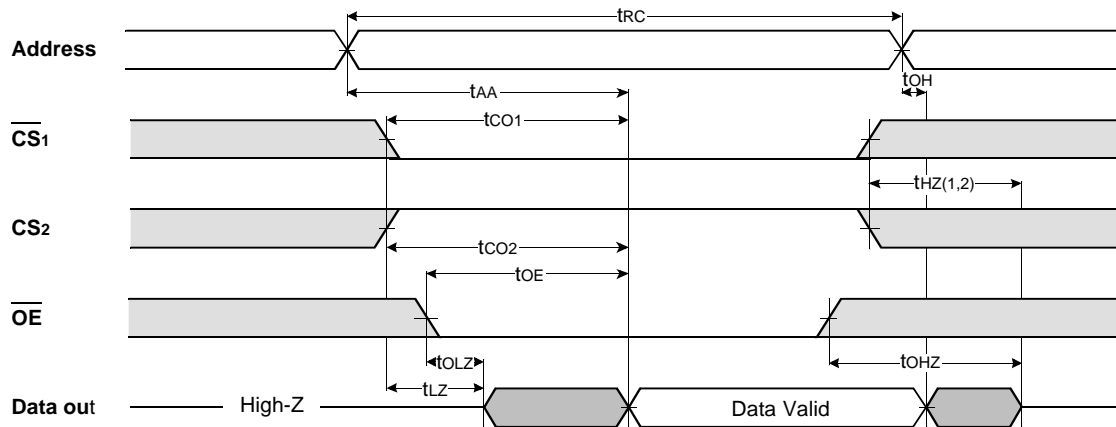
1. $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$, $\overline{CS}_2 \geq V_{CC}-0.2\text{V}$ (\overline{CS}_1 controlled) or $\overline{CS}_2 \leq 0.2\text{V}$ (\overline{CS}_2 controlled)

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



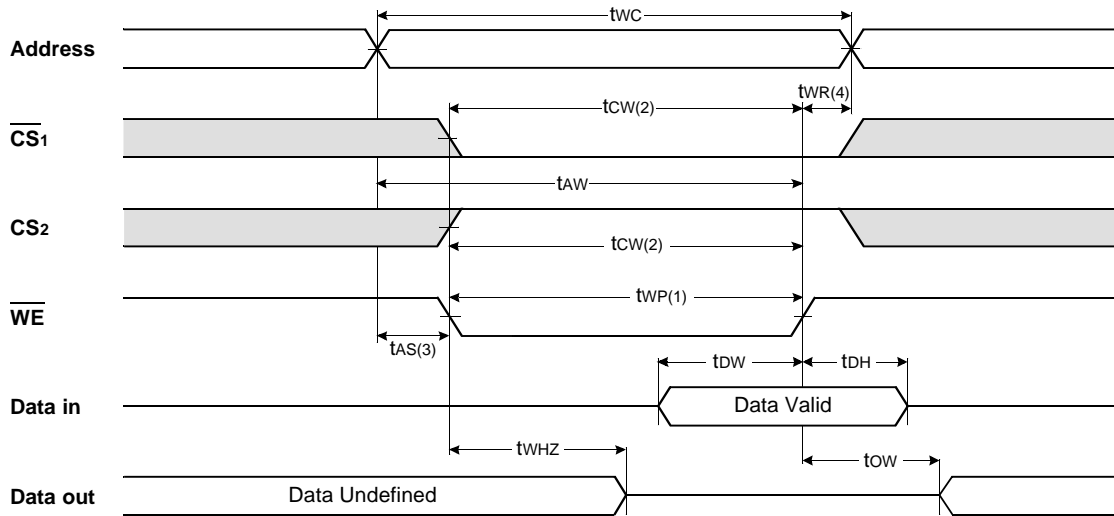
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



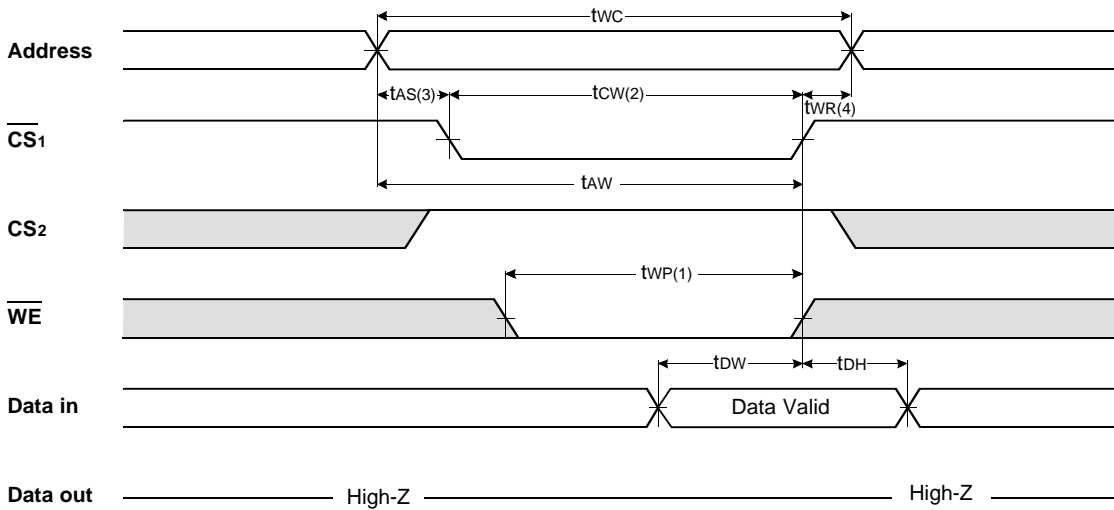
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

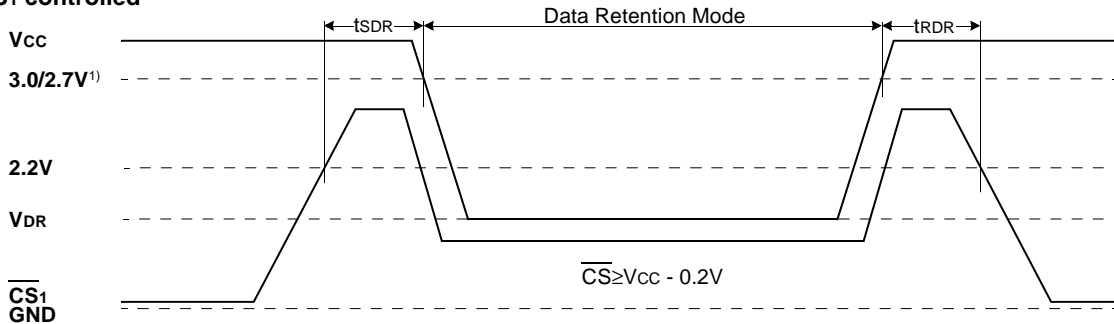


NOTES (WRITE CYCLE)

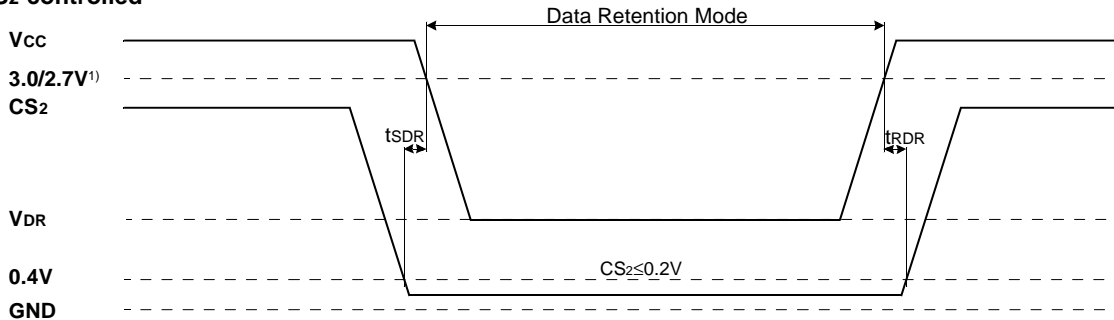
1. A write occurs during the overlap of a low \overline{CS}_1 , a high CS₂ and a low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS₂ going high and \overline{WE} going low : A write ends at the earliest transition among CS₁ going high, CS₂ going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS}_1 going low or CS₂ going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS}_1 or \overline{WE} going high . t_{WR2} is applied in case a write ends with CS₂ going low.

DATA RETENTION WAVE FORM

CS₁ controlled



CS₂ controlled

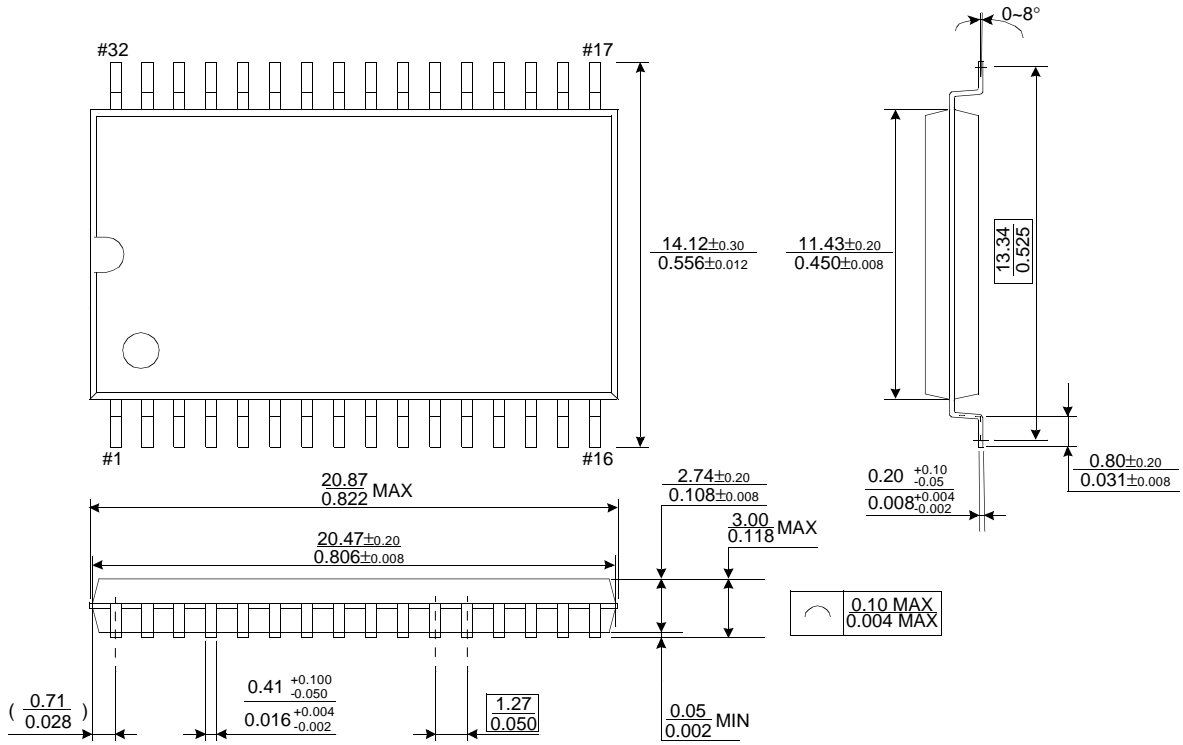


1. 3.0V for K6T1008V2E Family, 2.7V for K6T1008U2E Family

PACKAGE DIMENSIONS

Units: millimeters(inches)

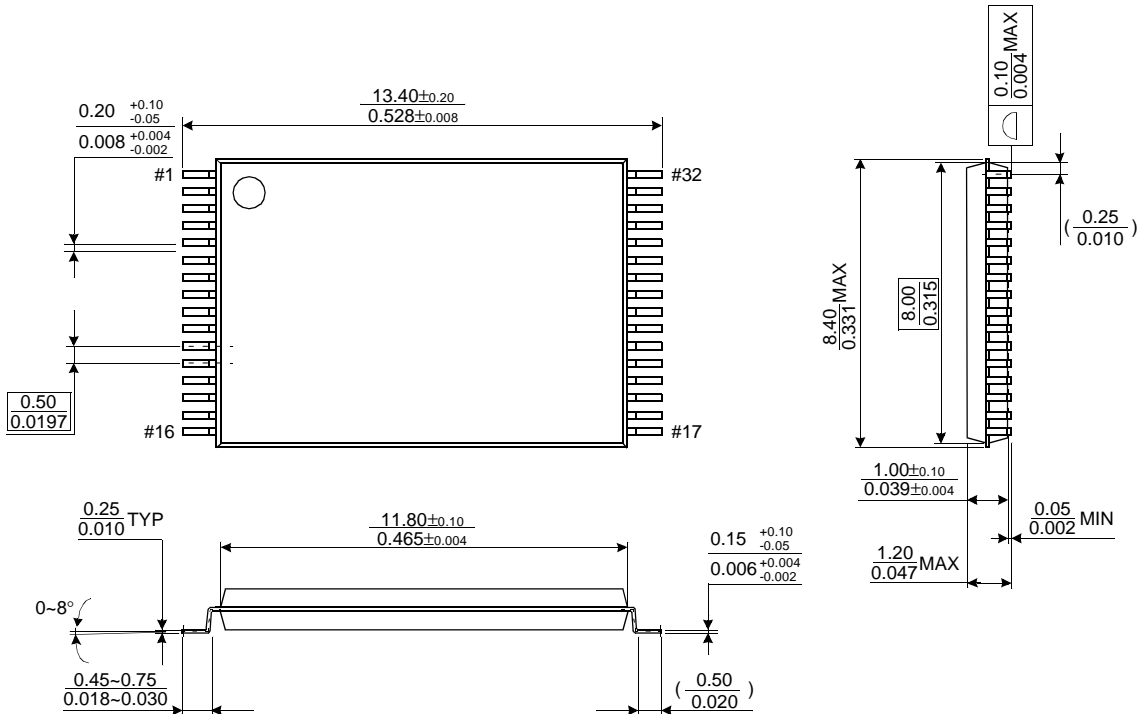
32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



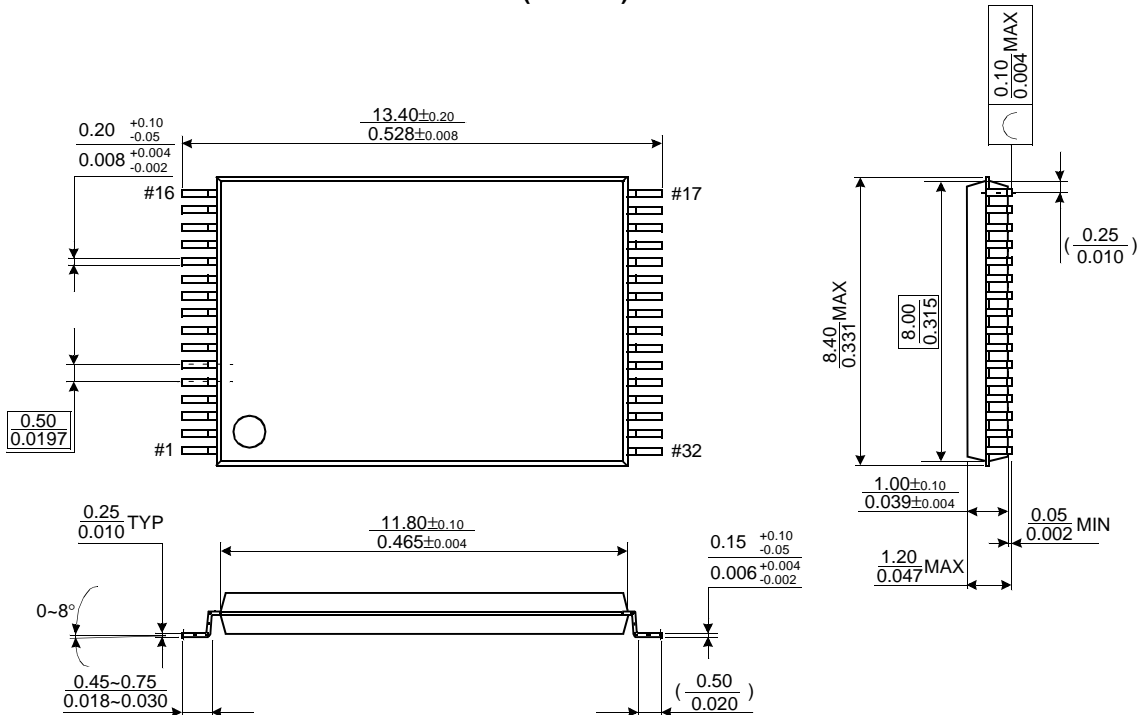
PACKAGE DIMENSIONS

Units: millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



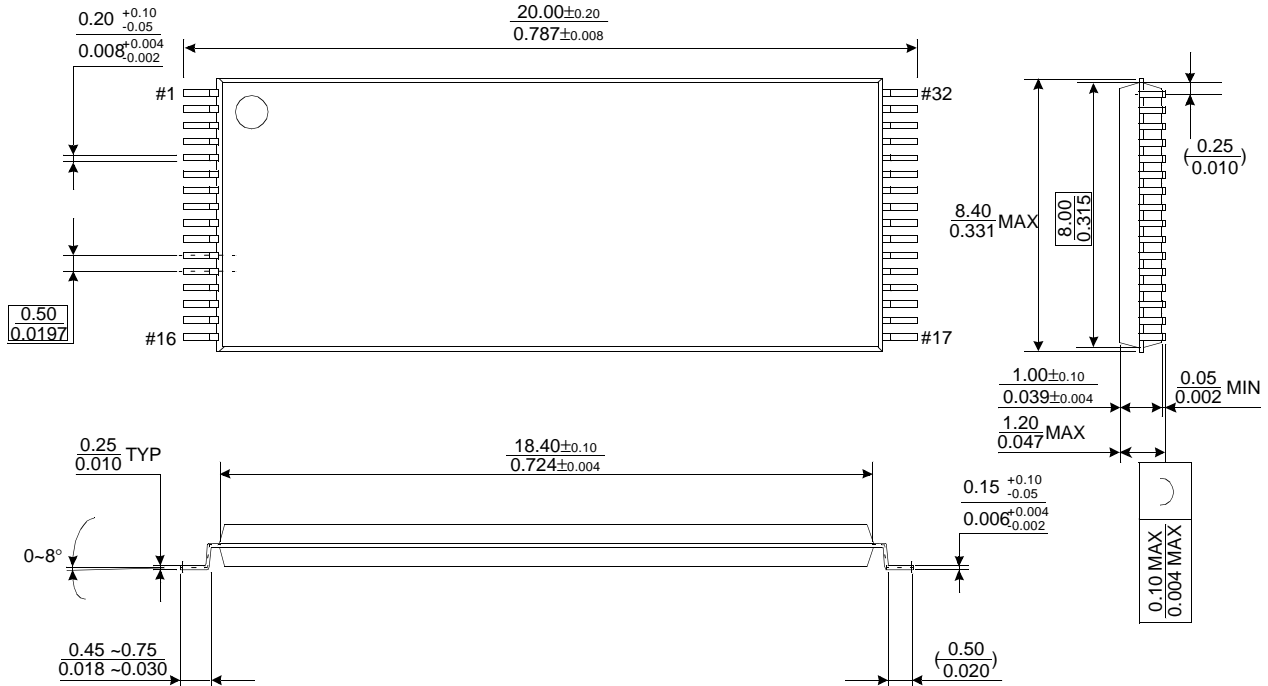
32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)



PACKAGE DIMENSIONS

Units: millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820R)

