WIDE DRAM

1 MEG x 16 DRAM

5.0V SELF REFRESH (MT4C1M16C3/5/6/7 S)
3.0/3.3V, SELF REFRESH (MT4LC1M16C3/5/6/7 S)

FEATURES

- SELF REFRESH, or "Sleep Mode"
- Industry standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V only or +3.0/+3.3V only ±10% power supply
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST-PAGE-MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C1M16C3/5 S only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1M16C5/7 S only)
- 1,024-cycle refresh in 128ms (ten rows and ten columns)
- Low power, 2mW standby; 500mW active, typical (5V)

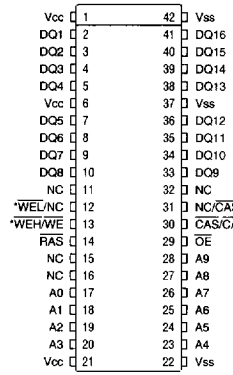
OPTIONS / MARKING

• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Power Supply	
+5V ±10% only	4C
+3.0/3.3V ±10% only	4LC
• Refresh Rate	
1,024 rows	None
4,096 rows	Contact Factory
• WRITE Cycle Access	
BYTE or WORD via $\overline{CAS}$ (nonmaskable)	16C3 S
BYTE or WORD via $\overline{CAS}$ (maskable)	16C5 S
BYTE or WORD via $\overline{WE}$ (nonmaskable)	16C6 S
BYTE or WORD via $\overline{WE}$ (maskable)	16C7 S
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

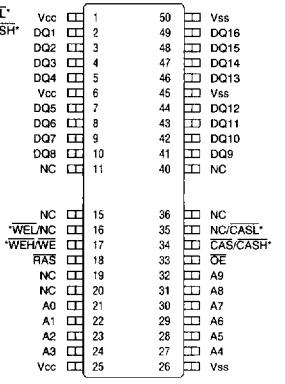
- Part Number Example: MT4C1M16C3DJ-7 S

PIN ASSIGNMENT (Top View)

42-Pin SOJ (DC-7)



44-Pin TSOP (DD-6)



*MT4C1M16C6/7 S / MT4C1M16C3/5 S

GENERAL DESCRIPTION

The MT4C1M163/5/6/7 S and MT4LC1M163/5/6/7 S are randomly accessed solid-state memories containing 16,777,216 bits organized in a x16 configuration. The MT4C1M163/5/6/7 S and the MT4LC1M163/5/6/7 S are the same DRAM versions except that the MT4LC1M163/5/6/7 S is the low voltage version of MT4C1M163/5/6/7 S. The MT4LC1M163/5/6/7 S is designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made to the MT4C1M163/5/6/7 S also apply to the MT4LC1M163/5/6/7 S, unless specifically stated otherwise. The MT4C1M16C6 S and MT4C1M16C7 S have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C1M16C3 S and MT4C1M16C5 S have both BYTE WRITE and WORD WRITE access cycles

via two $\overline{CAS}$ pins. The MT4C1M16C5 S and MT4C1M16C7 S are also able to perform WRITE-PER-BIT accesses.

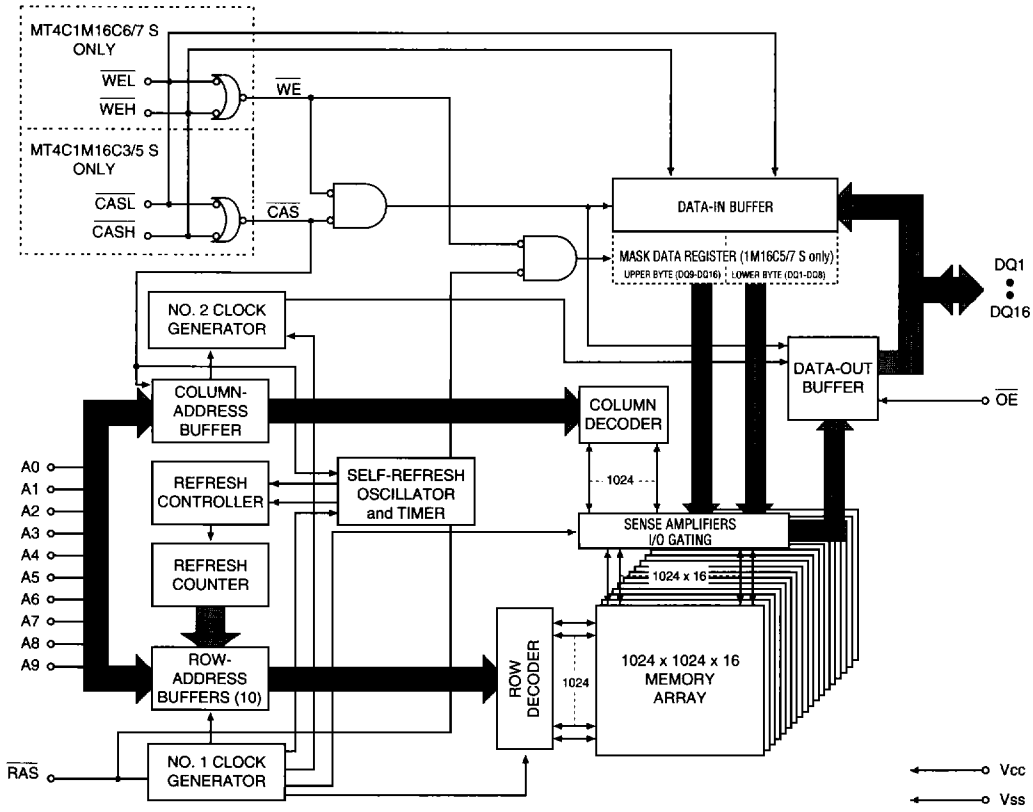
The MT4C1M16C3 S and MT4C1M16C6 S function in the same manner except that $\overline{WEL}$ and $\overline{WEH}$ on MT4C1M16C6 S and $\overline{CASL}$ and $\overline{CASH}$ on MT4C1M16C3 S control the selection of BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$ in that either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$.

The MT4C1M16C6 S $\overline{WE}$ function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8), and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1M16C3 S $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last $\overline{CAS}$ to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C1M16C3 S.

The MT4C1M16C5 S and MT4C1M16C7 S function in the same manner as MT4C1M16C3 S and MT4C1M16C6 S, respectively and they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C1M16C5 S and MT4C1M16C7 S to operate with either normal WRITE cycles or NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
14	18	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch-in the 10 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C1M16C5 S and MT4C1M16C7 S only).
30	34	$\overline{CAS}$/ $\overline{CASH}$	Input	Column-Address Strobe: $\overline{CAS}$ (MT4C1M16C6/7 S) is used to latch-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16. Column-Address Strobe Upper Byte: $\overline{CASH}$ (MT4C1M16C3/5 S) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
29	33	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C1M16C6/7 S) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C1M16C3/5 S) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C1M16C6/7 S) or $\overline{WE}$ (MT4C1M16C3/5 S) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	17	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C1M16C6/7 S) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C1M16C7 S, it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C1M16C3/5 S) controls DQ1 through DQ16 inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C1M16C5/7 S also uses $\overline{WE}$ to enable the mask register during $\overline{RAS}$ time.
12	16	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C1M16C6/7 S) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C1M16C3 S, it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
31	35	NC/$\overline{CASL}$	Input	Column-Address Strobe Lower Byte: $\overline{CASL}$ (MT4C1M16C3/5 S) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
17-20, 23-28	21-24, 27-32	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 1 Meg available words.

PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 33-36, 38-41	2-5, 7-10, 41-44, 46-49	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C1M16C6/7 S) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C1M16C3/7 S) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All sixteen I/Os are active for READ cycles (MT4C1M16C6/7 S). The MT4C1M16C3/5 S allows for BYTE READ cycles.
11, 15, 16, 30-32	11, 15, 36, 40	NC	-	No Connect: These pins should be left either unconnected or tied to ground.
1, 6, 21	1, 6, 25	Vcc	Supply	Power Supply: +5V ±10% (C) or 2.7V to 3.6V (LC)
22, 37, 42	26, 45, 50	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C1M16C6 S and MT4C1M16C7 S each have one $\overline{CAS}$ control while the MT4C1M16C3 S and MT4C1M16C5 S have two, $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 1 Meg x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8 and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C1M16C3 S and MT4C1M16C5 S $\overline{CAS}$ function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C1M16C3 S and MT4C1M16C5 S both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C1M16C3 S or MT4C1M16C5 S are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the $\overline{WE}$ on the MT4C1M16C6 S or MT4C1M16C7 S. The MT4C1M16C6 S and MT4C1M16C7 S $\overline{WE}$ function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1M16C6 S and MT4C1M16C7 S) or $\overline{WE}$ (MT4C1M16C3 S and MT4C1M16C5 S).

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BBU is a CBR REFRESH performed at the extended refresh rate with CMOS input levels. This mode provides a very low-current, data-retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during sleep mode. Thus, an external clock is not required, which provides additional power savings and design ease. The DRAM's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding both $\overline{RAS}$ and $\overline{CAS}$ LOW for a specified period. The industry standard for this value is 100µs minimum (^tRASS). The DRAM will remain in the SELF REFRESH mode while $\overline{RAS}$ and $\overline{CAS}$ remain LOW. Once $\overline{CAS}$ has been held LOW for 600µs (^tCHD), $\overline{CAS}$ is no longer required to remain LOW and becomes a "don't care." $\overline{CAS}$ is a "don't care" until ^tCHS, at which time $\overline{CAS}$ must be either HIGH or LOW.

The SELF REFRESH mode is terminated by taking $\overline{RAS}$ HIGH for the time minimum of an operation cycle, typically 200ns (^tRPS). Once the SELF REFRESH mode has been terminated, it is recommended that the user perform a refresh of all rows within the time of the external refresh rate prior to active use of the DRAM. The external refresh rate is typically 125µs per row-address. Once this burst has been completed, the DRAM may be used in the functional mode with distributed refreshes such as CBR or $\overline{RAS}$-ONLY.

The alternative approach when exiting SELF REFRESH mode is to utilize distributed refreshes once ^tRPS has been met, provided CBR REFRESH cycles are employed. The first CBR pulse should occur within the time of the external refresh rate prior to active use of the DRAM to ensure maximum data integrity and must be executed within three external refresh rate periods.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8). Enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C1M16C3 S, MT4C1M16C5 S, MT4C1M16C6 S and MT4C1M16C7 S may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{WE}$ or $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C1M16C6 S BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C1M16C3 S BYTE WRITE and WORD WRITE cycles.

The MT4C1M16C3 S also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C1M16C3 S BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C1M16C5/7 S ONLY)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1M16C3 S and MT4C1M16C6 S do not have the MASKED WRITE cycle function.

The mask data present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a NONPERSTENT MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same.

Figure 4 illustrates the MT4C1M16C7 S MASKED WRITE operation and Figure 5 illustrates the MT4C1M16C5 S MASKED WRITE operation.

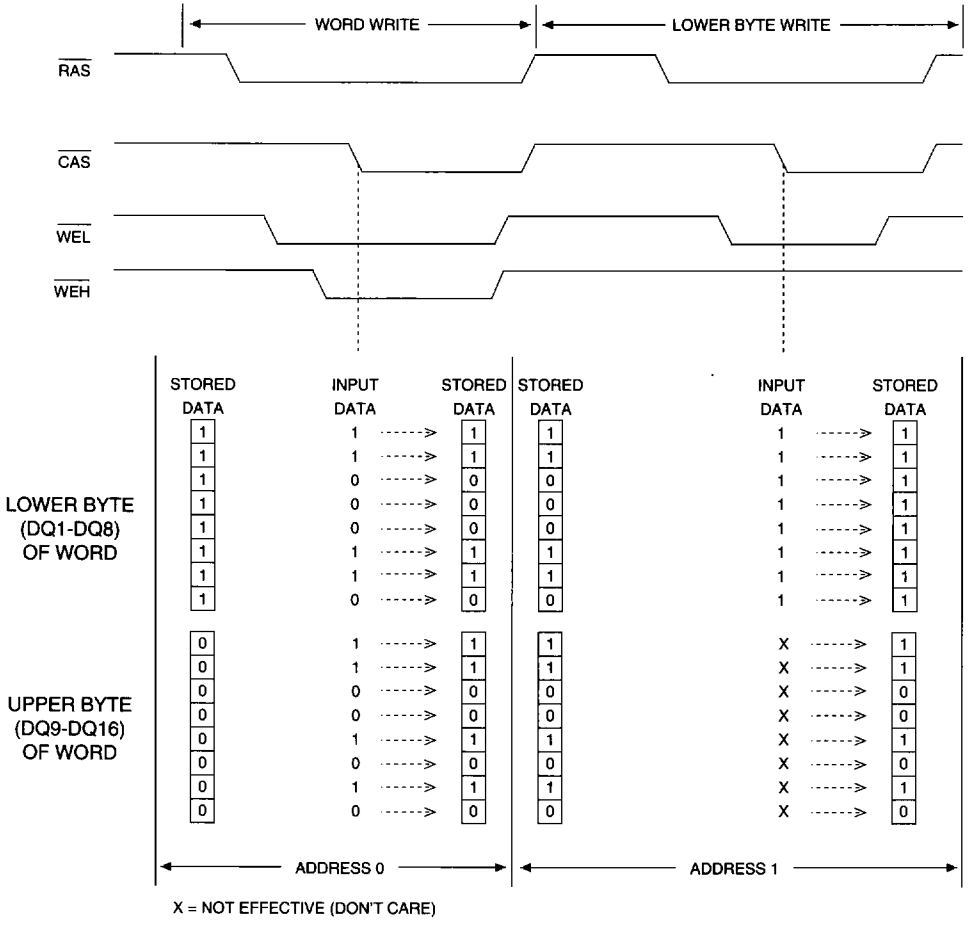


Figure 1
MT4C1M16C6/7 S WORD AND BYTE WRITE EXAMPLE

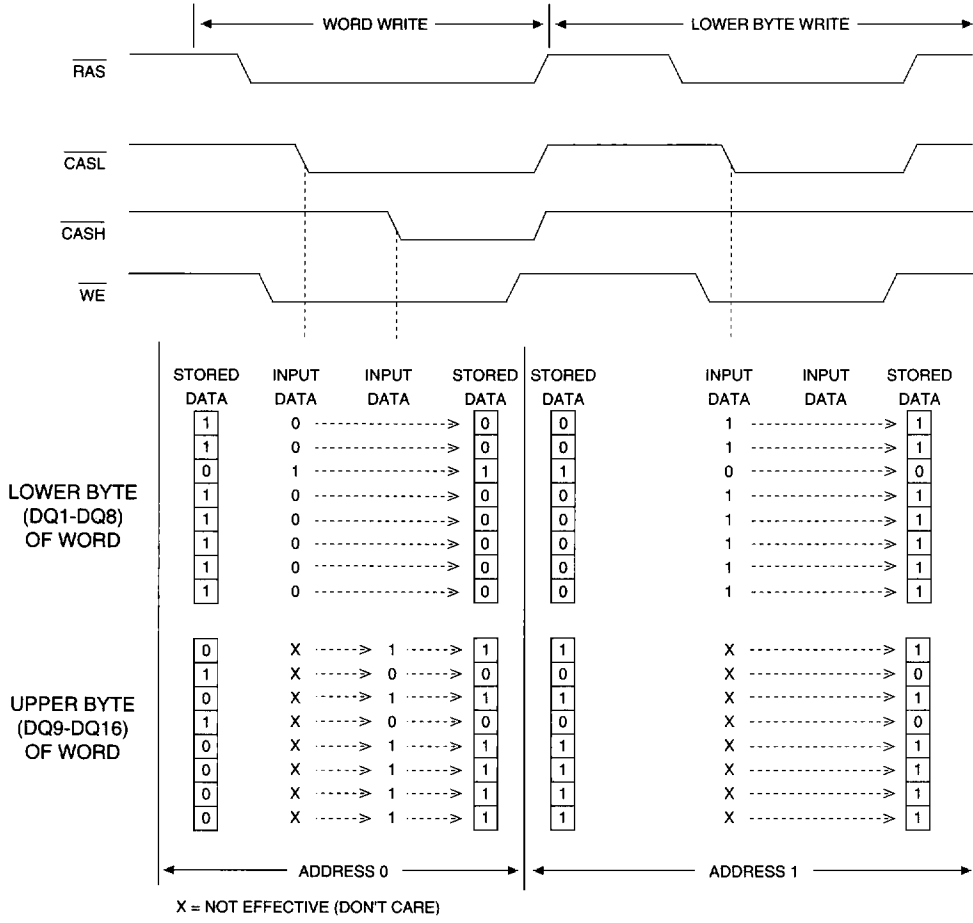


Figure 2
MT4C1M16C3/5 S WORD AND BYTE WRITE EXAMPLE

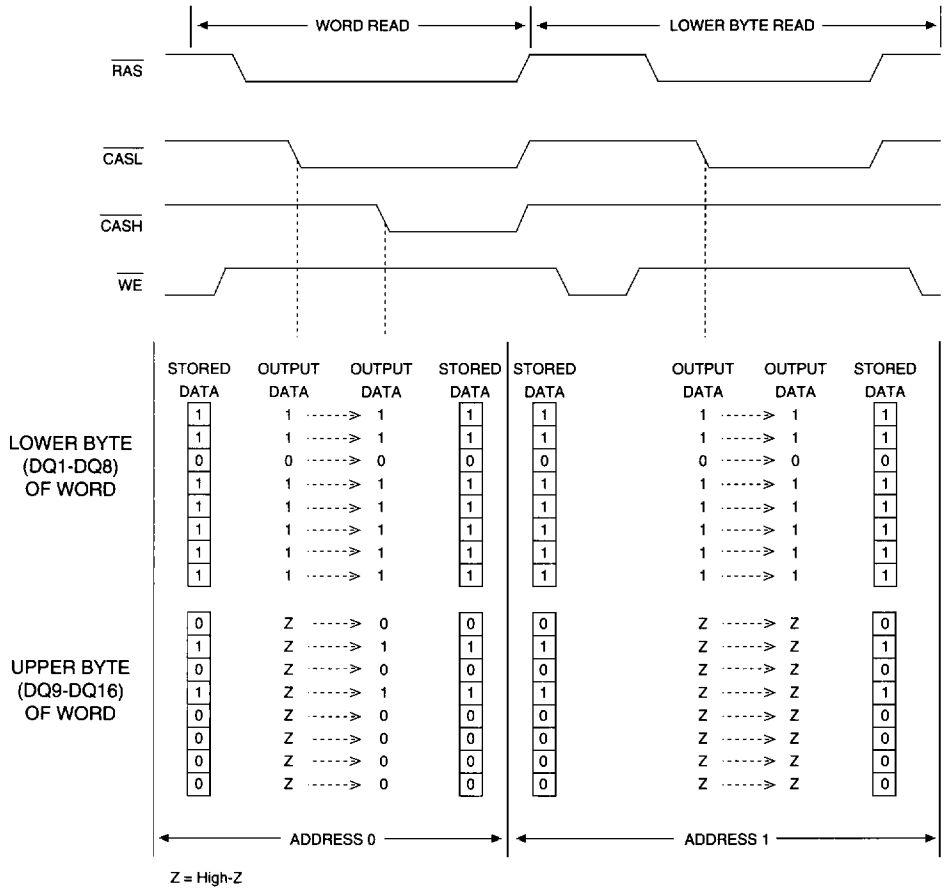


Figure 3
MT4C1M16C3/5 S WORD AND BYTE READ EXAMPLE

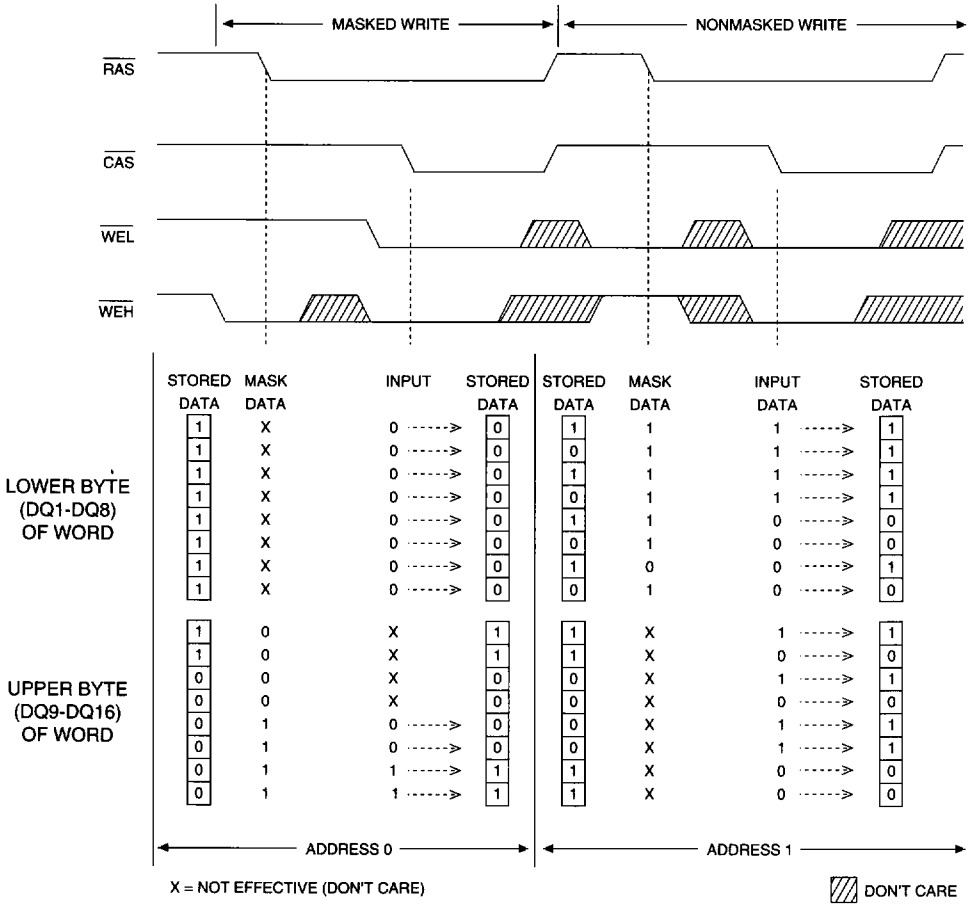


Figure 4
MT4C1M16C7 S MASKED WRITE EXAMPLE

NOTE: If $\overline{WEL}$ is LOW and $\overline{WEH}$ is HIGH when $\overline{RAS}$ goes LOW, then only DQs 1-8 will be masked. If $\overline{WEL}$ is HIGH and $\overline{WEH}$ is LOW when $\overline{RAS}$ goes LOW, then only DQs 9-16 will be masked.

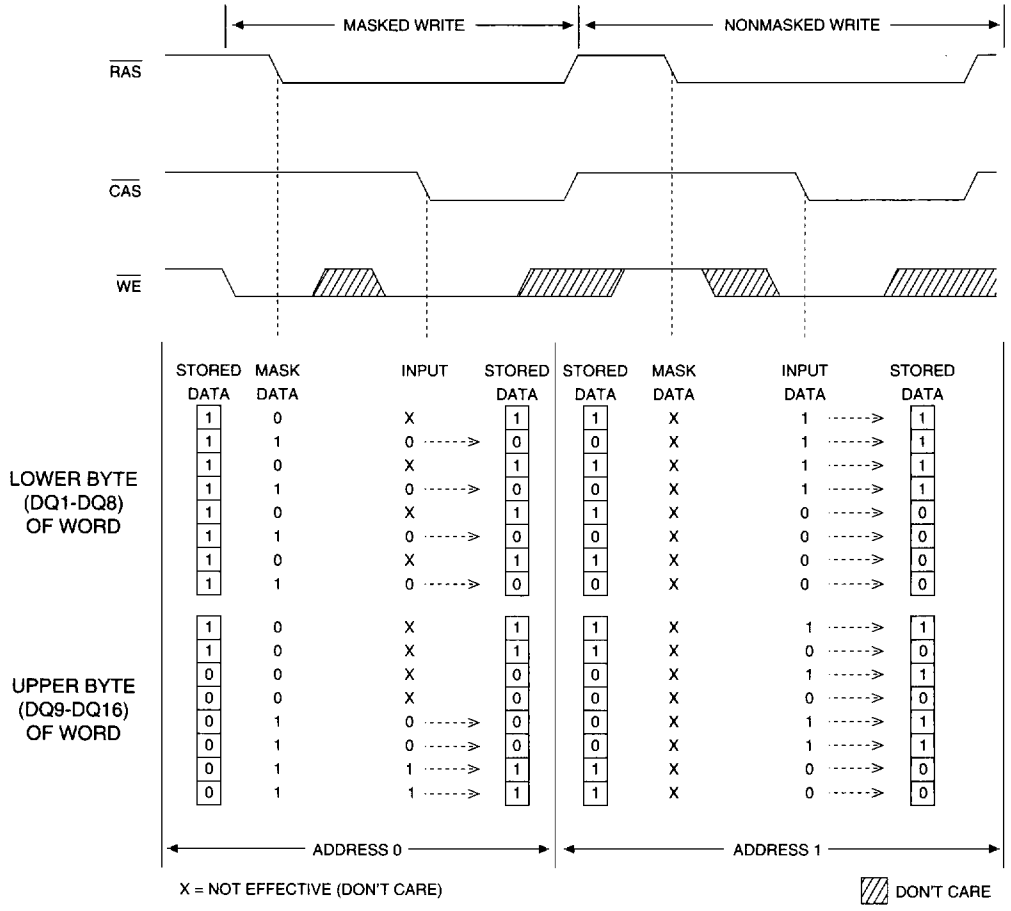


Figure 5
MT4C1M16C5 S MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1M16C6/7 S

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data-In, Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z, Upper Byte, Data-In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 3
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data-In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data-In	1, 3
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 2, 3
RAS-ONLY REFRESH		L	H	H	H	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	H	H	X	X	X	High-Z	
BBU REFRESH		H→L	L	H	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	H	H	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C1M16C7 S only). Refer to Figure 4.

TRUTH TABLE: MT4C1M16C3/5 S

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1, 5
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1, 5
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2, 5
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2, 5
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4
BBU REFRESH		H→L	L	L	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	L	H	X	X	X	High-Z	

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one CAS must be active (CASL or CASH).
5. Data-in will be dependent on the mask provided (MT4C1M16C5 S only). Refer to Figure 5.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} (5V) ..... -1V to +7V
Voltage on V_{CC} supply relative to V_{SS} (3V) .... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1, 44
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) (0°C ≤ T_A ≤ 70°C; V_{CC} = 2.7V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	2.7	3.6	V	1, 44
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 1.0mA)	V_{OL}		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	300	300	300	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: tRC = tRC [MIN])	ICC3	170	160	140	mA	3, 4, 44
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC [MIN]; tCP, tASC = 10ns)	ICC4	130	120	110	mA	3, 4, 44
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=VIH: tRC = tRC [MIN])	ICC5	170	160	140	mA	3, 5, 44
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: tRC = tRC [MIN])	ICC6	170	160	140	mA	3, 5
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open); tRC = 125µs (1,024 rows at 125µs = 128ms)	ICC7	400	400	400	µA	3, 42
REFRESH CURRENT: SELF Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	ICC8	400	400	400	µA	5

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) (0°C ≤ T_A ≤ 70°C; Vcc = 2.7V to 3.6V)

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	170	160	140	mA	3, 4, 44
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	130	120	110	mA	3, 4, 44
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	170	160	140	mA	3, 4, 44
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	170	160	140	mA	3, 4
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	400	400	400	µA	3, 42
REFRESH CURRENT: SELF Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	I_{CC8}	400	400	400	µA	5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ-WRITE cycle time	^tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	35
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 33
Output Enable	^tOE		15		15		15	ns	33
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	33
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	40
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	15	100,000	20	100,000	20	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (FAST-PAGE-MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	15	45	20	50	20	60	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	32
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	31
Column-address hold time	^tCAH	10		15		15		ns	31
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26, 32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	t_{OFF}	3	15	3	20	3	20	ns	20, 29, 33
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	21, 26, 31
Write command hold time	t_{WCH}	10		15		15		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	45		55		60		ns	26
Write command pulse width	t_{WP}	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	26, 32
Data-in setup time	t_{DS}	0		0		0		ns	22, 33
Data-in hold time	t_{DH}	10		15		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	t_{DHR}	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	t_{AWD}	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40		45		45		ns	21, 31
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	t_{REF}		128		128		128	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	t_{CSR}	5		5		5		ns	5, 31
$\overline{CAS}$ hold time (CBR REFRESH)	t_{CHR}	15		15		15		ns	5, 32
$\overline{WE}$ hold time (MASKED WRITE and CBR REFRESH)	t_{WRH}	15		15		15		ns	26, 27
$\overline{WE}$ setup time (CBR REFRESH)	t_{WRP}	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	t_{WRS}	10		10		10		ns	26, 27
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	t_{ORD}	0		0		0		ns	
Output disable	t_{OD}	3	15	3	15	3	15	ns	29, 41
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	t_{OEH}	15		15		15		ns	28
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	t_{CLCH}	10		10		10		ns	34
Mask data to $\overline{RAS}$ setup time	t_{MS}	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ setup time	t_{MH}	15		15		15		ns	26, 27
$\overline{RAS}$ pulse width during SELF REFRESH cycle	t_{RASS}	100		100		100		µs	46
$\overline{RAS}$ precharge time during SELF REFRESH cycle	t_{RPS}	150		150		150		ns	46
$\overline{CAS}$ hold time during SELF REFRESH cycle	t_{CHS}	-70		-70		-70		ns	46
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	t_{CHD}	600		600		600		µs	29

NOTES

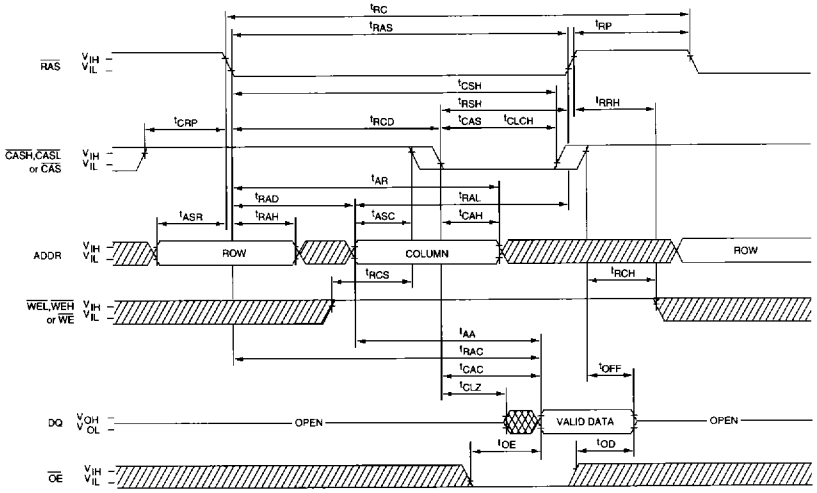
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V or 3.0/3.3V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.*
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE and READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1M16C6/7 S. Write command is defined as $\overline{WE}$ going LOW on the MT4C1M16C3/5 S.
27. MT4C1M16C5/7 S only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

*The 3ns minimum is a parameter guaranteed by design.

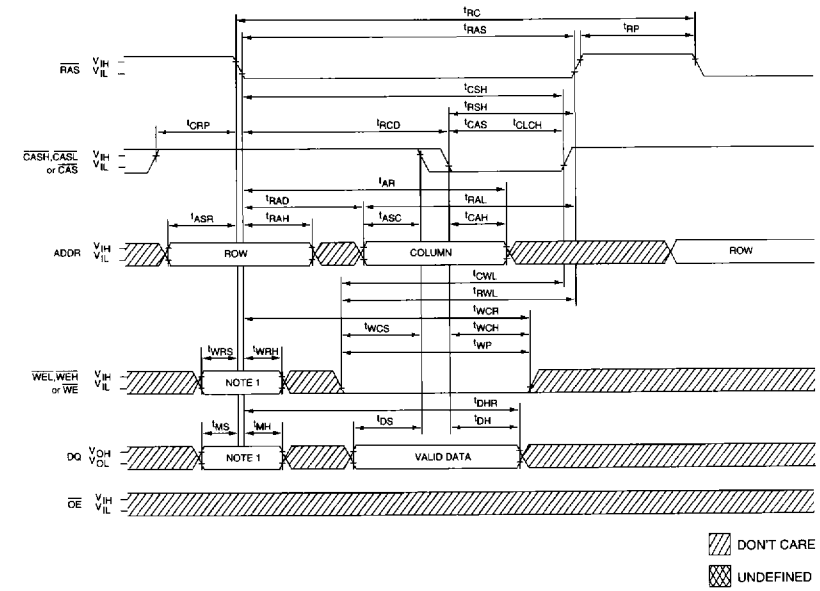
NOTES (continued)

30. Notes 31 through 41 apply to MT4C1M16C3/5 S only.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. BBU current is reduced as ^{t}RAS is reduced from its maximum specification during BBU cycle.
43. The 5V version is restricted to operate between 4.5 V and 5.5V only.
44. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only. The -6 speed version is only valid for V_{CC} = 3.0V to 3.6 V whereas the -7 and -8 speed versions are valid for V_{CC} = 2.7V to 3.6V.
45. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
46. When exiting the SELF REFRESH mode, a complete set of row refreshes should be executed in order to ensure that the DRAM will be fully refreshed. Alternatively, distributed refreshes may be utilized, provided CBR refreshes are employed.

READ CYCLE

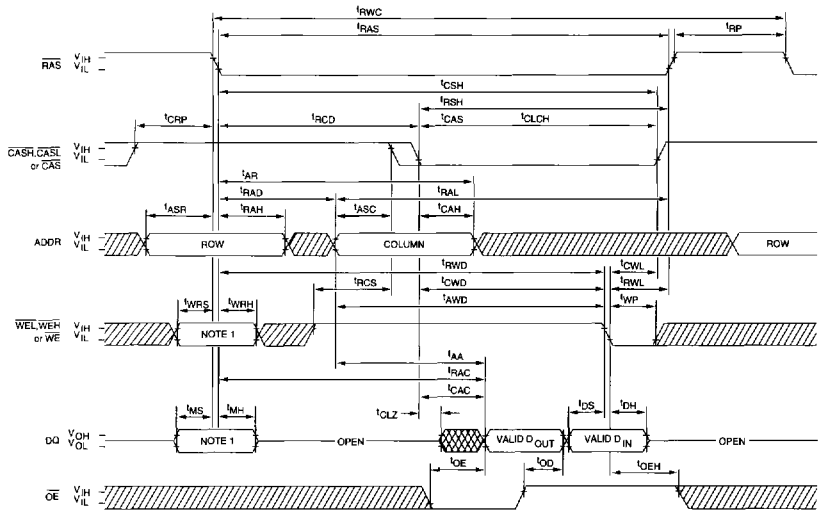


EARLY-WRITE CYCLE

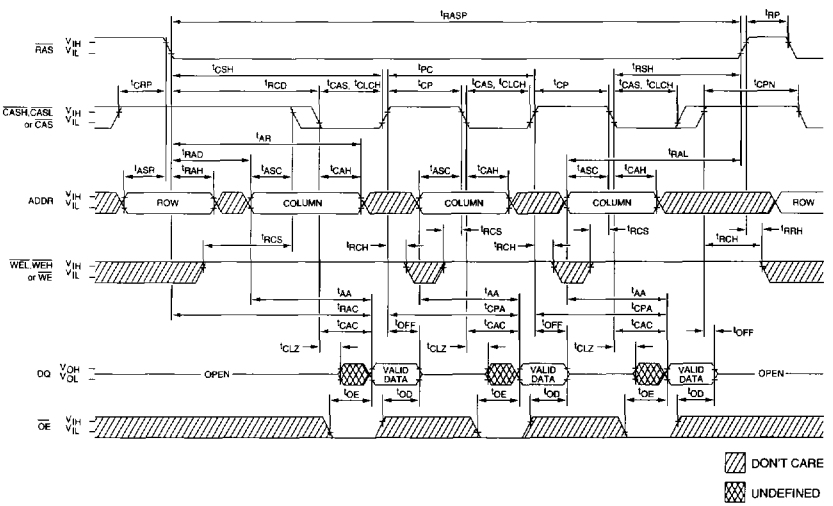


NOTE: 1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at $\overline{RAS}$ time.

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

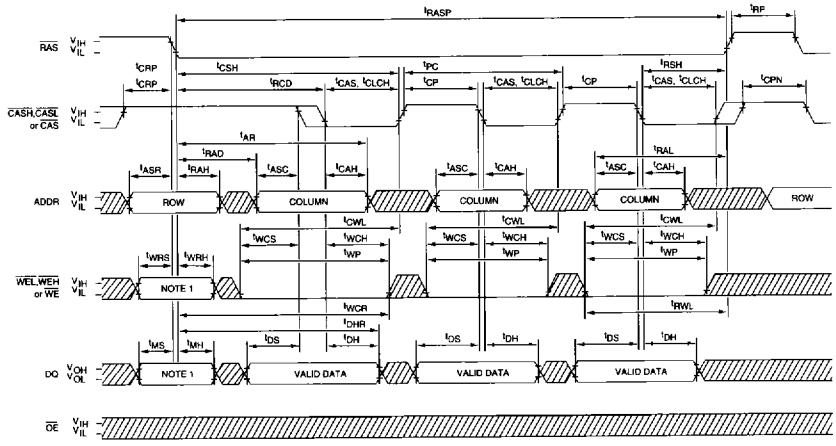


FAST-PAGE-MODE READ CYCLE

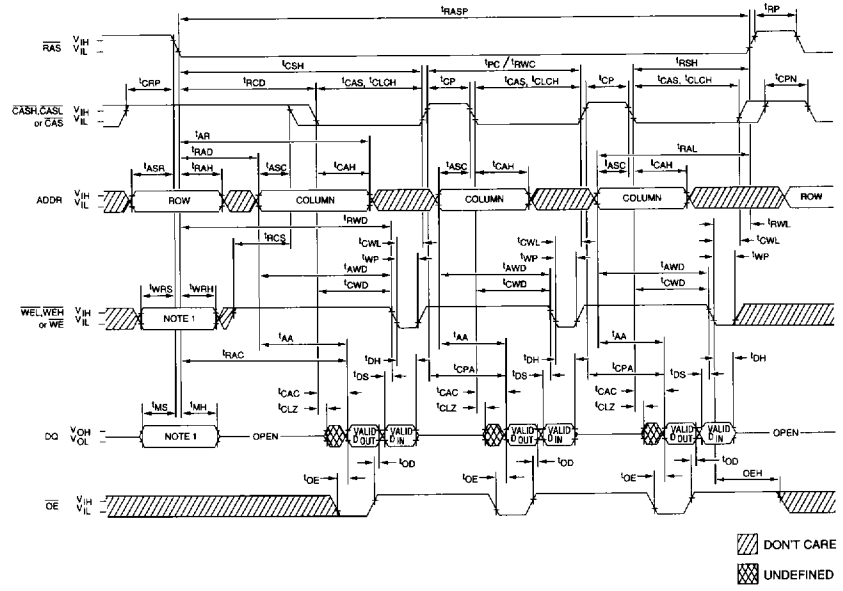


NOTE: 1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE EARLY-WRITE CYCLE

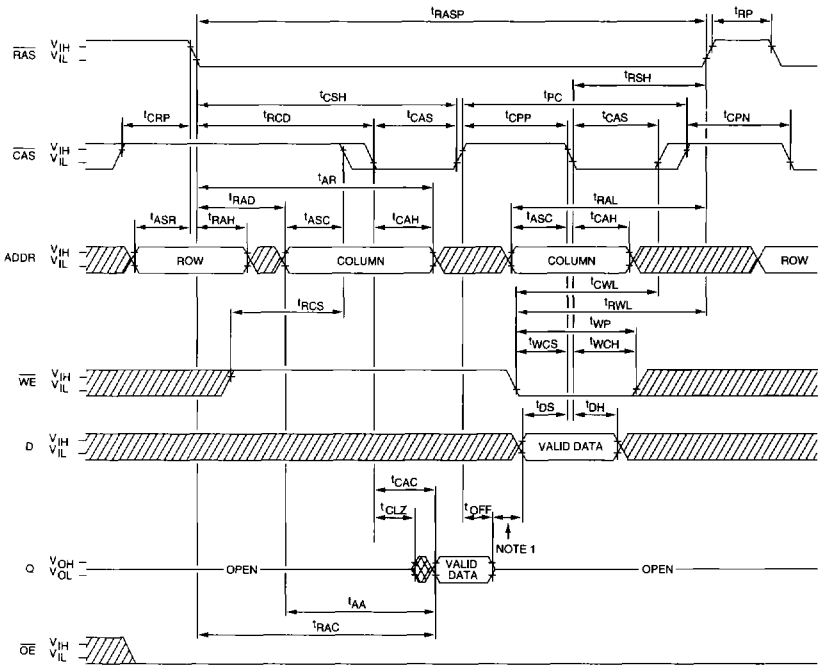


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



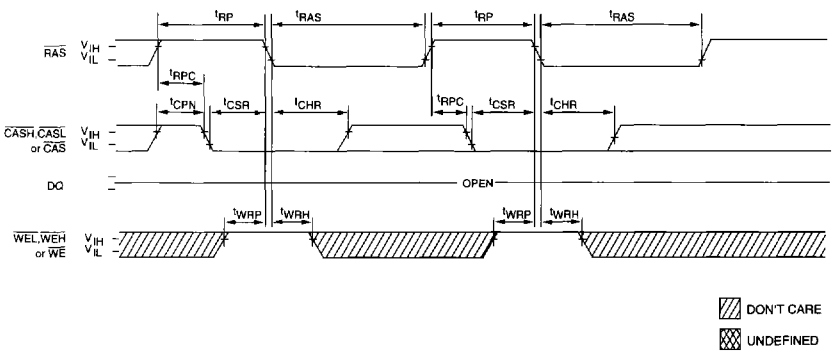
NOTE: 1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at $\overline{RAS}$ time.

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

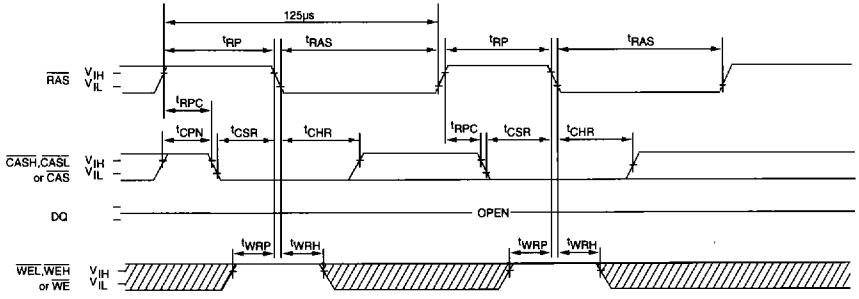


NOTE: 1. Do not drive data prior to High-Z; that is completion of tOFF. tCPP is equal to tOFF + tDS(MIN) + guardband between data-out and driving new data-in.

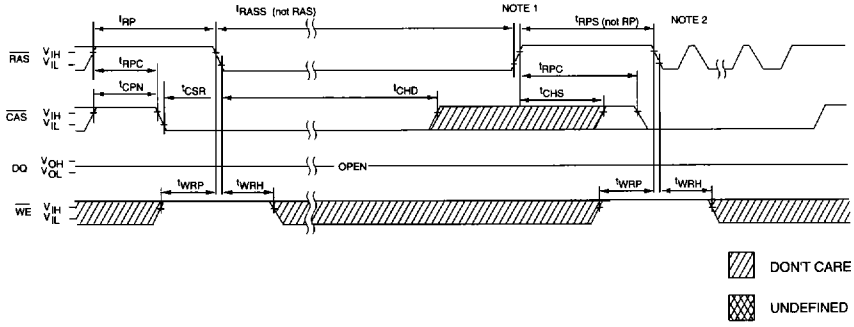
CBR REFRESH CYCLE
(A0-A9, $\overline{OE}$ = DON'T CARE)



BBU REFRESH CYCLE
(A0-A9, $\overline{OE}$ = DON'T CARE)



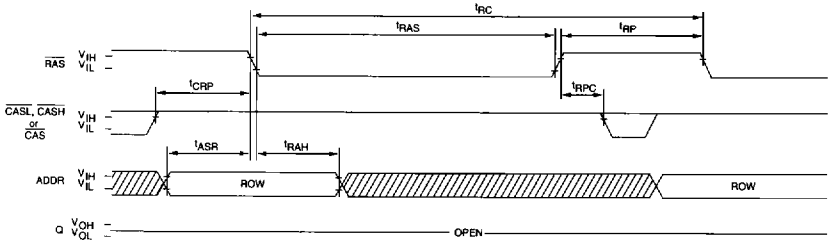
SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A9, $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a compete burst of all rows should be executed.

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

(ADDR = A0-A9, $\overline{\text{OE}}$; $\overline{\text{WEL}}$, $\overline{\text{WEH}}$ or $\overline{\text{WE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

($\overline{\text{WEL}}$, $\overline{\text{WEH}}$ or $\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)