

Flip-flop

54F109

DESCRIPTION

The 54F109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, K, Clock, Set and Reset inputs, and complementary Q outputs.

Set (\overline{S}_D) and Reset (\overline{R}_D) are asynchronous active-Low inputs and operate independently of the Clock Input.

The J and K are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition of the positive-going pulse.

The J and K inputs must be stable just one setup time prior to the Low-to-High transition of the Clock for predictable operation.

The JK design allows operation as a D flip-flop by tying the J and \overline{K} inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	54F109/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	54F109/BFA	GDFP2-F16
20-Pin Ceramic LLCC	54F109/B2A	CQCC2-N20

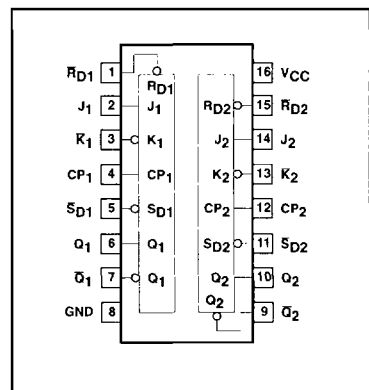
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

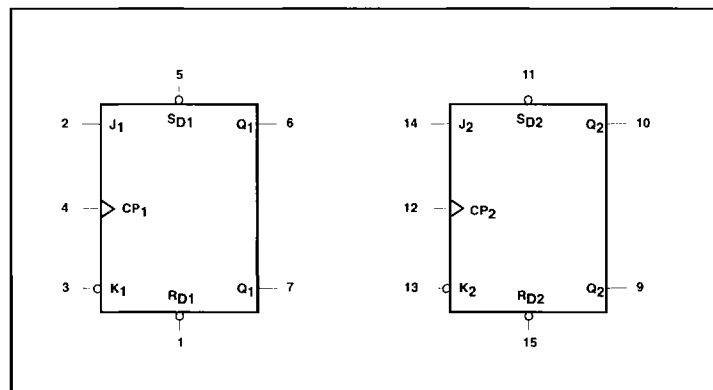
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J ₁ - J ₂ , \overline{K}_1 - \overline{K}_2	Data inputs	1.0/1.0	20μA/0.6mA
CP ₁ , CP ₂	Clock pulse inputs (active rising edge)	1.0/1.0	20μA/0.6mA
\overline{R}_D1 , \overline{R}_D2	Reset inputs (active Low)	1.0/3.0	20μA/1.8mA
\overline{S}_D1 , \overline{S}_D2	Set inputs (active Low)	1.0/3.0	20μA/1.8mA
Q ₁ , Q ₂ , \overline{Q}_1 , \overline{Q}_2	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

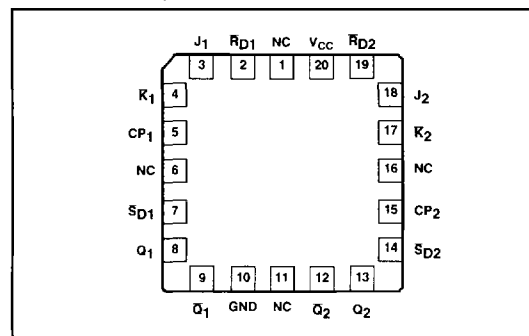
PIN CONFIGURATION



LOGIC SYMBOL



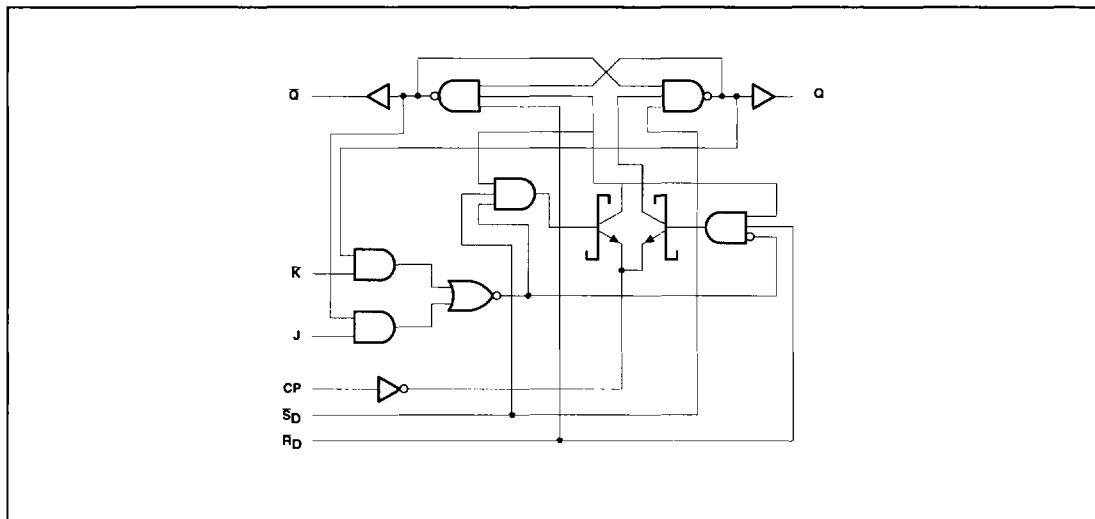
LLCC LEAD CONFIGURATION



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LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	J	K	q	\bar{q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	\bar{q}	q
Load "0" (Reset)	H	H	↑	l	l	L	H
Load "1" (Set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	\bar{q}

H = High voltage level steady state
 L = Low voltage level steady state
 h = High voltage level one setup time prior to the Low-to-High Clock transition
 l = Low voltage level one setup time prior to the Low-to-High Clock transition
 X = Don't care
 q = Lower case letters indicate the state of the referenced output prior to the Low-to-High Clock transition
 ↑ = Low-to-High Clock transition

NOTE:
 Both outputs will be High if both \bar{S}_D and \bar{R}_D go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1.0	mA
I _{OL}	Low-level output current			20.0	mA
T _A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ ²	Max	
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OH} = Max, V _{IH} = Min	2.5			V
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OL} = Max, V _{IH} = Min		0.35	0.50	V
V _{IK}	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}		-0.73	-1.2	V
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max, V _I = 7.0V			100	μA
I _{IH1}	High-level input current	J, K, CP inputs S _D , R _D inputs	V _{CC} = Max, V _I = 2.7V	1	20	μA
				1	20	μA
I _{IL}	Low-level input current	J, K, CP inputs S _D , R _D inputs	V _{CC} = Max, V _I = 0.5V	-0.4	-0.6	mA
				-1.3	-1.8	mA
I _{OS}	Short-circuit output current ³	V _{CC} = Max, V _O = 0.0V	-60	-85	-150	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = Max		12.3	17	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _A = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 1	90	125		80 ⁵		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Q _n , Q _n	Waveform 1	3.8	5.3	7.0	3.8	9.0	ns
			4.4	6.2	8.0	4.4	10.5	ns
t _{PLH} t _{PHL}	Propagation delay S _{Dn} or R _{Dn} to Q _n , Q _n	Waveform 2	3.2	5.2	7.0	2.8	9.0	ns
			3.5	7.0	9.0	3.5	11.5	ns

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and Q̄ outputs High in turn.
- These parameters are guaranteed, but not tested.

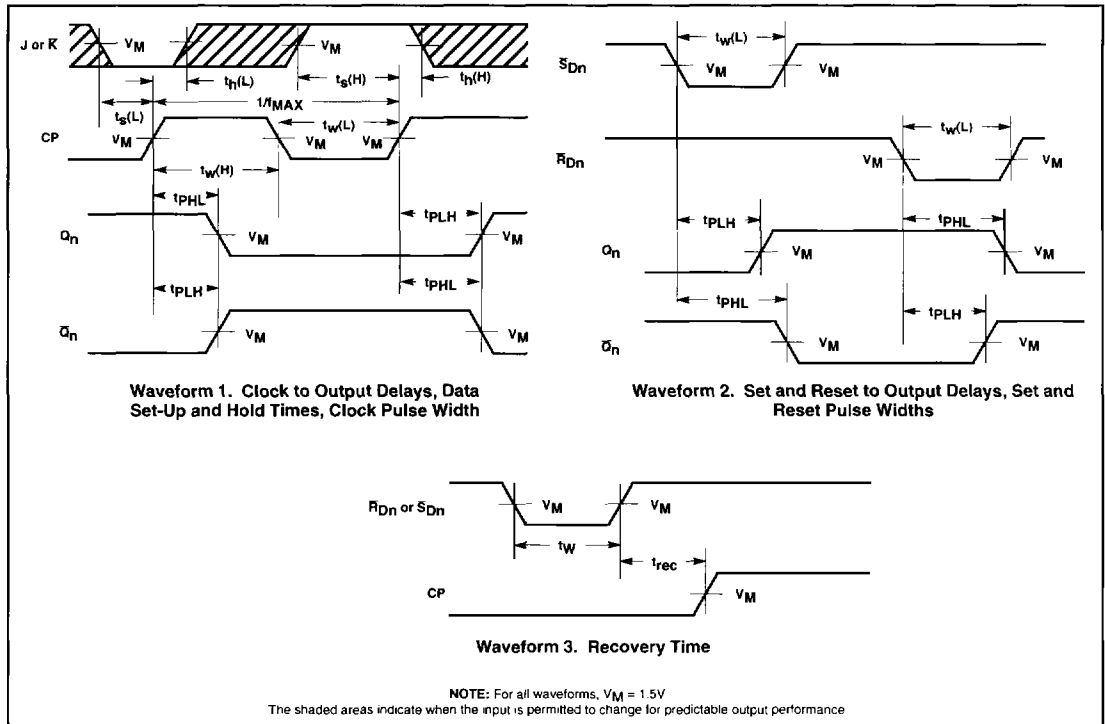
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AC SETUP REQUIREMENTS

			T _A = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _A = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _s (H) t _s (L)	Setup time High or Low, J or K to CP	Waveform 1	3.0 3.0			5.0 5.0		ns ns
t _h (H) t _h (L)	Hold time, High or Low, J or K to CP	Waveform 1	1.0 1.0			1.0 1.0		ns ns
t _w (H) t _w (L)	Clock pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns ns
t _w (L)	Set or Reset pulse width, Low	Waveform 2	4.0			4.0		ns
t _{rec}	Recovery time, Set or Re- set to clock	Waveform 3	2.0			2.0		ns

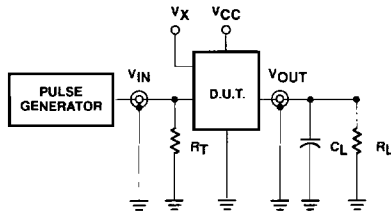
AC WAVEFORMS



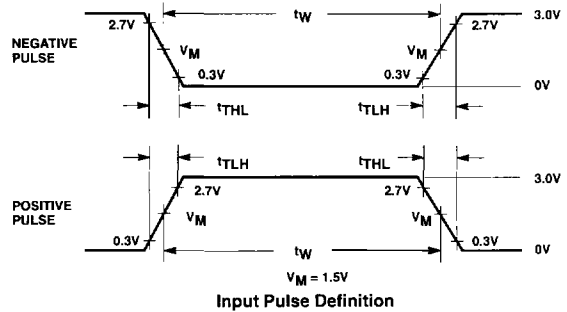
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TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

- R_L = Load Resistor; see AC Characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- V_X = Unclocked pins must be held at: $\leq 0.8V$; $\geq 2.7V$ or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$