# DATA SHEET

# 74AC16373/74ACT16373

## 16-bit D-type transparent latch (3-State)

Product specification

1997 Jul 15

# 16-bit D-type transparent latch (3-State)

## FEATURES

- 74ACT16373 has TTL-compatible inputs
- 74AC16373 has CMOS-compatible inputs
- 3-State outputs source/sink 24mA
- 3-State outputs drive bus lines or buffer memory address registers
- Distributed power and ground pins for minimum noise and ground bounce
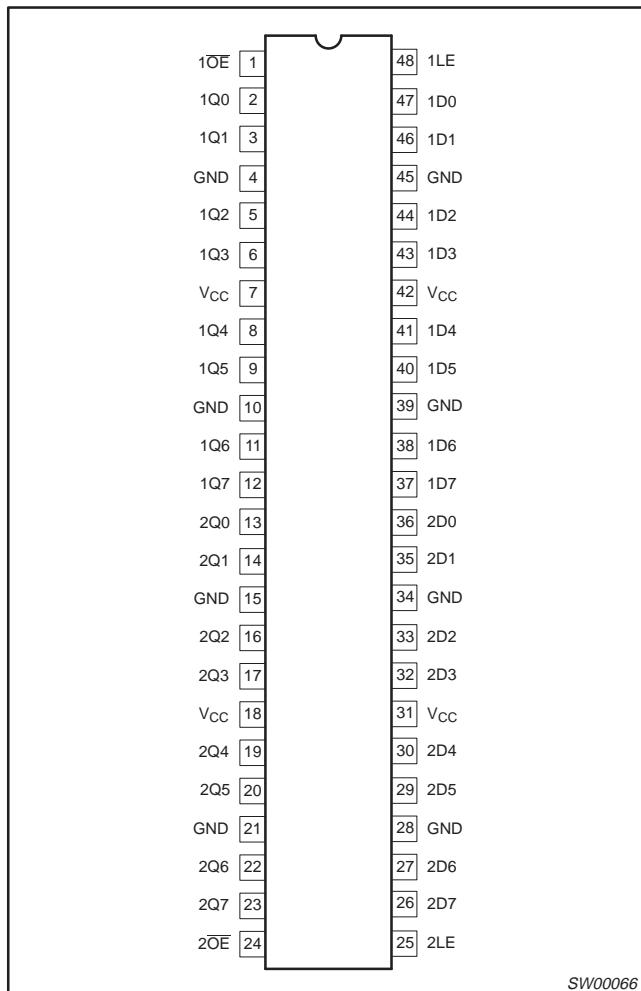
## DESCRIPTION

The 74AC16373/74ACT16373 is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. One latch enable (LE) input and one output enable ($\overline{OE}$) are provided for each octal.

The '16373' consists of 2 sections of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

## PIN CONFIGURATION

| | Pin | | Pin | |
|---|---|---|---|---|
| $1\overline{OE}$ | 1 | | 48 | 1LE |
| 1Q0 | 2 | | 47 | 1D0 |
| 1Q1 | 3 | | 46 | 1D1 |
| GND | 4 | | 45 | GND |
| 1Q2 | 5 | | 44 | 1D2 |
| 1Q3 | 6 | | 43 | 1D3 |
| $V_{CC}$ | 7 | | 42 | $V_{CC}$ |
| 1Q4 | 8 | | 41 | 1D4 |
| 1Q5 | 9 | | 40 | 1D5 |
| GND | 10 | | 39 | GND |
| 1Q6 | 11 | | 38 | 1D6 |
| 1Q7 | 12 | | 37 | 1D7 |
| 2Q0 | 13 | | 36 | 2D0 |
| 2Q1 | 14 | | 35 | 2D1 |
| GND | 15 | | 34 | GND |
| 2Q2 | 16 | | 33 | 2D2 |
| 2Q3 | 17 | | 32 | 2D3 |
| $V_{CC}$ | 18 | | 31 | $V_{CC}$ |
| 2Q4 | 19 | | 30 | 2D4 |
| 2Q5 | 20 | | 29 | 2D5 |
| GND | 21 | | 28 | GND |
| 2Q6 | 22 | | 27 | 2D6 |
| 2Q7 | 23 | | 26 | 2D7 |
| $2\overline{OE}$ | 24 | | 25 | 2LE |

SW00066

## QUICK REFERENCE DATA

GND = 0V; $T_{amb}$ = 25°C; $t_r$ = $t_f$ ≤ 2.5ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | AC | | ACT | |
| | | | $V_{CC}$ = 3.3V | $V_{CC}$ = 5.0V | $V_{CC}$ = 5.0V | |
| $t_{PHL}/t_{PLH}$ | Propagation delay Dn to Qn; LE to Qn | $C_L$ = 50pF | 3.7 4.1 | 2.5 2.7 | 3.8 4.4 | ns |
| $C_I$ | Input capacitance | | 4.5 | | | pF |
| $C_{PD}$ | Power dissipation capacitance | $V_I$ = GND to $V_{CC}$[1] outputs enabled[2] outputs enabled[3] outputs disabled[2] outputs disabled[3] | 26 216 14 54 | | 29 240 16 68 | pF |

**NOTE:**
1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   $f_i$ = input frequency in MHz; $C_L$ = output load capacity in pF; $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. Switch the latch enable and one data input such that one latch toggles.
3. Switch the latch enables and all data inputs such that all 16 latches toggle.

# 16-bit D-type transparent latch (3-State)
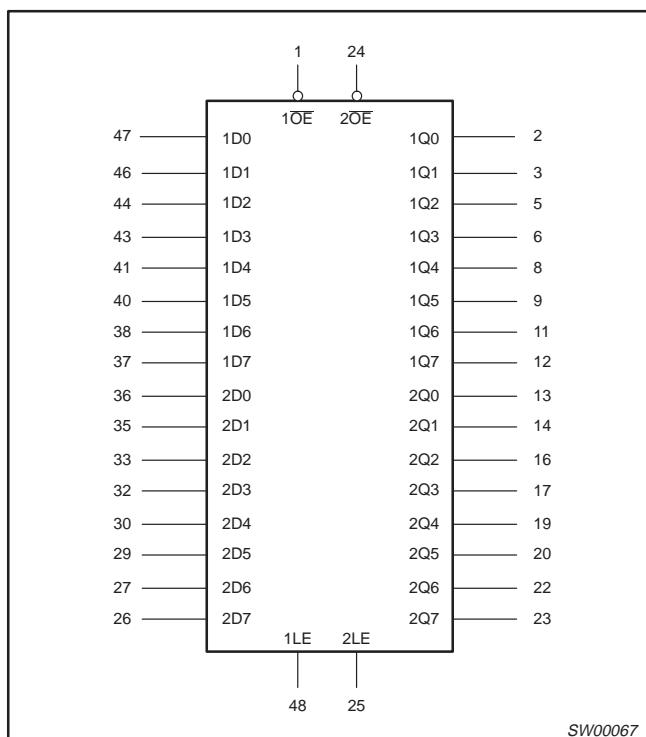
## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|---|---|---|---|---|
| 48-Pin Plastic SSOP Type III | −40°C to +85°C | 74AC16373 DL<br>74ACT16373 DL | 7AC16373 DL<br>7AT16373 DL | SOT370-1 |
| 48-Pin Plastic TSSOP Type II | −40°C to +85°C | 74AC16373 DGG<br>74ACT16373 DGG | 7AC16373 DGG<br>7AT16373 DGG | SOT362-1 |
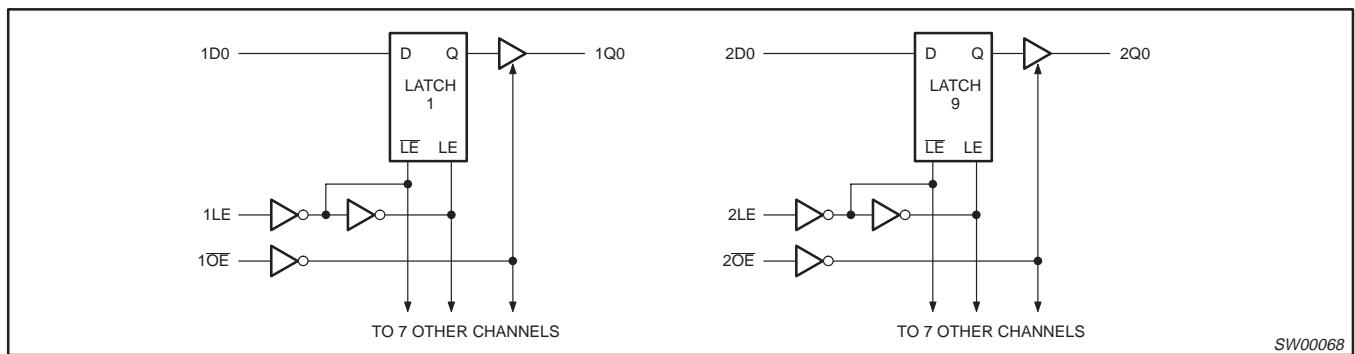
## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | 1$\overline{\text{OE}}$ | Output enable input (active LOW) |
| 2, 3, 5, 6, 8, 9, 11, 12 | 1Q0 to 1Q7 | Data inputs/outputs |
| 4, 10, 15, 21, 28, 34, 39, 45 | GND | Ground (0V) |
| 7, 18, 31, 42 | $V_{CC}$ | Positive supply voltage |
| 13, 14, 16, 17, 19, 20, 22, 23 | 2Q0 to 2Q7 | Data inputs/outputs |
| 24 | 2$\overline{\text{OE}}$ | Output enable input (active LOW) |
| 25 | 2LE | Latch enable input (active HIGH) |
| 36, 35, 33, 32, 30, 29, 27, 26 | 2D0 to 2D7 | Data inputs |
| 47, 46, 44, 43, 41, 40, 38, 37 | 1D0 to 1D7 | Data inputs |
| 48 | 1LE | Latch enable input (active HIGH) |

## LOGIC SYMBOL



SW00067

## LOGIC DIAGRAM



SW00068

16-bit D-type transparent latch (3-State)

74AC16373
74ACT16373

## FUNCTION TABLE (per section of eight bits)

| OPERATING MODES | INPUTS | | | INTERNAL LATCHES | OUTPUTS |
| | $\overline{OE}$ | LE | Dn | | Q0 to Q7 |
| --- | --- | --- | --- | --- | --- |
| Enable and read register (transparent mode) | L<br>L | H<br>H | L<br>H | L<br>H | L<br>H |
| Latch and read register | L<br>L | L<br>L | l<br>h | L<br>H | L<br>H |
| Latch register and disable outputs | H<br>H | L<br>L | l<br>h | L<br>H | Z<br>Z |
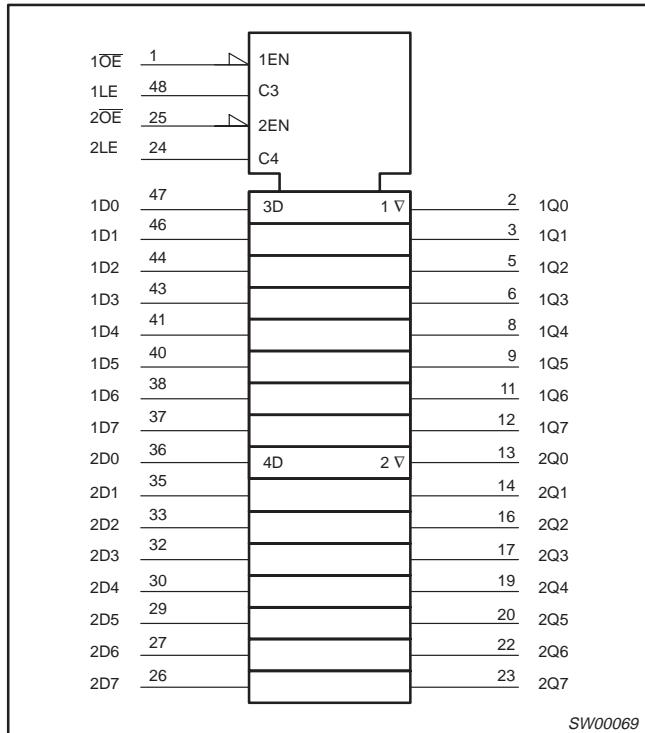
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

## LOGIC SYMBOL (IEEE/IEC)



SW00069

## 16-bit D-type transparent latch (3-State)

<div align="right">

74AC16373
74ACT16373

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### RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{CC}$ | DC supply voltage for 'AC | 2.0 | 6.0 | V |
| $V_{CC}$ | DC supply voltage for 'ACT | 4.5 | 5.5 | V |
| $V_{IN}$ | DC input voltage range | 0 | $V_{CC}$ | V |
| $V_O$ | DC output voltage range | 0 | $V_{CC}$ | V |
| $T_{amb}$ | Operating free-air temperature range | −40 | +85 | °C |
| $\Delta V/\Delta t$ | Minimum input edge rate<br>— AC devices<br>    $V_{IN}$ from 30% to 70% of $V_{CC}$<br>    $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 | | mV/ns |
| | — ACT devices<br>    $V_{IN}$ from 0.8V to 2.0V<br>    $V_{CC}$ @ 4.5V, 5.5V | 125 | | |

### ABSOLUTE MAXIMUM RATINGS[1]

in accordance with the Absolute Maximum Rating System (IEC134)
Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | −0.5 to +7.0 | V |
| $I_{IK}$ | DC input diode current | $V_{IN} = -0.5V$ | −20 | mA |
| | | $V_{IN} = V_{CC} + 0.5V$ | +20 | |
| $V_{IN}$ | DC input voltage | | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{OK}$ | DC output diode current | $V_O = -0.5V$ | −20 | mA |
| | | $V_O = V_{CC} + 0.5V$ | +20 | |
| $V_O$ | DC output voltage | | −0.5 to $V_{CC}$ +0.5 | V |
| $I_O$ | DC output source or sink current | | ± 50 | mA |
| $I_{CC}, I_{GND}$ | DC $V_{CC}$ or GND current per output | | ± 50 | mA |
| $I_{CC}, I_{GND}$ | DC $V_{CC}$ or GND current | | ± 200 | mA |
| $T_{stg}$ | Storage temperature range | | −65 to 150 | °C |
| $P_{TOT}$ | Power dissipation per package<br>– plastic mini-pack (SO)<br>– plastic shrink mini-pack (SSOP and TSSOP) | above +70°C derate linearly with 8 mW/K<br><br>above +60°C derate linearly with 5.5 mW/K | 500<br><br>500 | mW |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 16-bit D-type transparent latch (3-State)

### DC ELECTRICAL CHARACTERISTICS (74AC16373)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | TEST CONDITIONS | $V_{CC}$ (V) | LIMITS Temp = -40°C to +85°C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP[1] | MAX | |
| $V_{IH}$ | HIGH level Input voltage | $V_{OUT} = 0.1V$ or $(V_{CC} - 0.1V)$ | 3.0 | 2.1 | 1.5 | | V |
| | | | 4.5 | 3.15 | 2.25 | | |
| | | | 5.5 | 3.85 | 2.75 | | |
| $V_{IL}$ | LOW level Input voltage | $V_{OUT} = 0.1V$ or $(V_{CC} - 0.1V)$ | 3.0 | | 1.5 | 0.9 | V |
| | | | 4.5 | | 2.25 | 1.35 | |
| | | | 5.5 | | 2.75 | 1.65 | |
| $V_{OH}$ | HIGH level output voltage | $I_{OUT} = -50 \ \mu A$ | 3.0 | 2.9 | 2.99 | | V |
| | | | 4.5 | 4.4 | 4.49 | | |
| | | | 5.5 | 5.4 | 5.49 | | |
| | | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OH} = -12mA$[1] | 3.0 | 2.46 | | | V |
| | | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OH} = -24mA$[1] | 4.5 | 3.76 | | | |
| | | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OH} = -24mA$[1] | 5.5 | 4.76 | | | |
| $V_{OL}$ | LOW level output voltage | $I_{OUT} = 50 \ \mu A$ | 3.0 | | 0.01 | 0.1 | V |
| | | | 4.5 | | 0.01 | 0.1 | |
| | | | 5.5 | | 0.01 | 0.1 | |
| | | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OL} = 12mA$[1] | 3.0 | | | 0.44 | V |
| | | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OL} = 24mA$[1] | 4.5 | | | 0.44 | |
| | | $V_{IN} = V_{IL}$ or $V_{IH}$, $I_{OL} = 24mA$[1] | 5.5 | | | 0.44 | |
| $I_{IN}$ | Input leakage current | $V_{IN} = V_{CC}$, GND | 5.5 | | | ±1.0 | μA |
| $I_{OZ}$ | 3-State output OFF-state current | $V_{IN} = V_{IL}, V_{IH}$ $V_{OUT} = V_{CC}$, GND | 5.5 | | | ±2.5 | μA |
| $I_{OLD}$ | Dynamic output current[2] | $V_{OLD} = 1.65V$ max | 5.5 | 75 | | | mA |
| $I_{OHD}$ | Dynamic output current[2] | $V_{OHD} = 3.85V$ min | 5.5 | | | −75 | mA |
| $I_{CC}$ | Quiescent supply current | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 80 | μA |

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0 ms; one output loaded at a time

## 16-bit D-type transparent latch (3-State)

74AC16373
74ACT16373

### DC ELECTRICAL CHARACTERISTICS (74ACT16373)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | TEST CONDITIONS | $V_{CC}$ (V) | LIMITS | | | UNIT |
|--------|-----------|-----------------|--------------|--------|--------|--------|------|
| | | | | Temp = -40°C to +85°C | | | |
| | | | | MIN | TYP[1] | MAX | |
| $V_{IH}$ | HIGH level Input voltage | $V_{OUT}$ = 0.1V or ($V_{CC}$ − 0.1V) | 4.5 | 2.0 | 1.5 | | V |
| | | | 5.5 | 2.0 | 1.5 | | |
| $V_{IL}$ | LOW level Input voltage | $V_{OUT}$ = 0.1V or ($V_{CC}$ − 0.1V) | 4.5 | | 1.5 | 0.8 | V |
| | | | 5.5 | | 1.5 | 0.8 | |
| $V_{OH}$ | HIGH level output voltage | $I_{OUT}$ = −50 µA | 4.5 | 4.4 | 4.49 | | V |
| | | | 5.5 | 5.4 | 5.49 | | |
| | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = −24mA[1] | 4.5 | 3.76 | 3.86 | | V |
| | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OH}$ = −24mA[1] | 5.5 | 4.76 | 4.86 | | |
| $V_{OL}$ | LOW level output voltage | $I_{OUT}$ = 50 µA | 4.5 | | 0.01 | 0.1 | V |
| | | | 5.5 | | 0.01 | 0.1 | |
| | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OL}$ = 24mA[1] | 4.5 | | | 0.44 | V |
| | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$, $I_{OL}$ = 24mA[1] | 5.5 | | | 0.44 | |
| $I_{IN}$ | Input leakage current | $V_{IN}$ = $V_{CC}$, GND | 5.5 | | | ± 1.0 | µA |
| $I_{OZ}$ | 3-State output OFF-state current | $V_{IN}$ = $V_{IL}$, $V_{IH}$ $V_{OUT}$ = $V_{CC}$, GND | 5.5 | | | ± 2.5 | µA |
| $\Delta I_{CC}$ | Additional quiescent supply current per input pin | $V_{IN}$ = $V_{CC}$ − 2.1V Other inputs at $V_{CC}$ or GND; $I_{OUT}$ = 0 | 5.5 | | | 1.0 | mA |
| $I_{OLD}$ | Dynamic output current[2] | $V_{OLD}$ = 1.65V max | 5.5 | 75 | | | mA |
| $I_{OHD}$ | Dynamic output current[2] | $V_{OHD}$ = 3.85V min | 5.5 | | | −75 | mA |
| $I_{CC}$ | Quiescent supply current | $V_{IN}$ = $V_{CC}$ or GND | 5.5 | | | 80 | µA |

**NOTES:**
1. All outputs loaded
2. Maximum test duration 2.0ms, one output loaded at a time
In accordance with the Absolute Maximum Rating System (IEC 134)

## 16-bit D-type transparent latch (3-State)

### AC CHARACTERISTICS (74AC16373)

GND = 0V; $t_r$ = $t_f$ = 2.5ns; $C_L$ = 50pF; $R_L$ = 500Ω; .

| SYMBOL | PARAMETER | $V_{CC}$[1] | LIMITS | | | | | UNIT | WAVEFORM |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C | | | $T_{amb}$ = −40°C to +85°C | | | |
| | | | MIN | TYP | MAX | MIN | MAX | | |
| $t_{PLH}$ | Propagation delay $D_n$ to $Q_n$ | 3.3 / 5.0 | 2.0 / 1.5 | 3.6 / 2.5 | 9 / 7 | 1.5 / 1.0 | 10 / 8 | ns | 1, 3 |
| $t_{PHL}$ | Propagation delay $D_n$ to $Q_n$ | 3.3 / 5.0 | 2.0 / 1.5 | 3.8 / 2.6 | 9 / 7 | 1.5 / 1.0 | 10 / 8 | ns | 1, 3 |
| $t_{PLH}$ | Propagation delay LE to $Q_n$ | 3.3 / 5.0 | 2.0 / 1.5 | 4.2 / 2.8 | 9 / 7 | 1.5 / 1.0 | 10 / 8 | ns | 1, 3 |
| $t_{PHL}$ | Propagation delay LE to $Q_n$ | 3.3 / 5.0 | 2.0 / 1.5 | 4.0 / 2.7 | 9 / 7 | 1.5 / 1.0 | 10 / 8 | ns | 1, 3 |
| $t_{PZH}$ | 3-State output enable time $\overline{OE}$ to $Q_n$ | 3.3 / 5.0 | 2.0 / 1.5 | 4.7 / 3.2 | 9 / 7 | 1.5 / 1.0 | 10 / 8 | ns | 2, 3 |
| $t_{PZL}$ | 3-State output enable time $\overline{OE}$ to $Q_n$ | 3.3 / 5.0 | 2.0 / 1.5 | 4.7 / 3.2 | 9 / 7 | 1.5 / 1.0 | 10 / 8 | ns | 2, 3 |
| $t_{PHZ}$ | 3-State output disable time $\overline{OE}$ to $Q_n$ | 3.3 / 5.0 | 2.0 / 1.5 | 3.5 / 2.4 | 8 / 6 | 1.5 / 1.0 | 9 / 7 | ns | 2, 3 |
| $t_{PLZ}$ | 3-State output disable time $\overline{OE}$ to $Q_n$ | 3.3 / 5.0 | 2.0 / 1.5 | 4.3 / 2.9 | 8 / 6 | 1.5 / 1.0 | 9 / 7 | ns | 2, 3 |
| $t_w$ | LE pulse width HIGH | 3.3 / 5.0 | 4.0 / 3.5 | 1.6 / 1.4 | | 4.5 / 4.0 | | ns | 2 |
| $t_{su}$ | Set-up time $D_n$ to LE | 3.3 / 5.0 | 1.0 / 1.0 | 0.3 / 0.2 | | 1.5 / 1.5 | | ns | 4 |
| $t_h$ | Hold time $D_n$ to LE | 3.3 / 5.0 | 1.0 / 1.0 | 0.3 / 0.2 | | 1.5 / 1.5 | | ns | 4 |

**NOTE:**
1. Voltage range 3.3V is $V_{CC}$ = 3.3V ± 0.3V
   Voltage range 5.0V is $V_{CC}$ = 5.0V ± 0.5V

### AC CHARACTERISTICS (74ACT16373)

GND = 0V; $t_r$ = $t_f$ = 2.5ns; $C_L$ = 50pF; $R_L$ = 500Ω; .

| SYMBOL | PARAMETER | $V_{CC}$[1] | LIMITS | | | | | UNIT | WAVEFORM |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C | | | $T_{amb}$ = −40°C to +85°C | | | |
| | | | MIN | TYP | MAX | MIN | MAX | | |
| $t_{PLH}$ | Propagation delay $D_n$ to $Q_n$ | 5.0 | 2.0 | 3.9 | 9 | 1.5 | 10 | ns | 1, 3 |
| $t_{PHL}$ | Propagation delay $D_n$ to $Q_n$ | 5.0 | 2.0 | 3.6 | 9 | 1.5 | 10 | ns | 1, 3 |
| $t_{PLH}$ | Propagation delay LE to $Q_n$ | 5.0 | 2.0 | 4.4 | 9 | 1.5 | 10 | ns | 1, 3 |
| $t_{PHL}$ | Propagation delay LE to $Q_n$ | 5.0 | 2.0 | 4.3 | 9 | 1.5 | 10 | ns | 1, 3 |
| $t_{PZH}$ | 3-State output enable time $\overline{OE}$ to $Q_n$ | 5.0 | 2.0 | 4.2 | 9 | 1.5 | 10 | ns | 2, 3 |
| $t_{PZL}$ | 3-State output enable time $\overline{OE}$ to $Q_n$ | 5.0 | 2.0 | 4.2 | 9 | 1.5 | 10 | ns | 2, 3 |
| $t_{PHZ}$ | 3-State output disable time $\overline{OE}$ to $Q_n$ | 5.0 | 2.0 | 4.0 | 8 | 1.5 | 9 | ns | 2, 3 |
| $t_{PLZ}$ | 3-State output disable time $\overline{OE}$ to $Q_n$ | 5.0 | 2.0 | 4.4 | 8 | 1.5 | 9 | ns | 2, 3 |
| $t_w$ | LE pulse width HIGH | 5.0 | 4 | 1.2 | | 4.5 | | ns | 2 |
| $t_{su}$ | Set-up time $D_n$ to LE | 5.0 | 1.0 | 0 | | 1.5 | | ns | 4 |
| $t_h$ | Hold time $D_n$ to LE | 5.0 | 1.5 | 0.4 | | 2 | | ns | 4 |

**NOTE:**
1. These values are at $V_{CC}$ = 5.0V ± 0.5V
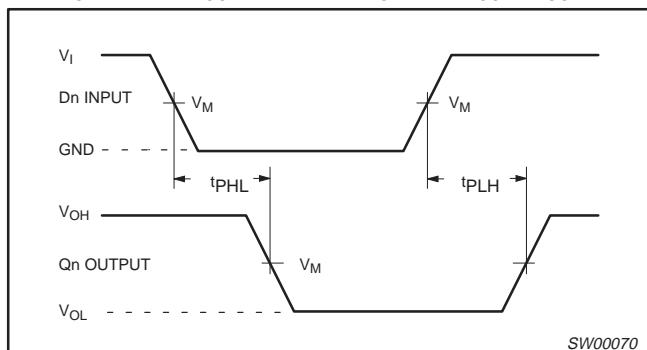
# 16-bit D-type transparent latch (3-State)
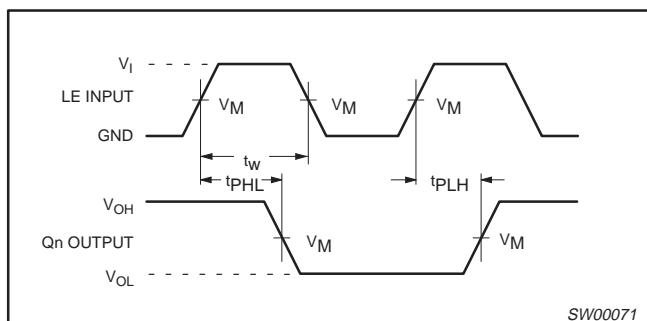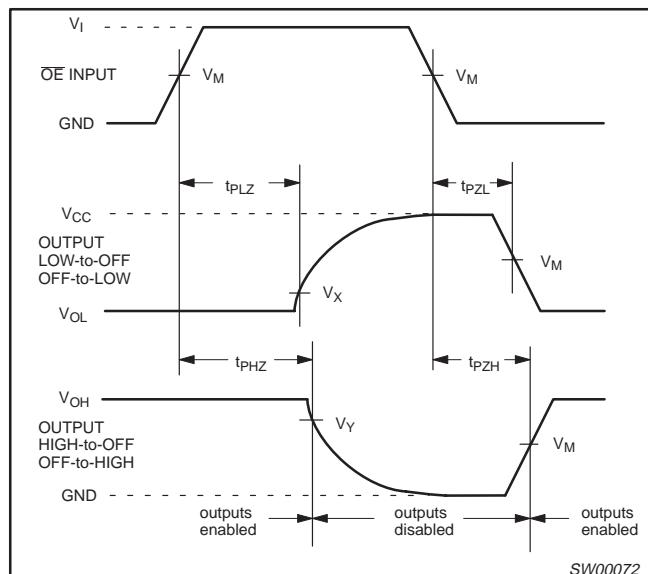
## AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5\ V_{CC}$ at $V_{CC} < 2.7V$.
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1\ V_{CC}$ at $V_{CC} < 2.7V$
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1\ V_{CC}$ at $V_{CC} < 2.7V$



SW00070
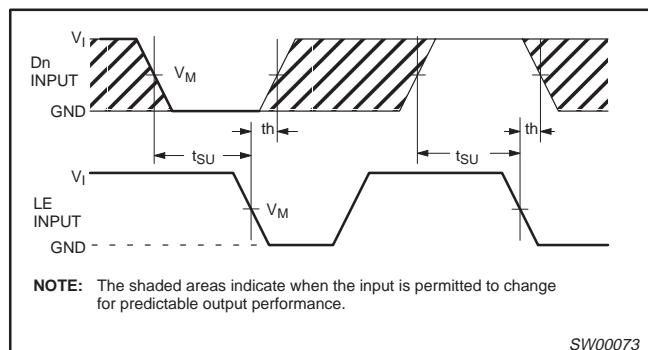
**Waveform 1.   Input (Dn) to output (Qn) propagation delays**



SW00071

**Waveform 2.   Latch enable input (LE) pulse width and the latch enable input to output (Qn) propagation delays**



SW00072

**Waveform 3.   3-State enable and disable times**



**NOTE:** The shaded areas indicate when the input is permitted to change for predictable output performance.

SW00073
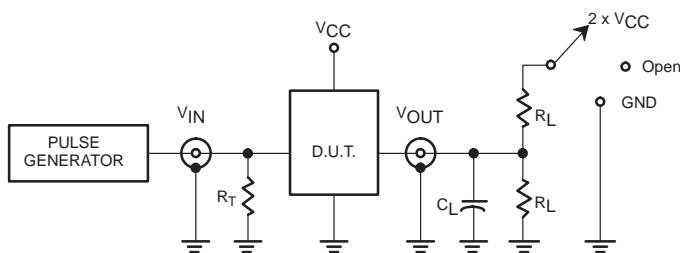
**Waveform 4.   Data set-up and hold times for the Dn input to the LE input**

## TEST CIRCUIT



Test Circuit for 3-State Outputs

### SWITCH POSITION

| TEST | SWITCH |
|------|--------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| FAMILY | $V_{IN}$ Input Requirements | $V_m$ Input | $V_m$ Output |
|--------|----------------------------|-------------|--------------|
| AC | GND to $V_{CC}$ | 50% $V_{CC}$ | 50% $V_{CC}$ |
| ACT | GND to 3.0V | 1.5V | 50% $V_{CC}$ |

### DEFINITIONS

$R_L$ = Load resistor; see AC Characteristics for value.

$C_L$ = Load capacitance, see AC characteristics

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

SV00302
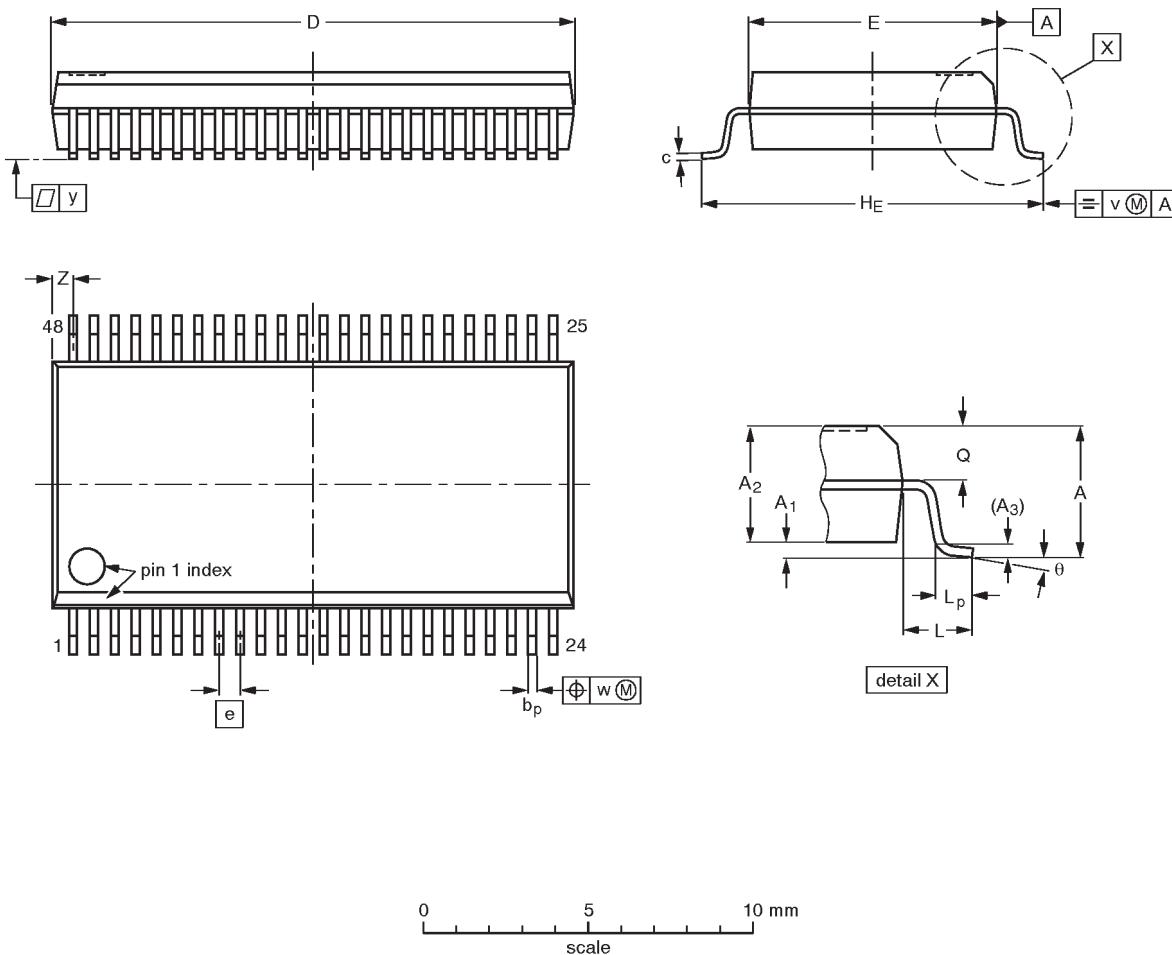
**Waveform 5.  Load circuitry for switching times**

16-bit D-type transparent latch (3-State)

74AC16373
74ACT16373

SSOP48:   plastic shrink small outline package; 48 leads; body width 7.5 mm                    SOT370-1

pin 1 index

detail X

0          5          10 mm
scale

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D (1) | E (1) | e | H_E | L | Lₚ | Q | v | w | y | Z (1) | θ |
|------|--------|----|----|----|----|----|-------|-------|---|-----|---|----|---|---|---|---|-------|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 16.00<br>15.75 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
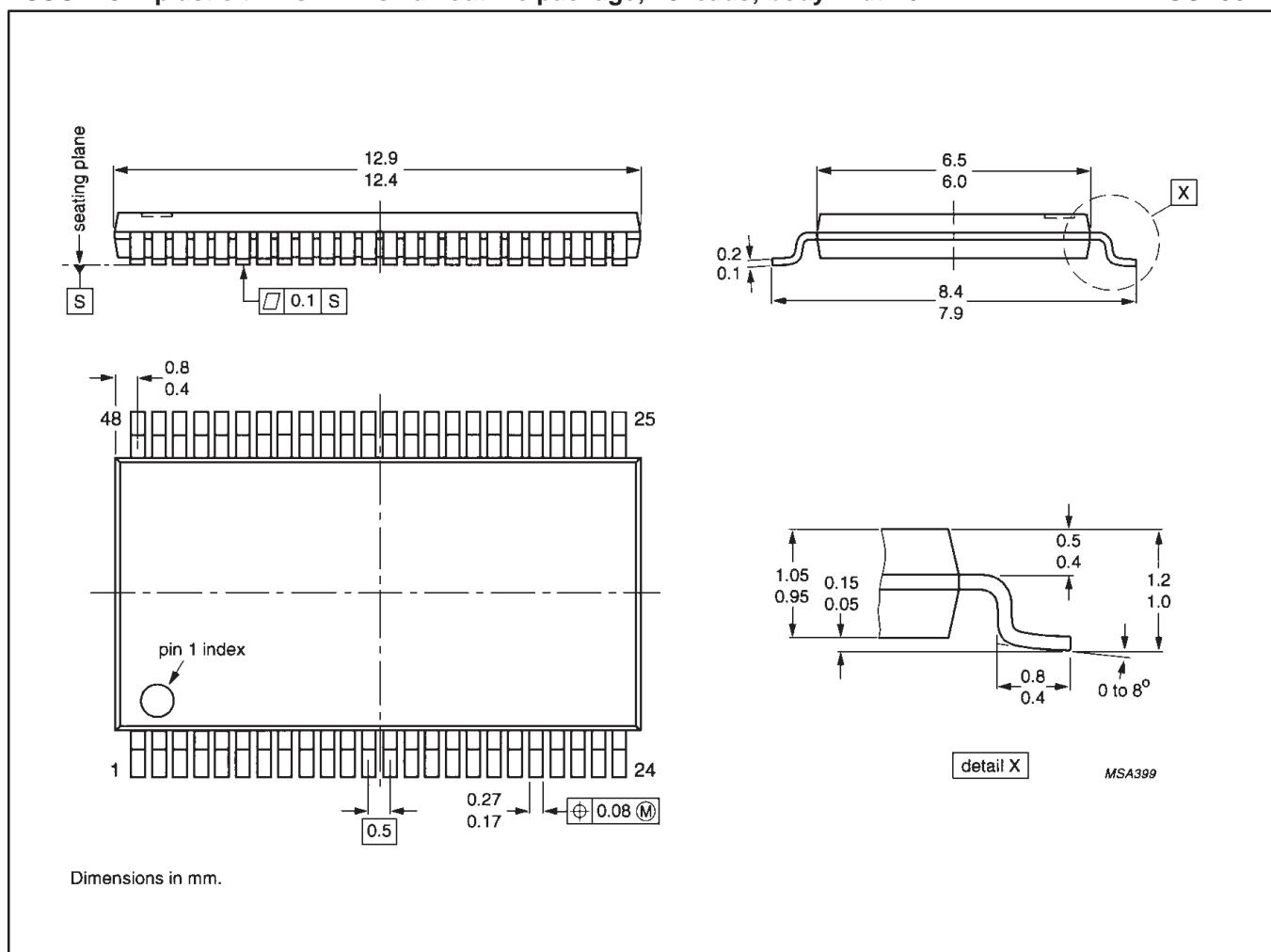
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|---|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT370-1 | | MO-118AA | | | | ~~93-11-02~~<br>95-02-04 |

**TSSOP48:** **plastic thin shrink small outline package; 48 leads; body width 6.1mm**     **SOT362-1**



Dimensions in mm.

**NOTES**

16-bit D-type transparent latch (3-State)                                                           **74AC16373**
                                                                                                                        **74ACT16373**

## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | **Formative or in Design** | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | **Preproduction Product** | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| *Product Specification* | **Full Production** | This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product. |