TEXAS INSTR (ASIC/MEMORY)   25E D
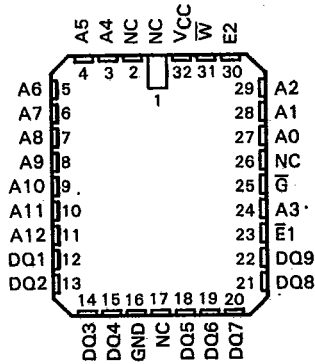
- 8192 × 9 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2-Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  '69CE72-25 . . . 25 ns
  '69CE72-35 . . . 35 ns
  '69CE72-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- 3-State Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  − Active . . . 660 mW MAX
  − Standby . . . 55 mW MAX (TTL Inputs)
  − Standby . . . 5.5 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  − SM Prefix . . . Standard Processing
  − SMJ Prefix . . . Class B Processing
- Output Enable for Bus Control
- Two Chip-Enable Pins for Increased Flexibility
- Packaging Options:
  − 28-Pin Ceramic 300-mil DIP
  − 32-Pad Leadless Ceramic Chip Carrier

JD PACKAGE T-46-23-12
(TOP VIEW)

FG PACKAGE
(TOP VIEW)

PIN NOMENCLATURE	
A0-A12	Address Inputs
DQ1-DQ9	Data In/Data Out
$\overline{E1}$	Chip Enable/Power Down
E2	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

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description

The '69CE72 is a common I/O, 73,728-bit static random-access memory organized as 8192 words by 9 bits. Bit nine is generally used for parity bit storage for improved system reliability. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array. Access time from chip enable or address is available for 25, 35, or 45 ns cycle times, while maximum power dissipation is less than 660 mW. This reduces to 55 mW (TTL Inputs) or 5.5 mW (CMOS Inputs) during standby operation.

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The '69CE72's static design and control signals ($\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The two enable pins add flexibility and simplify memory expansion/design. The output-enable pin minimizes bus contention problems.

The '69CE72 static RAM provides single 5-V operation with all inputs and outputs fully compatible with standard TTL and CMOS voltage levels.

operation

addresses (A0-A12)

The 13 address inputs select one of the 8192 9-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL without external pull-up resistors.

chip enable/power down ($\overline{E}1$)

The chip enable/power down terminal ($\overline{E}1$) can be driven directly by standard TTL circuits, and affects the powerdown/deselect function of the chip. Whenever $\overline{E}1$ is high (disabled), the device is put into a reduced power standby mode. Data is retained during the standby mode.

chip enable (E2)

The chip enable terminal (E2) affects the chip deselect function. Whenever chip enable (E2) is high (enabled), and chip enable/powerdown ($\overline{E}1$) is low (enabled) the device is operational, and data may be written or read provided input and output terminals are enabled. Whenever chip enable (E2) is low and chip enable/powerdown ($\overline{E}1$) is low, the device is in the powered-up deselected state.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}1$ must be high or E2 must be low when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.
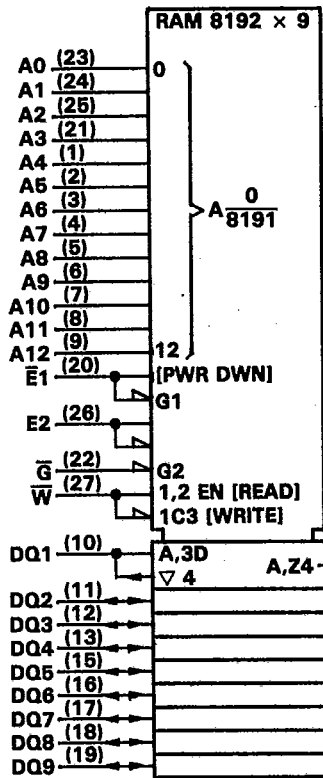
output enable ($\overline{G}$)

The output-enable terminal, which can be driven directly from standard TTL circuits, affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

data in/data out (DQ1-DQ9)

Data can be written into a selected device when the write-enable ($\overline{W}$) input is low, chip enable/powerdown ($\overline{E}1$) is low, and chip enable (E2) is high. Data can be read when write enable ($\overline{W}$) is high, chip enable/powerdown ($\overline{E}1$) is low, chip enable (E2) is high, and output enable ($\overline{G}$) is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffers provide direct TTL compatibility with a fanout of twenty Series 54LS or 54ALS TTL gates, sixteen Series 54AS TTL gates, or thirteen Series 54F TTL gates.

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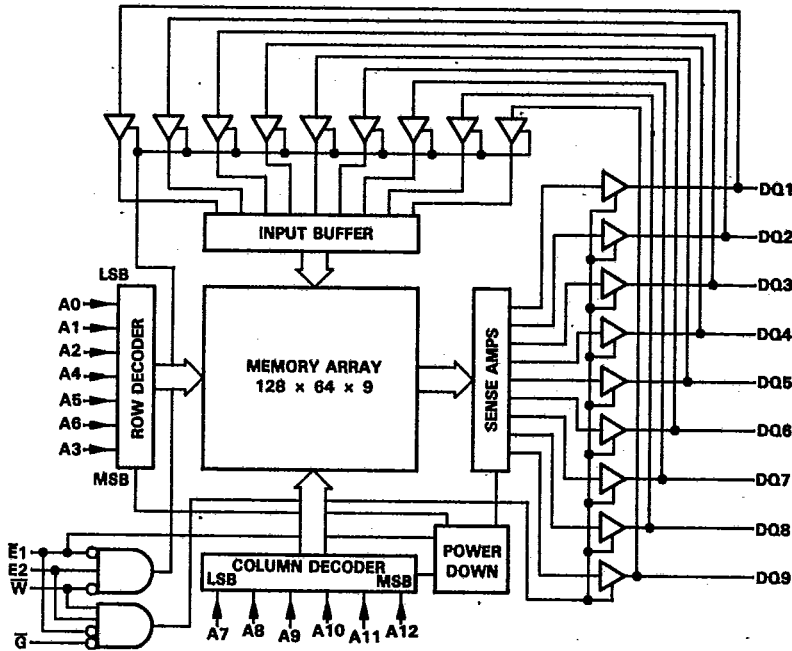POST OFFICE BOX 225012 ● DALLAS, TEXAS 75265

logic symbol†

FUNCTION TABLE

$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	Input/Outputs	Mode
H	X	X	X	High Z	Deselect Power Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

X = Don't Care.

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and
IEC Publication 617-12.
Pin numbers shown are for the JD package.

TEXAS INSTR (ASIC/MEMORY) 25E D

functional block diagram

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data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† Vcc @ 2.0 V	TYP† Vcc @ 3.0 V	MAX Vcc @ 2.0 V	MAX Vcc @ 3.0 V	UNIT
V_{DR}	Vcc for data retention		2.0	—	—	—	—	V
I_{CCDR}	Data retention current	$\overline{E1} \geq V_{CC} - 0.2$ V,		3	5	100	200	μA
t_{CDR}§	Chip deselect to data retention time	$V_{IN} \geq V_{CC} - 0.2$ V,	0	—		—		ns
t_R§	Operation recovery time	or $\leq$ GND + 0.2 V	$t_{c(RD)}$‡	—		—		ns
I_{LI}§	Input leakage current			—		1		μA

†TYP values listed are typical values at 25°C.
‡$t_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) .... −0.5 V to 7 V
Input voltage range (see Note 2) .... −1 V to 7 V
Output voltage range in high-impedance state .... −0.5 V to 7 V
Output current .... 20 mA
Minimum operating free-air temperature .... −55°C
Maximum operating case-temperature .... 125°C
Storage temperature range .... −65°C to 150°C
Latch-up current .... 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
        2. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device input.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		V_{CC}+1	V
V_{IL}	Low-level input voltage (see Note 3)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

NOTE 3: V_{IL} (min) for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device input.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'69CE72-25			'69CE72-35			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)	0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	−10		10	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = 5.5 V, I_O = 0 mA			130			120	mA
I_{CCI} V_{CC} supply current (standby)	TTL-level inputs	$\overline{E1}$ ≥ V_{IH}, V_{CC} = 5.5 V			10			10	mA
	CMOS-level inputs	$\overline{E1}$ = V_{CC}±0.3, V_{CC} = 5.5 V			0.9			0.9	

PARAMETER		TEST CONDITIONS	'69CE72-45			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)	0 V ≤ V_I ≤ V_{CC}	−10		10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI} V_{CC} supply current (standby)	TTL-level inputs	$\overline{E1}$ ≥ V_{IH}, V_{CC} = 5.5 V			10	mA
	CMOS-level inputs	$\overline{E1}$ = V_{CC}±0.3, V_{CC} = 5.5 V			0.9	

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capacitance, $T_A = 25°C$, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	$T_A = 25°C$, f = 1 MHz, V_{CC} = 5 V			6	pF
C_o	Output capacitance				7	

†Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'69CE72-25			'69CE72-35			'69CE72-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	15			20			25			ns
$t_{su(E1)}$	Chip-enable 1 low to end of write	20			30			40			ns
$t_{su(E2)}$	Chip-enable 2 high to end of write	15			20			25			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			20			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			0			ns
t_{PU}	Delay time, chip-enable E1 low to power up‡	0			0			0			ns
t_{PD}	Delay time, chip-enable E1 high to power down ‡			20			20			25	ns
t_{AW}	Address setup to write end	25			30			40			ns

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'69CE72-25		'69CE72-35		'69CE72-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address			25		35		45	ns
$t_{a(E1)}$	Access time from chip enable E1 low	R1 = 481 Ω, R2 = 255 Ω		25		35		45	ns
$t_{a(E2)}$	Access time from chip enable E2 high	C_L = 30 pF,		20		25		30	
$t_{a(G)}$	Access time from output enable low	See Figure 1a		15		20		20	ns
$t_{v(A)}$	Output data valid after address change		3		3		3		ns
$t_{en(W)}$	Output enable time from write enable high		0		0		3		ns
$t_{en(E1)}$	Output enable time from chip enable E1 low		0		0		3		ns
$t_{en(E2)}$	Output enable time from chip enable E2 high	R1 = 481, R2 = 255 Ω,	0		0		3		ns
$t_{en(G)}$	Output enable time from output enable low	C_L = 5 pF,	0		0		0		ns
$t_{dis(E1)}$	Output disable time from chip enable E1 high	See Figure 1b and		15		15		20	ns
$t_{dis(E2)}$	Output disable time from chip enable E2 low	Note 4		15		15		20	ns
$t_{dis(W)}$	Output disable time from write enable low			10		15		20	ns
$t_{dis(G)}$	Output disable time from output enable high			10		15		20	ns

‡This parameter is guaranteed but not tested.
NOTE 4:   Transition is measured ± 500 mV from steady state voltage. This parameter is guaranteed but not tested.

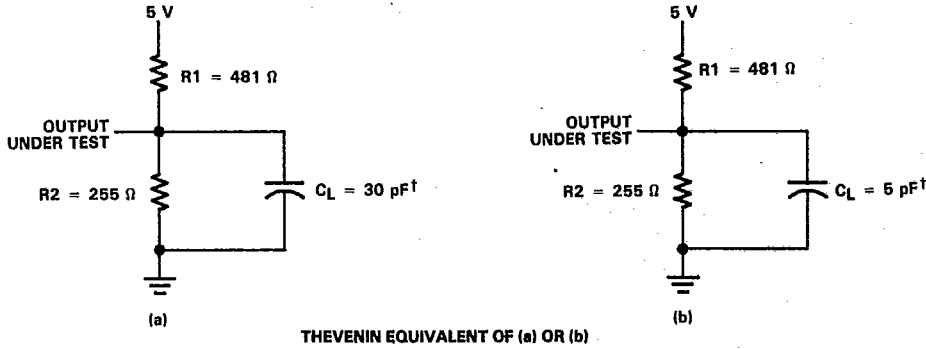ADVANCE INFORMATION

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PARAMETER MEASUREMENT INFORMATION

†C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT

‡t_r and $t_f \leq 5$ ns.
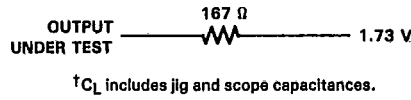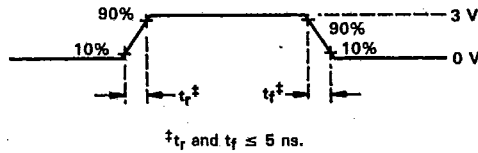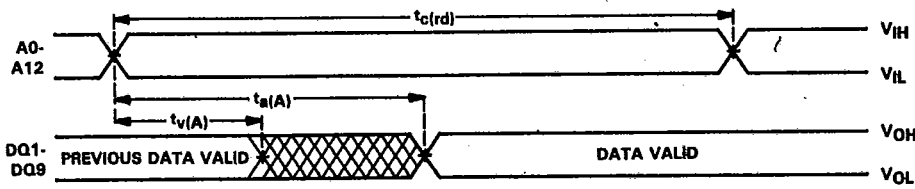
FIGURE 2. TRANSITION TIMES

NOTE 5:   All switching characteristics and timing requirements assume test conditions as depicted in Figures 1 and 2 with timing references of 1.5 V (50% reference point) as shown in subsequent timing diagrams.
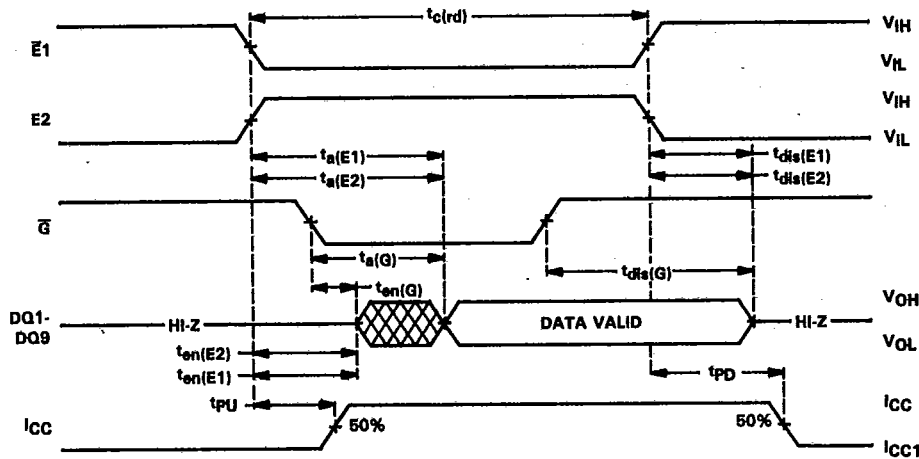
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read cycle timing from address†

†$\overline{W}$ is high, and $\overline{E}$ is low.

read cycle timing from chip enable‡

‡$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.
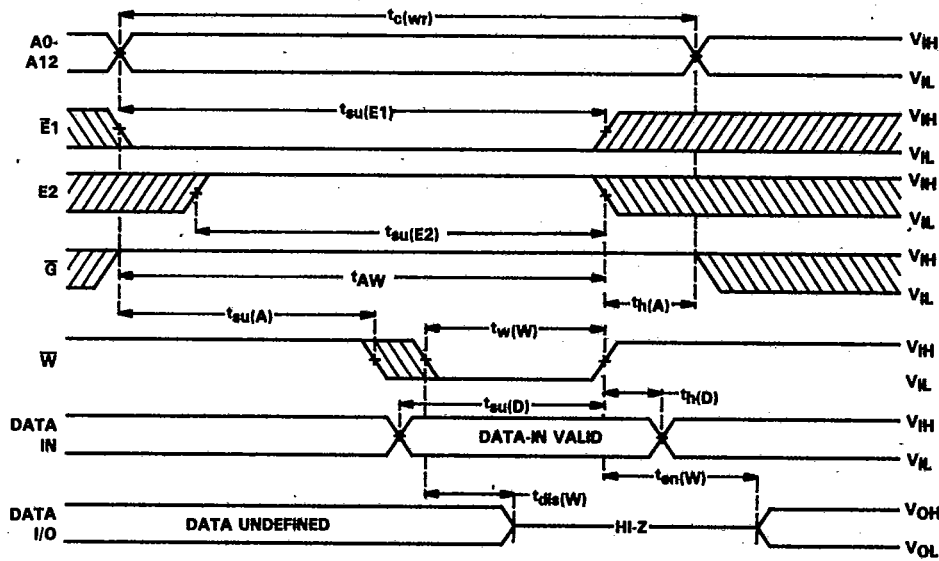
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write cycle timing controlled by write enable†
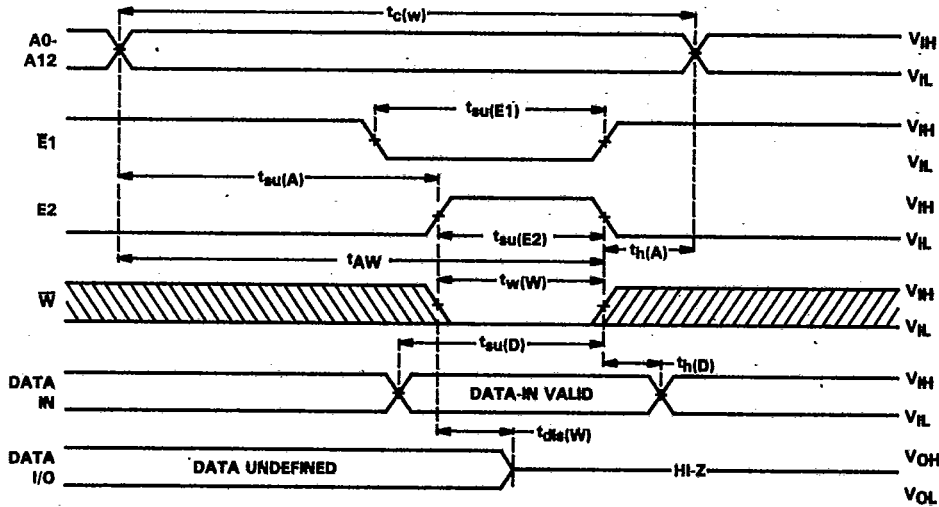

†E or W̄ must be high during address transitions.
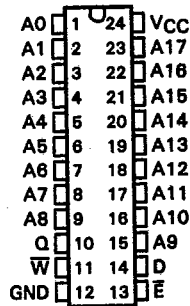
write cycle timing controlled by chip enable†

†E or W̄ must be high during address transitions.

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SM61CD256, SMJ61CD256
262,144 BY 1-BIT STATIC RAMS

TEXAS INSTR (ASIC/MEMORY)   25E D   DECEMBER 1987—REVISED FEBRUARY 1988

T-46-23-05

- 262,144 × 1 Organization
- Separate I/O
- Military Temperature Range . . . –55°C to 125°C (M Suffix)
- Fast Static Operation
- Maximum Access Time from Address or Chip Enable
  '61CD256-35 . . . 35 ns
  '61CD256-45 . . . 45 ns
  '61CD256-55 . . . 55 ns
- Single 5-V Supply (10% Tolerance)
- Automatic Powerdown when Deselected
- 3-State Output
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Low Power Dissipation (V_{CC} = 5.5 V)
  —Active . . . 660 mW MAX
  —Standby . . . 27.5 mW MAX (TTL Inputs)
  —Standby . . .1.1 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  —SM Prefix . . . Standard Processing
  —SMJ Prefix . . . Class B Processing
- Packaging Options:
  —24-Pin Ceramic 300-mil DIP
  —28-Pad Leadless Ceramic Chip Carrier
- Chip Enable Pin for Memory Expansion and Standby Operation

JD PACKAGE
(TOP VIEW)

```
         _____
A0  [ 1    24 ] VCC
A1  [ 2    23 ] A17
A2  [ 3    22 ] A16
A3  [ 4    21 ] A15
A4  [ 5    20 ] A14
A5  [ 6    19 ] A13
A6  [ 7    18 ] A12
A7  [ 8    17 ] A11
A8  [ 9    16 ] A10
Q   [ 10   15 ] A9
W   [ 11   14 ] D
GND [ 12   13 ] E
```

PIN NOMENCLATURE	
A0-A17	Address Inputs
D	Data Input
Q	Data Output
E	Chip Enable/Power Down
GND	Ground
VCC	5-V Supply
W	Write Enable

description

The '61CD256 is a separate I/O, 262,144-bit static random-access memory organized as 262,144 words by 1 bit. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six-transistor cell) memory array. The six-transistor cell provides inherently lower soft error rates, improved stability over the operating temperature range, and very low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

The '61CD256's static design and control signals (E̅ and W̅) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin provides for easy memory expansion and for automatic power-down. This feature, in conjunction with the full CMOS array, provides for very low standby power operation when the memory is deselected, greatly reducing the overall memory power requirements.

Access time from either address or chip enable is a maximum of 35, 45, or 55 ns, allowing speed enhancements for new and existing designs.

PRODUCT PREVIEW

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