QUALITY SEMICONDUCTOR, INC.

3.3V Low Skew CMOS PLL Clock Driver With Integrated Loop Filter

FEATURES/BENEFITS

- JEDEC compatible LVTTL level
- Clock inputs are 5V tolerant
- < 300ps output skew, Q0-Q4
- 2xQ output, Q outputs, $\overline{Q}$ output, Q/2 output
- Outputs 3-state and reset while OE/$\overline{RST}$ low
- PLL disable feature for low frequency testing
- Internal loop filter RC network
- Pin compatible MC88LV915, IDT74FCT388915
- Positive or negative edge synchronization ($\overline{PE}$)
- Balanced drive outputs ±24mA
- 160MHz maximum frequency (2xQ output)
- Industrial temperature range
- Available in space saving QSOP and PLCC packages

DESCRIPTION

The QS5LV919 Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to one of two reference clock inputs. Eight outputs are available: 2xQ, Q0-Q4, $\overline{Q5}$, Q/2. Careful layout and design ensure < 300 ps skew between the Q0-Q4, and Q/2 outputs. The QS5LV919 includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The PLL can also be disabled by the PLL_EN signal to allow low frequency or DC testing. The LOCK output asserts to indicate when phase lock has been achieved. The QS5LV919 is designed for use in high-performance workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks.

For more information on PLL clock driver products, see Application Note AN-22A.

Figure 1. Functional Block Diagram

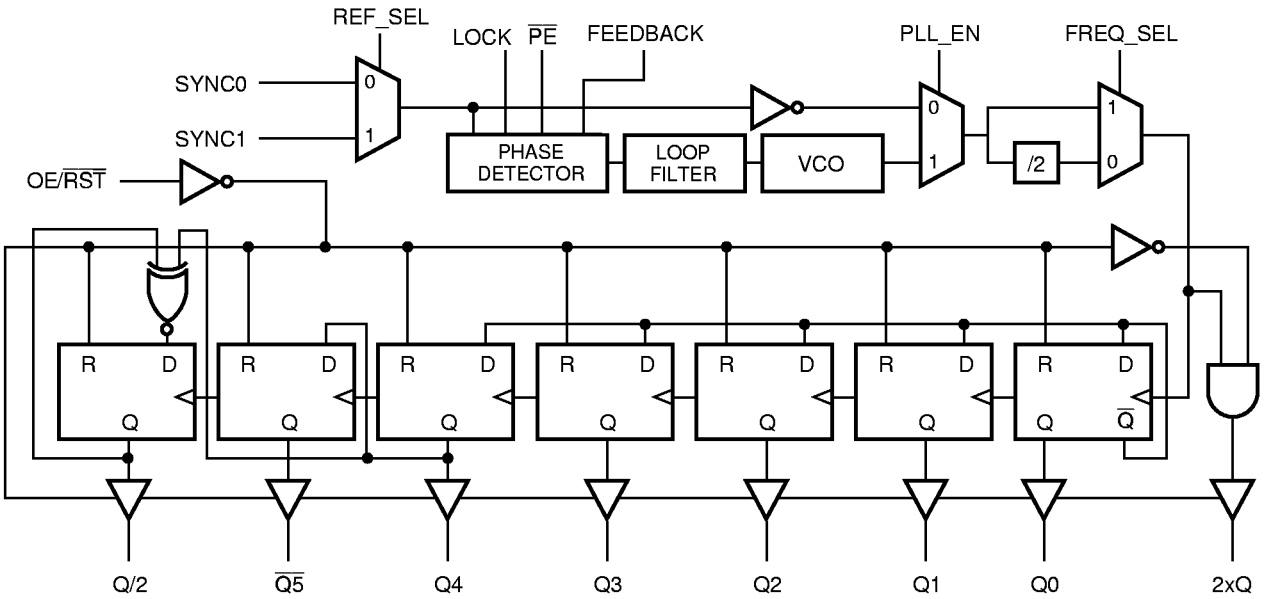


Figure 2. Pin Configuration (All Pins Top View)

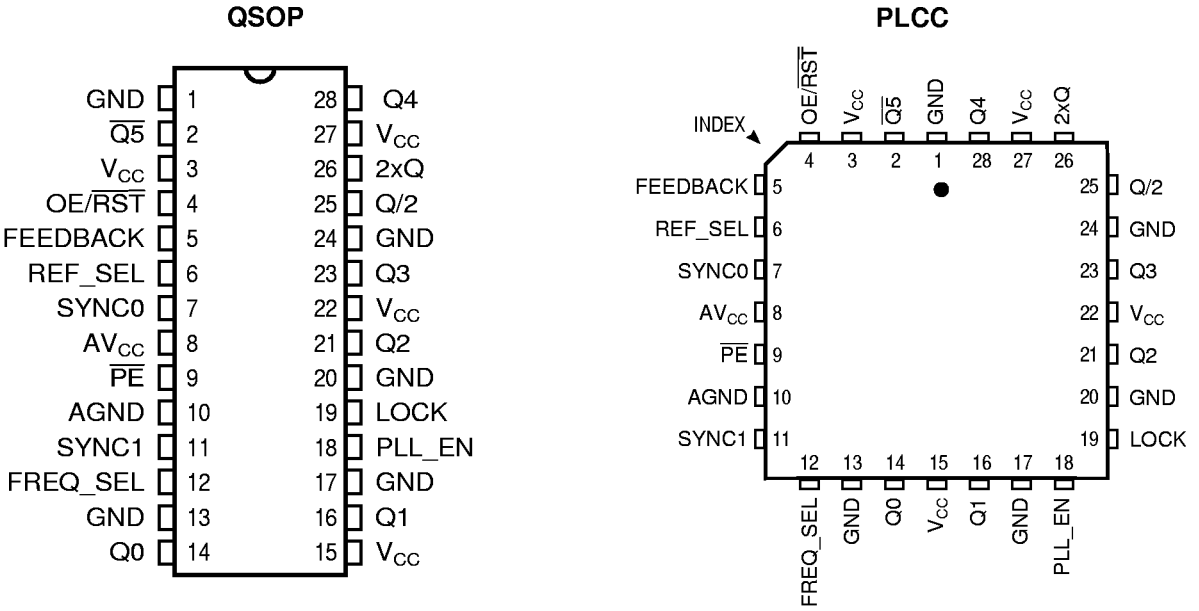


Table 1. Pin Description

Pin Name	I/O	Functional Description
SYNC0	I	Reference clock input.
SYNC1	I	Reference clock input.
REF_SEL	I	Reference clock select. When 1, selects SYNC1. When 0, selects SYNC0.
FREQ_SEL	I	VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency.
FEEDBACK	I	PLL feedback input which is connected to a user selected output pin. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information.
Q0-Q4	O	Clock outputs.
$\overline{Q5}$	O	Clock output. Matched in frequency, but inverted with respect to Q.
2xQ	O	Clock output. Matched in phase, but frequency is double the Q frequency.
Q/2	O	Clock output. Matched in phase, but frequency is half the Q frequency.
LOCK	O	PLL lock indication signal. 1 indicates positive lock. 0 indicates that the PLL is not locked and outputs may not be synchronized to the inputs.
OE/$\overline{RST}$	I	Output enable/asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled.
PLL_EN	I	PLL enable. Enables and disables the PLL. Useful for testing purposes.
$\overline{PE}$	I	When $\overline{PE}$ is LOW, outputs are synchronized with the positive edge of SYNC. When HIGH, outputs are synchronized with the negative edge of SYNC.
V_{CC}	—	Power supply for output buffers.
AV_{CC}	—	Power supply for phase lock loop and other internal circuitries.
GND	—	Ground supply for output buffers.
AGND	—	Ground supply for phase lock loop and other internal circuitries.

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Input Voltage V_{IN}	–0.5V to 5.5V
Maximum Power Dissipation At T_A = 85°C, QSOP	655mW
PLCC	770mW
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Output Frequency Specifications

Industrial: T_A = –40°C to 85°C, V_{CC} = 3.3 ±0.3V

Symbol	Description	–55	–70	–100	–133	–160	Units
F_{MAX_2xQ}	Max Frequency, 2xQ	55	70	100	133	160	MHz
F_{MAX_Q}	Max Frequency, Q0-Q4, $\overline{Q5}$	27.5	35	50	66.5	80	MHz
$F_{MAX\_Q/2}$	Max Frequency, Q/2	13.75	17.5	25	33.25	40	MHz
F_{MIN_2xQ}	Min Frequency, 2xQ	20	20	20	20	20	MHz
F_{MIN_Q}	Min Frequency, Q0-Q4, $\overline{Q5}$	10	10	10	10	10	MHz
$F_{MIN\_Q/2}$	Min Frequency, Q/2	5	5	5	5	5	MHz

Table 4. Frequency Selection Table

FREQ_SEL	Output Used for Feedback	SYNC (MHz) (allowable Range)[1] Min	Max	Output Frequency Relationship Q/2	$\overline{Q5}$	Q0-Q4	2xQ
HIGH	Q/2	$F_{MIN\_Q/2}$	$F_{MAX\_Q/2}$	SYNC	–SYNC x 2	SYNC x 2	SYNC x 4
HIGH	Q0-Q4	F_{MIN_Q}	F_{MAX_Q}	SYNC/2	–SYNC	SYNC	SYNC x 2
HIGH	$\overline{Q5}$	F_{MIN_Q}	F_{MAX_Q}	–SYNC/2	SYNC	–SYNC	–SYNC x 2
HIGH	2xQ	F_{MIN_2xQ}	F_{MAX_2xQ}	SYNC/4	–SYNC/2	SYNC/2	SYNC
LOW	Q/2	$F_{MIN\_Q/2}$/2	$F_{MAX\_Q/2}$/2	SYNC	–SYNC x 2	SYNC x 2	SYNC x 4
LOW	Q0-Q4	F_{MIN_Q}/2	F_{MAX_Q}/2	SYNC/2	–SYNC	SYNC	SYNC x 2
LOW	$\overline{Q5}$	F_{MIN_Q}/2	F_{MAX_Q}/2	–SYNC/2	SYNC	–SYNC	–SYNC x 2
LOW	2xQ	F_{MIN_2xQ}/2	F_{MAX_2xQ}/2	SYNC/4	–SYNC/2	SYNC/2	SYNC

Note:

1. Operation in the specified SYNC frequency range guarantees that the VCO will operate in its optimal range of 20MHz to F_{MAX_2xQ}. Operation with Sync inputs outside specified frequency ranges may result in out-of-lock outputs. FREQ_SEL only affects VCO frequency and does not affect output frequencies.

Table 5. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

Pins	QSOP Typ	QSOP Max	PLCC Typ	PLCC Max	Unit
C_{IN}	3	4	4	6	pF

Note: Capacitance is characterized but not tested.

Table 6. DC Electrical Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 3.3 ±0.3V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –24mA I_{OH} = –100µA	V_{CC} –0.60 V_{CC} –0.20			V V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 24mA V_{CC} = Min., I_{OL} = 100µA			0.45 0.2	V V
V_H	Input Hysteresis			100		mV
$\|I_{OZ}\|$	Output Leakage Current	V_{OUT} = V_{CC} or V_{OUT} = GND, V_{CC} = Max.			5	µA
$\|I_{IN}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = V_{CC} or V_{IN} = GND			5	µA
$\|I_{PD}\|$	Input Pull-down Current ($\overline{PE}$)	V_{CC} = Max., V_{IN} = V_{CC}			100	µA

Table 7. Power Supply Characteristics

Industrial: T_A = –40°C to 85°C, V_{CC} = 3.3 ±0.3V

Symbol	Parameter	Test Conditions	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max, OE/$\overline{RST}$ = Low, SYNC = Low, All outputs unloaded		1	mA
ΔI_{CC}	Power Supply Current Per Input HIGH (3.0V)	V_{CC} = Max., V_{IN} = 3.0V	1	30	µA
I_{CCD}	Dynamic Power Supply Current[2]	V_{CC} = Max., C_L = 0pF	0.2	0.4	mA/ MHz

Note:

1. Guaranteed by characterization but not tested.
2. Relative to the frequency of Q outputs.

Table 8. Switching Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 3.3 ±0.3V

Symbol	Description[1]	Min	Max	Unit
t_{SKR}	Output Skew Between Rising Edges of Q0-Q4 (and Q/2 if $\overline{PE}$=Low)[2,3]	—	300	ps
t_{SKF}	Output Skew Between Falling Edges, Q0-Q4 (and Q/2 if $\overline{PE}$=High)[2,3]	—	300	ps
t_{SKALL}	Output Skew, All Outputs[2,3,6]	—	500	ps
t_{PW}	Pulse Width, 2xQ output >40MHz[2]	T_{CY}/2 –0.4	T_{CY}/2 +0.4	ns
t_{PW}	Pulse Width, Q0-Q4, $\overline{Q5}$, Q/2 outputs, 80MHz[2]	T_{CY}/2 –0.4	T_{CY}/2 +0.4	ns
t_J	Cycle to Cycle Jitter[2,5]	–0.15	0.15	ns
t_{PD}	SYNC Input to Feedback Delay[2,7]	–500	0	ps
t_{LOCK}	SYNC to Phase Lock	—	10	ms
t_{PZH} t_{PZL}	Output Enable Time, OE/$\overline{RST}$ LOW to High[4]	0	14	ns
t_{PHZ} t_{PLZ}	Output Disable Time, OE/$\overline{RST}$ HIGH to Low[2,4]	0	14	ns
t_R, t_F	Output Rise/Fall Times, 0.8V~2.0V[2]	0.3	2.0	ns

Notes:

1. See Figure 3 for test load and termination. Test circuit 1 is used for output enable/disable parameters. Test circuit 2 is used for all other timing parameters.
2. This parameter is guaranteed by characterization but not tested.
3. Skew specifications apply under identical environments (loading, temperature, V_{CC}, device speed grade).
4. Measured in open loop mode PLL_EN = 0.
5. Jitter is characterized using an oscilloscope, Q output at 20MHz. Measurement is taken one cycle after jitter. See FREQUENCY SELECTION TABLE for information on proper FREQ_SEL level for specified input frequencies.
6. Skew measured at selected synchronization edge.
7. t_{PD} measured at device inputs at 0.5V_{CC}, Q output at 80MHz.

Table 9. Input Timing Requirements

Industrial: T_A = –40°C to 85°C, V_{CC} = 3.3 ±0.3V

Symbol	Description	Min	Max	Unit
t_R, t_F	Maximum Input Rise and Fall Times, 0.8V to 2.0V	—	3.0	ns
F_I	Input Clock Frequency, SYNC0, SYNC1[1]	2.5	F_{MAX_2xQ}	MHz
t_{PWC}	Input Clock Pulse, HIGH or LOW[2]	2	—	ns
D_H	Duty Cycle, SYNC0, SYNC1[2]	25	75	%

Notes:

1. See Table 3 and Table 4 for more detail on allowable SYNC input frequencies for different speed grades with different FEEDBACK and FREQ_SEL combinations.
2. Input timing requirements are guaranteed by design but not tested. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

Figure 3. Test Loads and Waveforms

Test circuit 1 is used for output enable/disable parameters.
Test circuit 2 is used for all other timing parameters.

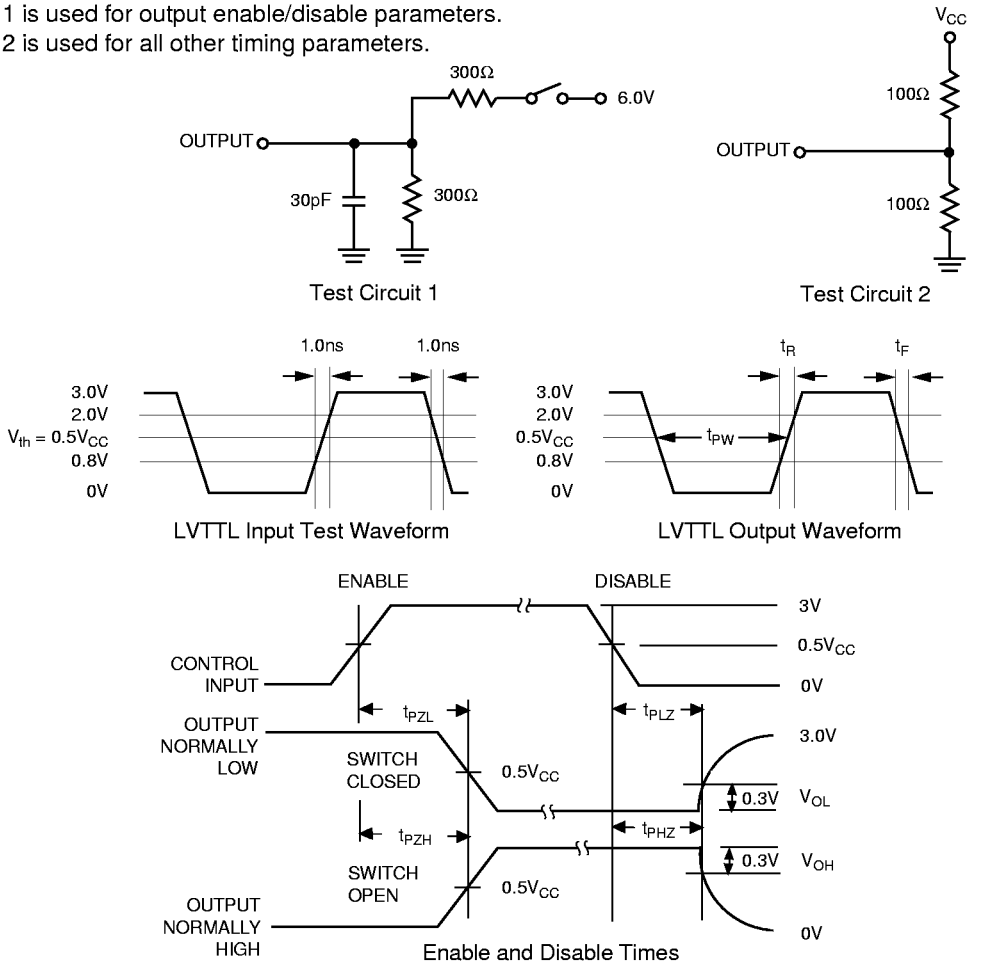
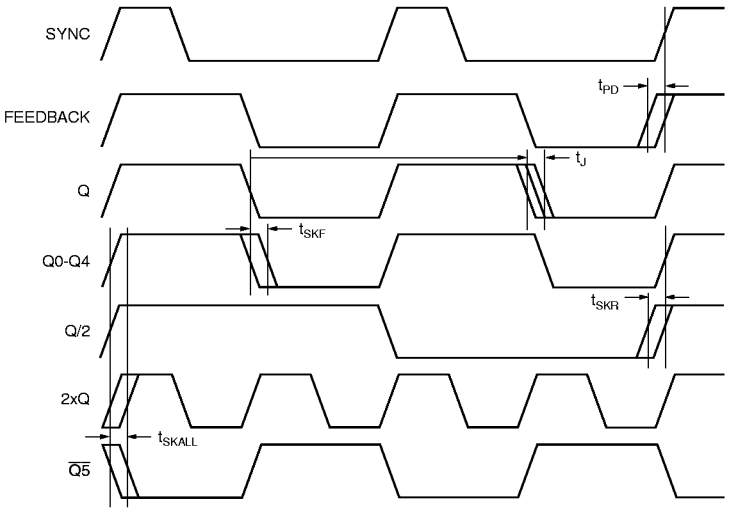


Figure 4. AC Timing Diagram



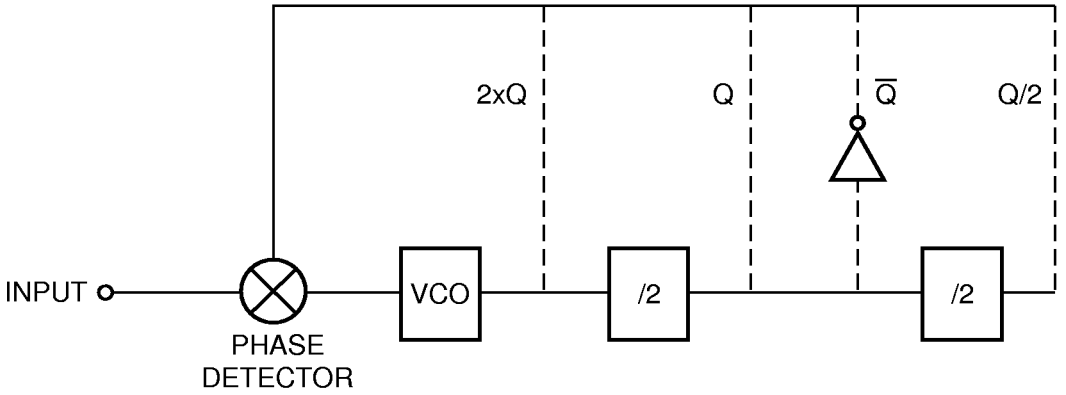
Notes:

1. Figure 4 applies to Q output connected to FEEDBACK and $\overline{PE}$ = GND. For $\overline{PE}$ = V_{CC}, the negative edge of FEEDBACK aligns with the negative edge of SYNC input, and the negative edges of the multiplied and divided outputs align with the negatve edge of SYNC.
2. All parameters are measured at $0.5V_{CC}$.

PLL OPERATION

The Phase Locked Loop (PLL) circuit included in the QS5LV919 provides for replication of incoming SYNC clock signals. Any manipulation of that signal, such as frequency multiplying or inversion is performed by digital logic following the PLL (see the block diagram). The key advantage of the PLL circuit is to provide an effective zero propagation delay between the output and input signals. In fact, adding delay circuits in the feedback path, 'propagation delay' can even be negative! Figure 5 shows a simplified schematic of the QS5LV919 PLL circuit:

Figure 5. Simplified Diagram of QS5LV919 Feedback



The phase difference between the output and the input frequencies feeds the VCO which drives the outputs. Whichever output is fed back, it will stabilize at the same frequency as the input. Hence, this is a true negative feedback closed loop system. In most applications, the output will optimally have zero phase shift with respect to the input. In fact, the internal loop filter on the QS5LV919 typically provides within 150ps of phase shift between input and output.

If the user wishes to vary the phase difference (typically to compensate for backplane delays), this is most easily accomplished by adding delay circuits to the feedback path. The respective output used for feedback will be advanced by the amount of delay in the feedback path. All other outputs will retain their proper relationships to that output.