## DESCRIPTION

The HY638100 is a high-speed 131,072 x 8-bits CMOS static RAM fabricated using Hyundai's high performance CMOS process technology. This high reliability process coupled with high-speed circuit design techniques, yields maximum access time of 15ns. The HY638100 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. It is suitable for use in high-density high-speed system applications.

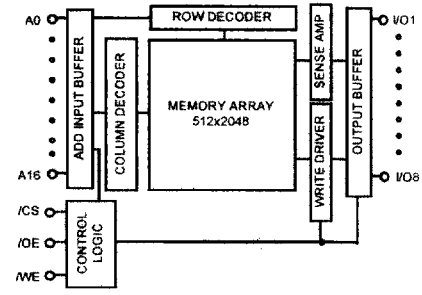
## FEATURES

- Single 5V±10% Power Supply
- High speed - 15/20/25ns(max.)
- Low power consumption(Max.)

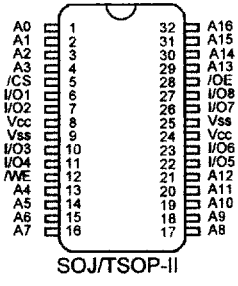
| Mode | Conditions | | Current | Units |
|---|---|---|---|---|
| Operating | 15ns | | 150 | mA |
| | 20/25ns | | 140 | mA |
| Standby | TTL | | 40 | mA |
| | CMOS | | 2 | mA |
| | | L | 500 | uA |

- Battery backup(L-part)
  - 2.0V(min.) data retention
- Fully static operation and Tri-state outputs
  - No clock or refresh required
- TTL compatible inputs and outputs
- Standard pin configuration
  - 32pin 400mil SOJ
  - 32pin 400mil TSOP-II

## BLOCK DIAGRM




## PIN CONNECTION




SOJ/TSOP-II

## PIN DESCRIPTION

| Pin Name | Pin Function |
|---|---|
| /CS | Chip Select |
| /WE | Write Enable |
| /OE | Output Enable |
| A0~A16 | Adderss Input |
| I/O1~I/O8 | Data Input/Output |
| Vcc | Power(+5.0V) |
| Vss | Ground |

## ORDERING INFORMATION

| Part No. | Speed | Power | Package |
|---|---|---|---|
| HY638100J | 15/20/25 | | SOJ |
| HY638100LJ | 15/20/25 | L-part | SOJ |
| HY638100T2 | 15/20/25 | | TSOP-II |
| HY638100LT2 | 15/20/25 | L-part | TSOP-II |

## ABSOLUTE MAXIMUM RATING (1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$, $V_{IN}$, $V_{OUT}$ | Power Supply, Input/Output Voltage | -0.5 to 7.0 | V |
| $T_A$ | Operating Temperature | 0 to 70 | ℃ |
| $T_{STG}$ | Storage Temperature | -65 to 150 | ℃ |
| $P_D$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | Data Output Current | 50 | mA |
| $T_{SOLDER}$ | Lead Soldering Temperature & Time | 260•10 | ℃•sec |

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

$T_A$=0℃ to 70℃

| Symbol | Parameter | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | - | Vcc+0.5 | V |
| $V_{IL}$ | Input Low Voltage | -0.5(1) | - | 0.8 | V |

Note
1. $V_{IL}$ = -3.0V for pulse width less than 10ns

## TRUTH TABLE

| /CS | /WE | /OE | Mode | I/O Operation |
|---|---|---|---|---|
| H | X | X | Standby | Hi-Z |
| L | H | H | Output Disabled | Hi-Z |
| L | H | L | Read | $D_{OUT}$ |
| L | L | X | Write | $D_{IN}$ |

Note:
1. H=$V_{IH}$, L=$V_{IL}$, X=Don't care

## DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V±10%, $T_A$ = 0℃ to 70℃, unless otherwise specified.

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | $V_{SS} \le V_{IN} \le V_{CC}$ | | -2 | - | 2 | uA |
| $I_{LO}$ | Output Leakage Current | $V_{SS} \le V_{OUT} \le V_{CC}$, /CS = $V_{IH}$ or /OE = $V_{IH}$ or /WE = $V_{IL}$ | | -2 | - | 2 | uA |
| $I_{CC1}$ | Average Operating Current | /CS = $V_{IL}$, $I_{I/O}$ = 0mA, Min. Duty Cycle = 100% | 15ns | - | - | 150 | mA |
| | | | 20/25ns | - | - | 140 | mA |
| $I_{SB}$ | TTL Standby Current (TTL Inputs) | /CS = $V_{IH}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$ Min. Cycle | | - | - | 40 | mA |
| $I_{SB1}$ | CMOS Standby Current (CMOS Inputs) | /CS ≥ Vcc-0.2V, $V_{IN}$ ≥ | | - | - | 2 | mA |
| | | Vcc-0.2V or $V_{IN} \le$ 0.2V | L | - | 50 | 500 | uA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8.0mA | | - | - | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4.0mA | | 2.4 | - | - | V |

Note : Typical values are at Vcc = 5.0V, $T_A$ = 25℃

## AC CHARACTERISTICS

Vcc = 5.0V±10%, $T_A$ = 0℃ to 70℃, unless otherwise specified.

| # | Symbol | Parameter | -15 | | -20 | | -25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| | READ CYCLE | | | | | | | | |
| 1 | tRC | Read Cycle Time | 15 | - | 20 | - | 25 | - | ns |
| 2 | tAA | Address Access Time | - | 15 | - | 20 | - | 25 | ns |
| 3 | tACS | Chip Select Access Time | - | 15 | - | 20 | - | 25 | ns |
| 4 | tOE | Output Enable to Output Valid | - | 7 | - | 9 | - | 10 | ns |
| 5 | tCLZ | Chip Select to Output in Low Z | 3 | - | 3 | - | 3 | - | ns |
| 6 | tOLZ | Output Enable to Output in Low Z | 3 | - | 3 | - | 3 | - | ns |
| 7 | tCHZ | Chip Deselecting to Output in High Z | 0 | 8 | 0 | 9 | 0 | 10 | ns |
| 8 | tOHZ | Out Disable to Output in High Z | 0 | 8 | 0 | 9 | 0 | 10 | ns |
| 9 | tOH | Output Hold from Address Change | 3 | - | 3 | - | 3 | - | ns |
| | WRITE CYCLE | | | | | | | | |
| 10 | tWC | Write Cycle Time | 15 | - | 20 | - | 25 | - | ns |
| 11 | tCW | Chip Select to End of Write | 12 | - | 15 | - | 17 | - | ns |
| 12 | tAW | Address Valid to End of Write | 12 | - | 15 | - | 17 | - | ns |
| 13 | tAS | Address Set-up Time | 0 | - | 0 | - | 0 | - | ns |
| 14 | tWP | Write Pulse Width | 12 | - | 15 | - | 17 | - | ns |
| 15 | tWR | Write Recovery Time | 2 | - | 2 | - | 2 | - | ns |
| 16 | tWHZ | Write to Output in High Z | 0 | 7 | 0 | 9 | 0 | 10 | ns |
| 17 | tDW | Data to Write Time Overlap | 8 | - | 9 | - | 10 | - | ns |
| 18 | tDH | Data Hold from Write Time | 0 | - | 0 | - | 0 | - | ns |
| 19 | tOW | Output Active from End of Write | 3 | - | 3 | - | 3 | - | ns |

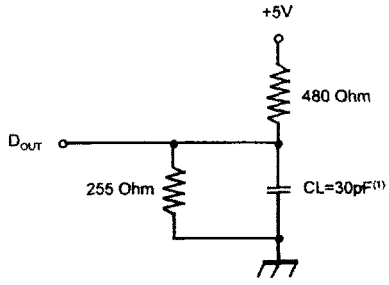
## AC TEST CONDITIONS

Vcc = 5.0V±10%, $T_A$ = 0℃ to 70℃, unless otherwise specified.

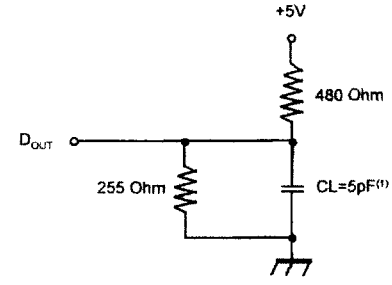
| Parameter | Value |
|---|---|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Time | 3ns |
| Input and Output Timing Reference Level | 1.5V |
| Output Load | See below |

## AC TEST LOADS

Output Load (A)




Output Load (B)
(for tCHZ, tCLZ, tOHZ, tOLZ, tWHZ & tOW)




Note : Including jig and scope capacitance

## CAPACITANCE

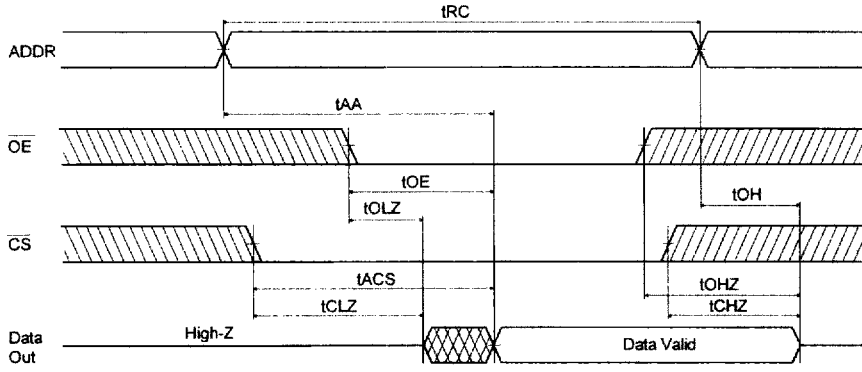
Temp = 25℃, f= 1.0MHz

| Symbol | Parameter | Condition | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$= 0V | 6 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{I/O}$ = 0V | 8 | pF |

Note : This parameter is sampled and not 100% tested

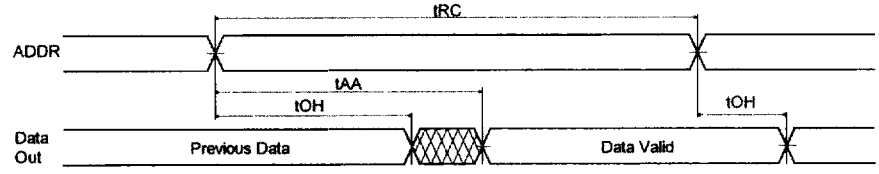
## TIMING DIAGRAM

### READ CYCLE 1



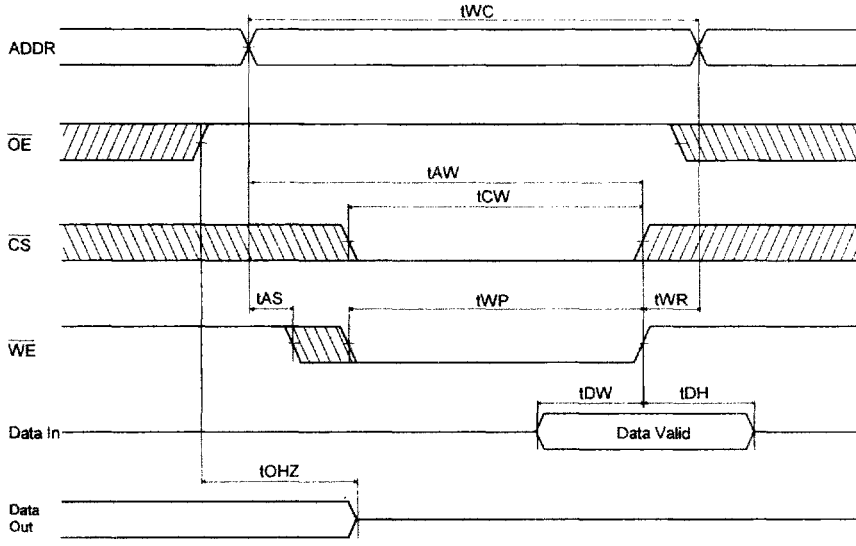

Note (Read Cycle)
1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for read cycle.

### READ CYCLE 2

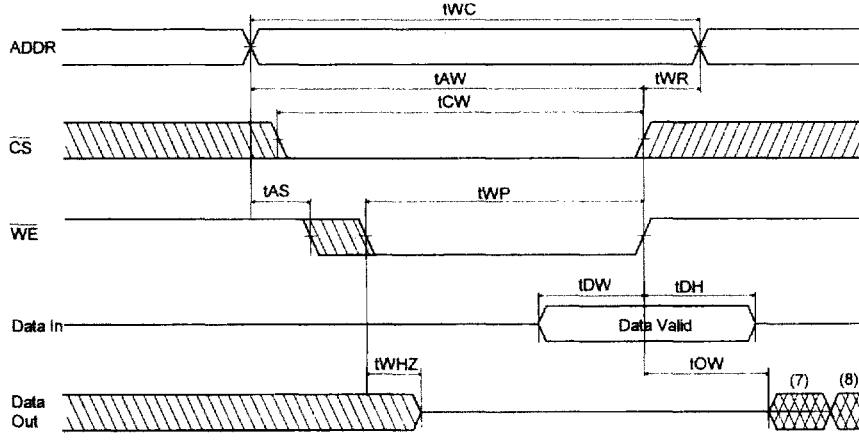



Note (Read Cycle)
1. /WE is high for read cycle.
2. Device is continuously selected /CS=VIL.
3. /OE=VIL.

**WRITE CYCLE 1(/OE Clocked)**




**WRITE CYCLE 2(/OE Low Fixed)**



Notes(Write Cycle)
1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low, and /WE going low : A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS or /WE going high.
5. If /OE and /WE are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of latest written data in the write cycle.
8. DOUT is the read data of the new address.

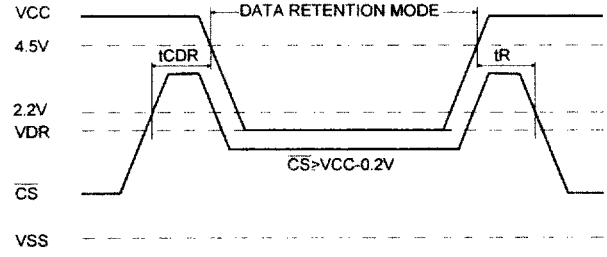
## DATA RETENTION ELECTRIC CHARACTERISTIC( L-Version )

TA=0℃ to 70℃

| Symbol | Parameter | Test Conditions | Power | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| VDR | Vcc for Data Retention | /CS ≥ Vcc - 0.2V<br>Vss ≤ VIN ≤ Vcc | | 2.0 | - | - | V |
| ICCDR | Data Retention Current | Vcc = 3V, /CS≥ Vcc-0.2V<br>Vss ≤ VIN ≤ Vcc | L | - | 10 | 50 | uA |
| tCDR | Chip Deselect to Data Retention Time | See Data Retention Timing Diagram | | 0 | - | - | ns |
| tR | Operating Recovery Time | | | tRC(2) | - | - | ns |

Notes
1. Typical values are at the condition of TA=25℃
2. tRC is read cycle time

## DATA RETENTION WAVEFORM

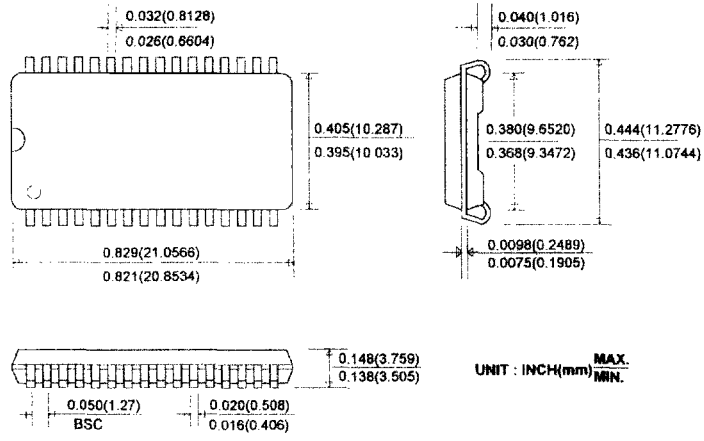



## RELIABILITY SPEC.

| TEST MODE | | TEST SPEC. |
|---|---|---|
| ESD | HBM | ≥ 2000V |
| | MM | ≥ 250V |
| LATCH - UP | | ≤ -100mA |
| | | ≥100mA |

## PACKAGE INFORMATION

### 32pin 400mil Small Outline J-Form Package (J)




### 32pin 400mil Thin Small Outline Package (T2)