MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Order this document
by MCM318165CV/D

1M x 16

MCM318165CV
EDO
1024 Cycle Refresh

Advance Information

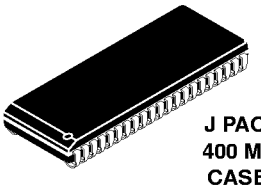
16M CMOS Wide DRAM Family

EDO, 1M x 16, 1K

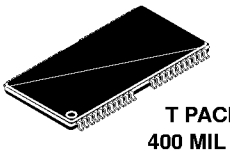
The family of 16M Dynamic RAMs is fabricated using 0.40µ CMOS high–speed silicon–gate process technology. It includes devices organized as 1,048,576 sixteen–bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The x16 with 1024 cycle refresh (MCM318165CV) require only 10 address lines (10 rows, 10 columns).

These devices are packaged in a standard 400 mil J–lead small outline package (SOJ) and a standard 400 mil thin–small–outline package (TSOP).



J PACKAGE
400 MIL SOJ
CASE 986B



T PACKAGE
400 MIL TSOP II
CASE 985D

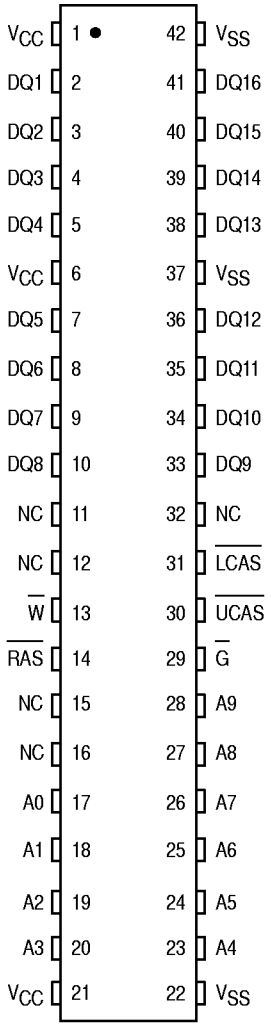
- Single 3.3 V ± 10% Power Supply
- Three–State Data Outputs, x16 Configuration
- Extended Data Out (EDO)
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 1024 Cycle Refresh:
  MCM318165CV = 16 ms
- Fast Access Time (t_{RAC}):
  MCM31xxxxCV–60 = 60 ns (Max)
  MCM31xxxxCV–70 = 70 ns (Max)
- Low Active Power Dissipation:
  MCM318165CV–60 = 540 mW (Max)
  MCM318165CV–70 = 470 mW (Max)
- Low Standby Power Dissipation:
  All Devices = 1.8 mW (Max, CMOS Levels)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

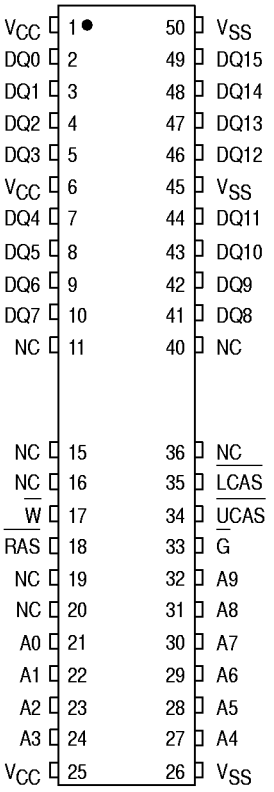
12/2/96

PIN ASSIGNMENTS

400 MIL SOJ



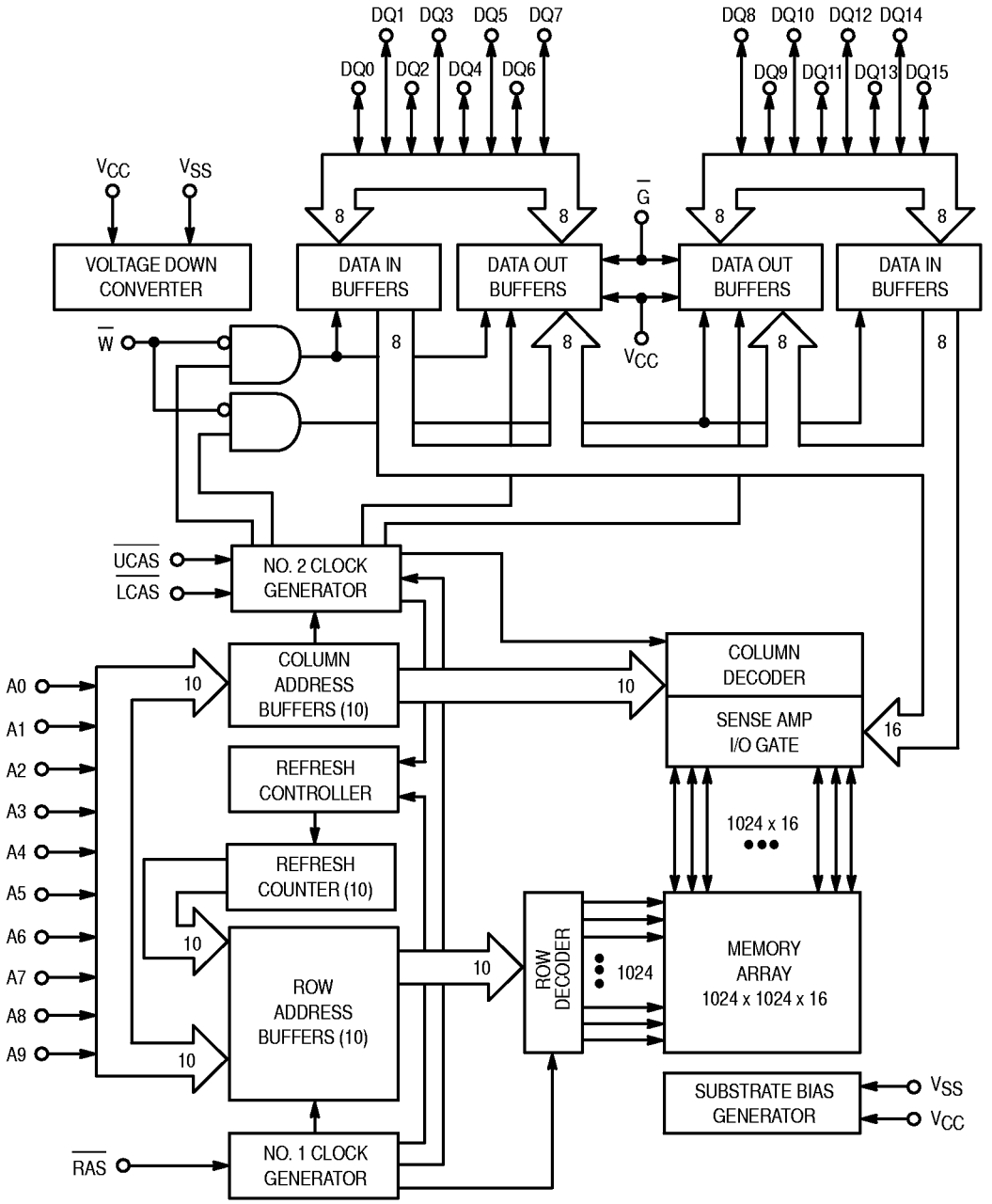
400 MIL TSOP



PIN NAMES	
A0 – A9 . . . . . Address Input	LCAS . . . . . Column Address Strobe
DQ0 – DQ15 . . . . . Data Input/Output	UCAS . . . . . Column Address Strobe
G . . . . . Output Enable	V_{CC} . . . . . Power Supply (+ 3.3 V)
W . . . . . Read/Write Enable	V_{SS} . . . . . Ground
RAS . . . . . Row Address Strobe	NC . . . . . No Connection

BLOCK DIAGRAMS

MCM318165CV BLOCK DIAGRAM
1M x 16, 1024 CYCLE REFRESH



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS}, Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to 4.6	V
Data Out Current	I_{out}	50	mA
Power Dissipation MCM318165CV	P_D	1000	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	0	—	V_{CC} + 0.3*	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.3**	—	0.8	V

* V_{CC} + 2.0 V at pulse width ≤ 20 ns.
** –2.0 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	MCM318165CV–60		MCM318165CV–70		Unit	Notes
		Min	Max	Min	Max		
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min)	I_{CC1}	—	150	—	130	mA	1, 2, 3
V_{CC} Power Supply Current (Standby) (RAS = UCAS = LCAS = V_{IH})	I_{CC2}	—	2	—	2	mA	4
V_{CC} Power Supply Current During RAS Only Refresh Cycles (UCAS = LCAS = V_{IH}, t_{RC} = t_{RC} Min)	I_{CC3}	—	150	—	130	mA	1, 3
V_{CC} Power Supply Current During Extended Data Out Cycle (RAS = V_{IL})	I_{CC4}	—	130	—	110	mA	1, 2, 3
V_{CC} Power Supply Current (Standby) (RAS = UCAS = LCAS = V_{CC} – 0.2 V)	I_{CC5}	—	0.5	—	0.5	mA	
V_{CC} Power Supply Current During CAS Before RAS Refresh Cycles (t_{RC} = t_{RC} Min)	I_{CC6}	—	150	—	130	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})	$I_{lkg(I)}$	–10	10	–10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ V_{CC}, Output Disable)	$I_{lkg(O)}$	–10	10	–10	10	µA	
Output High Voltage (I_{OH} = – 2 mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage (I_{OL} = 2 mA)	V_{OL}	—	0.4	—	0.4	V	

NOTES:
1. I_{CC1}(AV), I_{CC3}(AV), and I_{CC4}(AV) are dependent on cycle rate. Maximum current measured at the fastest cycle rate.
2. I_{CC1}(AV) and I_{CC4}(AV) are dependent on output loading. Specified values are obtained with the ouput open.
3. Column address can be changed once or less while RAS = V_{IL} and LCAS/UCAS = V_{IH}.
4. An initial pause of 500 µs is required after power–up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS–only refresh).

CAPACITANCE (T_A = 0 to 70°C, V_{CC} = 3.3 V, Unless Otherwise Noted)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A11	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$		7	
Input/Output Capacitance (UCAS, LCAS = V_{IH} to Disable Output)	DQ0 – DQ15	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.
1. IColumn address can be changed once or less while RAS = V_{IL} and LCAS/UCAS = V_{IH}.
2. IMeasured with a load circuit equivalent to V_{OH} = 2.4 V (I_{OH} = 2mA)/V_{OL} = 0.4 V (I_{OL} = 2mA) load 100 pF.

OPERATING PARAMETERS

SWITCHING CHARACTERISTICS

Parameter	Symbol		MCM318165CV–60		MCM318165CV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Access Time from CAS	t_{CELQV}	t_{CAC}	—	15	—	20	ns	1, 2
Access Time from RAS	t_{RELQV}	t_{RAC}	—	60	—	70	ns	1, 3
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	1, 4
Access Time from CAS Precharge	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	1, 5
Access Time from G	t_{GLGH}	t_{GA}	—	15	—	20	ns	1
CAS to Output in Low–Z	t_{CELQX}	t_{CLZ}	—	5	—	5	ns	1
Output Buffer Turn–Off Delay from G	t_{GHQZ}	t_{GZ}	0	15	0	20	ns	6
Output Buffer Turn–Off Delay from WE	t_{WLQZ}	t_{WEZ}	0	15	0	20	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	20	ns	6, 7
Output Buffer Turn–Off Delay from RAS	t_{REHQZ}	t_{REZ}	0	15	0	20	ns	6, 7

NOTES:
1. Measured with a load circuit equivalent to V_{OH} = 2.4 V (I_{OH} = 2mA)/V_{OL} = 0.4 V (I_{OL} = 2mA) load 100 pF.
2. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{ASC} \geq t_{ASC}(max)$ and $t_{CP} \geq t_{CP}(max)$.
3. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
4. Assumes that $t_{RAD} \geq t_{RAD}(max)$ and $t_{ASC} \geq t_{ASC}(max)$.
5. Assumes that $t_{CP} \leq t_{CP}(max)$ and $t_{ASC} \geq t_{ASC}(max)$.
6. $t_{GZ}(max)$, $t_{WEZ}(max)$, $t_{OFF}(max)$ and $t_{REZ}(max)$ define the time at which the output achieves the high impedance state ($|I_{OUT}| \leq |\pm 10\ \mu A|$) and is not reference to $V_{OH}(min)$ or $V_{OL}(max)$.
7. Output is disabled after both RAS and CAS go to high.

TIMING REQUIREMENTS

Parameter	Symbol		MCM318165CV–60		MCM318165CV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Refresh Period	t_{RVRV}	t_{REF}	—	16.4	—	16.4	ms	
RAS Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
Delay Time, RAS Low to CAS Low	t_{RELCEL}	t_{RCD}	20	45	20	50	ns	3
Delay Time, CAS High to RAS Low	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
Delay Time, RAS High to CAS Low	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Delay Time, RAS to Column Address	t_{RELAV}	t_{RAD}	15	30	15	35	ns	4
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	13	0	13	ns	5
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	0	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	10	—	ns	
Delay Time, G High to Data	t_{GLHDX}	t_{GD}	15	—	20	—	ns	
Transition Time (Rise and Fall)	t_T	t_T	1	50	1	50	ns	6

NOTES:
1. The timing requirements are assumed t_T = 2 ns.
2. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals.
3. $t_{RCD}(max)$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD}(max)$, access time is controlled exclusively by t_{AA}.
4. $t_{RAD}(max)$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD}(max)$ and $t_{ASC} \leq t_{ASC}$ (max), access time is controlled exclusively by t_{AA}.
5. $t_{ASC}(max)$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD}(max)$ and $t_{ASC} \geq t_{ASC}$ (max), access time is controlled exclusively by t_{CAC}.
6. t_T is measured between $V_{IH}(min)$ and $V_{IL}(max)$.

READ AND REFRESH CYCLES

Parameter	Symbol		MCM318165CV–60		MCM318165CV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	60	10K	70	10K	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	10	10K	13	10K	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	48	—	55	—	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	1
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	10	—	10	—	ns	1
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
RAS Hold Time Referenced to G	t_{GLREH}	t_{ROH}	15	—	20	—	ns	

NOTES:
1. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

WRITE CYCLE (EARLY WRITE AND DELAYED WRITE)

Parameter	Symbol		MCM318165CV–60		MCM318165CV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	60	10K	70	10K	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	10	10K	13	10K	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	48	—	55	—	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	15	—	20	—	ns	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	2
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	13	—	ns	
Write Command to CAS Lead	t_{WLCEH}	t_{CWL}	10	—	13	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	10	—	13	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	10	—	13	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	
Data in Hold Time	t_{CELDX}	t_{DH}	10	—	13	—	ns	

NOTES:
1. t_{RWC} is specified as $t_{RWC}(min) = t_{RAC}(max)+t_{GD}(min)+t_{RP}(min)=4t_T$.
2. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPWD} \geq t_{CPWD}(min)$ (for extended data out mode cycle only), the cycle is a read–modify–write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or G goes back to V_{IH}) is indeterminate.

READ–WRITE AND READ–MODIFY–WRITE CYCLES

Parameter	Symbol		MCM318165CV–60		MCM318165CV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read–Write/Read–Modify Write Cycle Time	t_{RELREL}	t_{RWC}	133	—	161	—	ns	
RAS Low Pulse Width	t_{RELREH}	t_{RAS}	89	10K	107	10K	ns	
CAS Low Pulse Width	t_{CELCEH}	t_{CAS}	44	10K	57	10K	ns	
CAS Hold Time after RAS Low	t_{RELCEH}	t_{CSH}	82	—	99	—	ns	
RAS Hold Time after CAS Low	t_{CELREH}	t_{RSH}	44	—	57	—	ns	
Read Setup Time before CAS Low	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	1
Delay Time, CAS Low to W Low	t_{CELWL}	t_{CWD}	32	—	42	—	ns	1
Delay Time, RAS Low to W Low	t_{RELWL}	t_{RWD}	77	—	92	—	ns	1
Delay Time, Address to W Low	t_{AVWL}	t_{AWD}	47	—	57	—	ns	
G Hold Time after W Low	t_{WLGL}	t_{GH}	15	—	20	—	ns	

NOTES:

1. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min) (for extended data out mode cycle only), the cycle is a read–modify–write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or G goes back to V_{IH}) is indeterminate.

EXTENDED DATA OUT MODE CYCLES

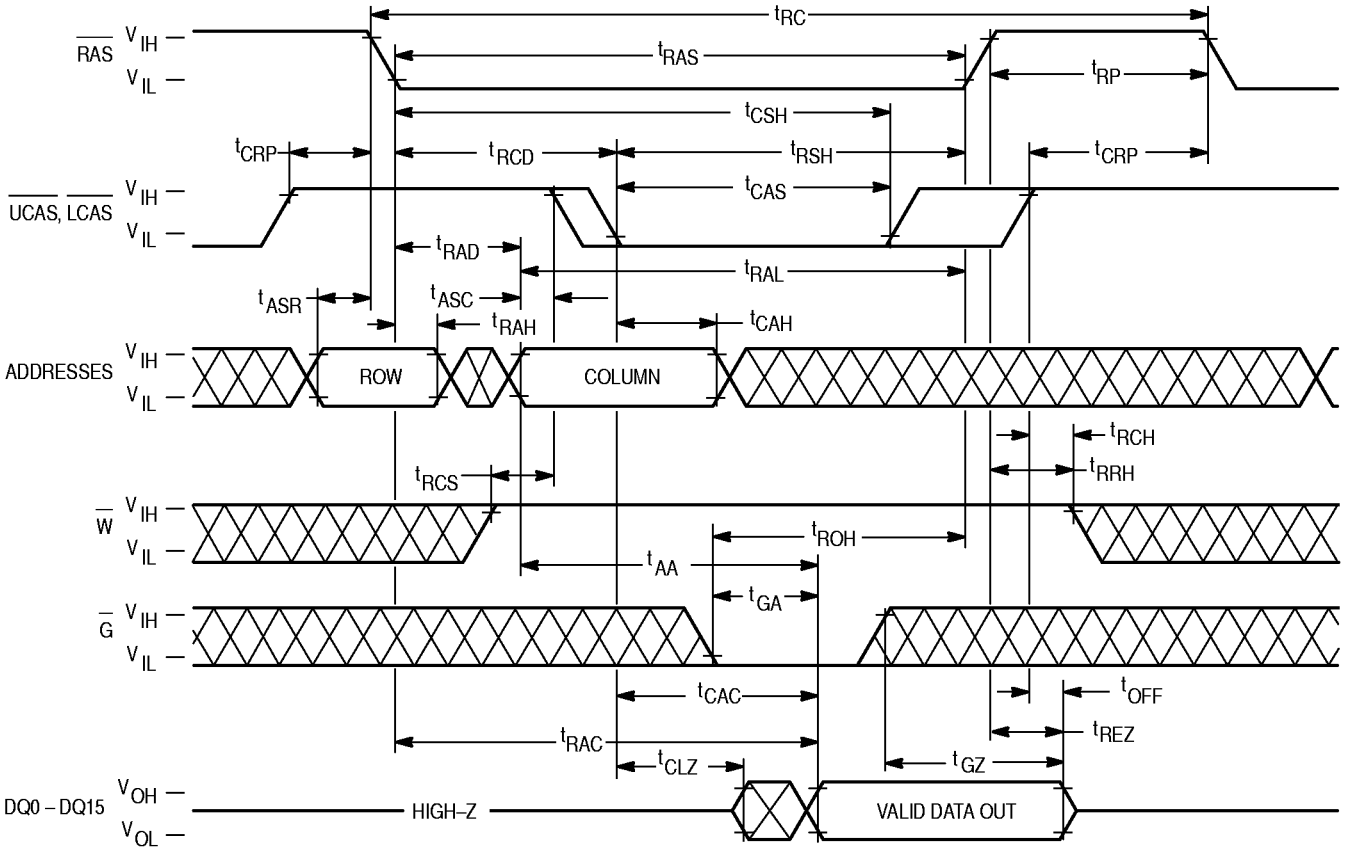
Parameter	Symbol		MCM318165CV–60		MCM318165CV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Extended Data Out Read/Write Cycle Time	t_{CELCEL}	t_{EPC}	25	—	30	—	ns	
Extended Data Out Read–Write Cycle Time	t_{CELCEL}	t_{ERWC}	66	—	79	—	ns	
Output Data Hold Time	t_{CELQZ}	t_{COH}	5	—	5	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RASP}	77	100K	92	100K	ns	3
CAS Precharge Time	t_{CEHCEL}	t_{ECP}	10	16	10	16	ns	4
RAS Hold Time after CAS Precharge	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
CAS Precharge to W Delay	t_{CEHWL}	t_{CPWD}	52	—	62	—	ns	1
Delay Time, CAS Low to W Low	t_{CELWL}	t_{ECWD}	32	—	42	—	ns	
Delay Time, Address to W Low	t_{AVWL}	t_{EAWD}	62	—	72	—	ns	

NOTES:

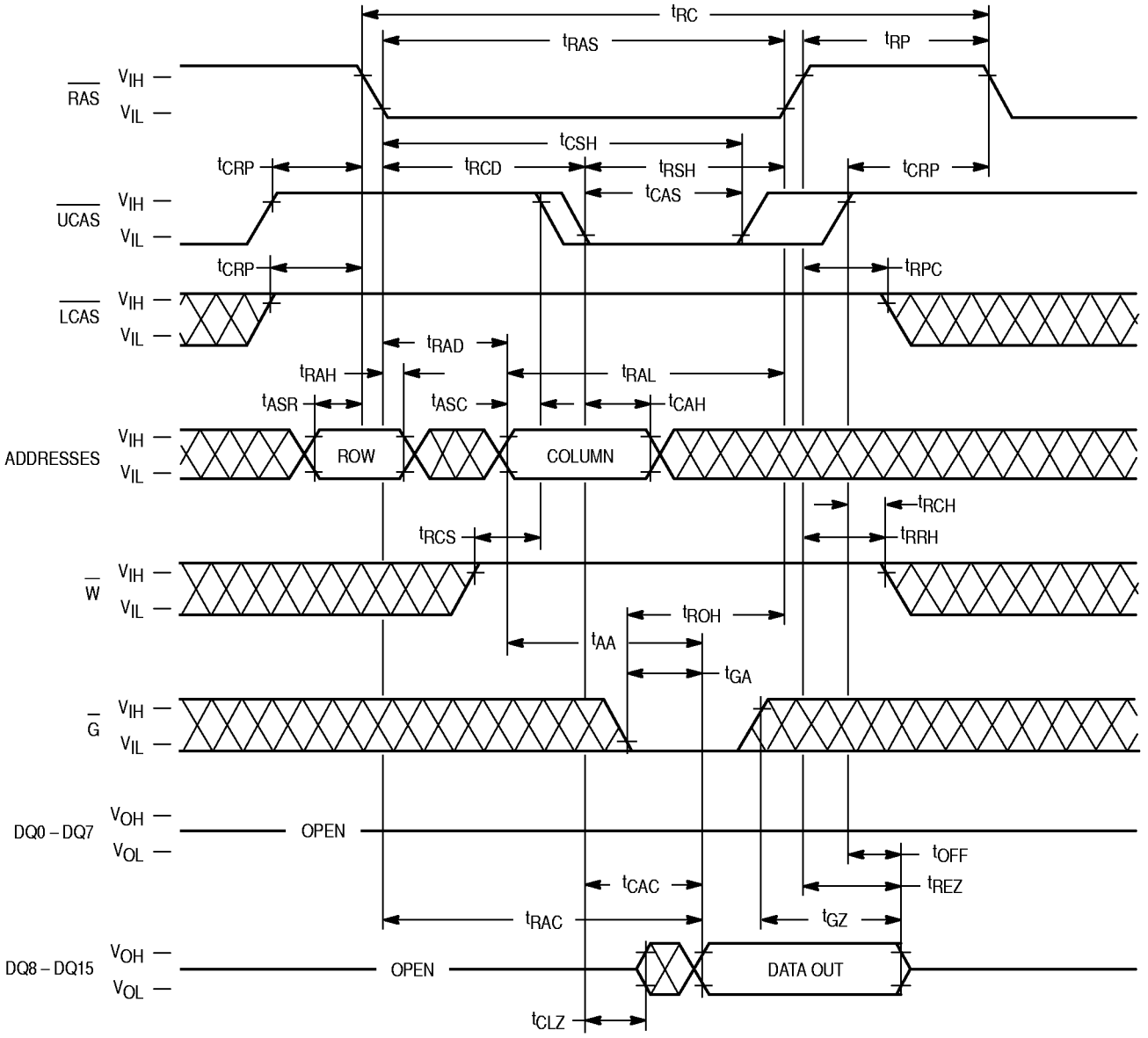
1. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min) (for extended data out mode cycle only), the cycle is a read–modify–write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or G goes back to V_{IH}) is indeterminate.
2. All previously specified timing requirements and switching characteristics are applicable to their respective Extended Data Out mode cycle.
3. t_{RAS}(min) is specified as two cycles of CAS input are performed.
4. t_{CP}(max) is specified as a reference point only.

TIMING DIAGRAMS

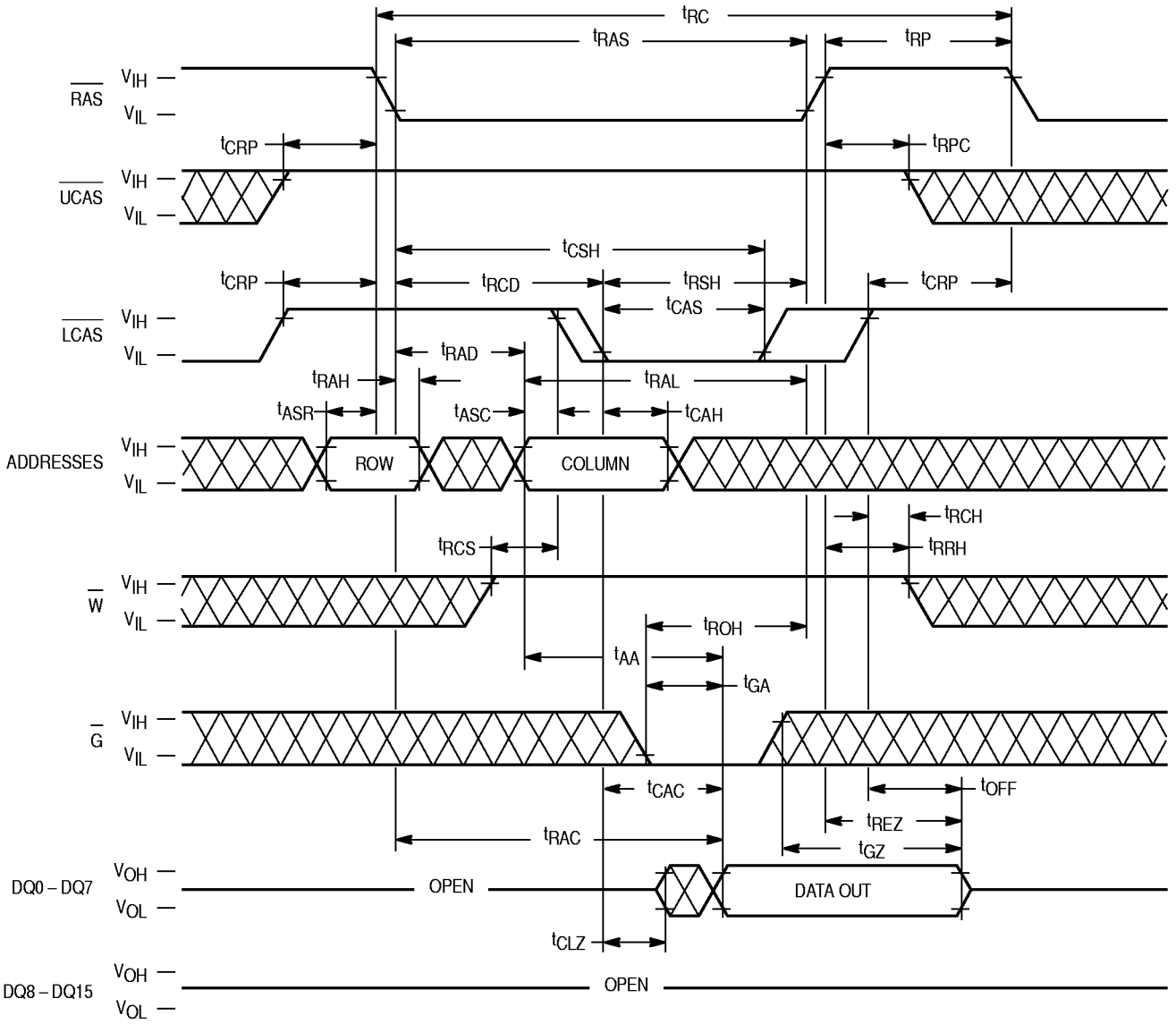
READ CYCLE



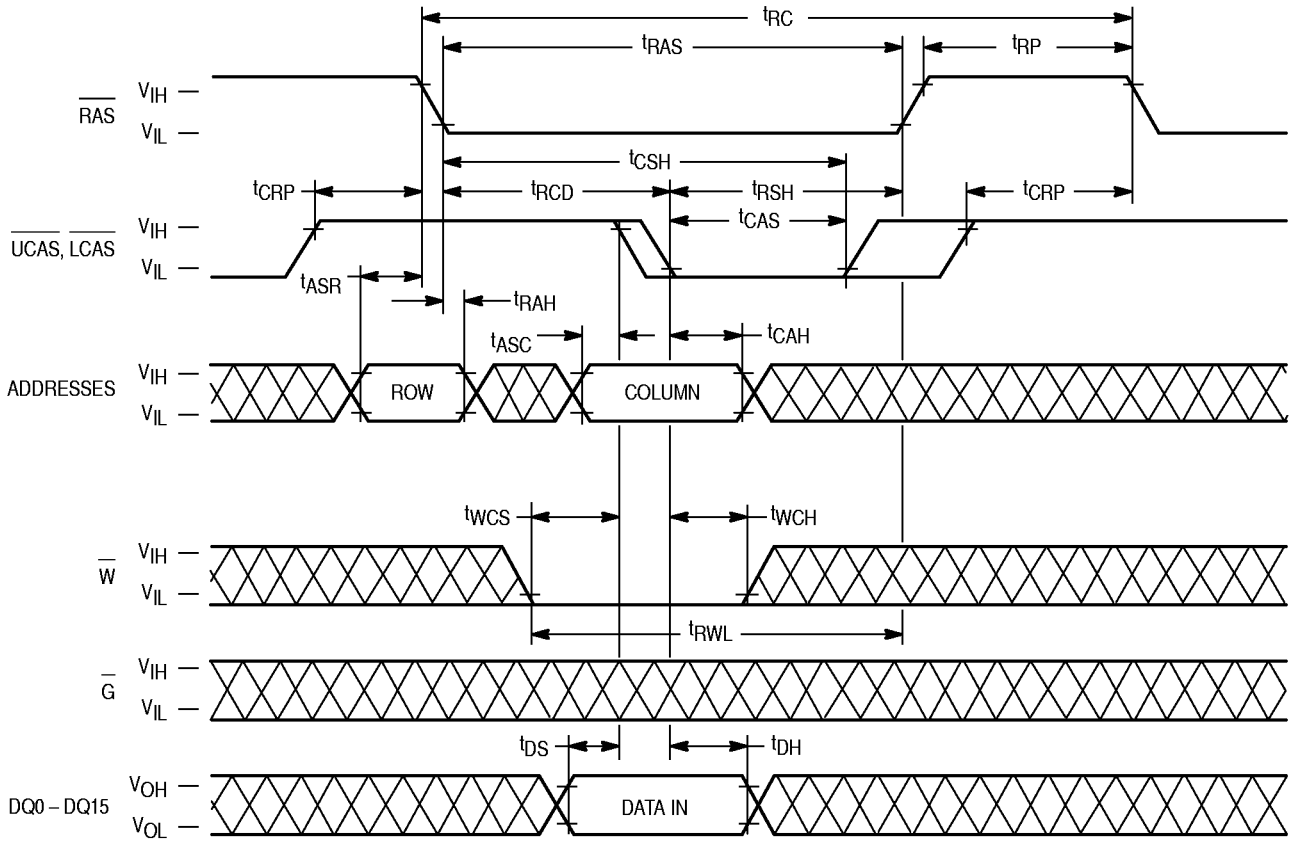
UPPER BYTE READ CYCLE



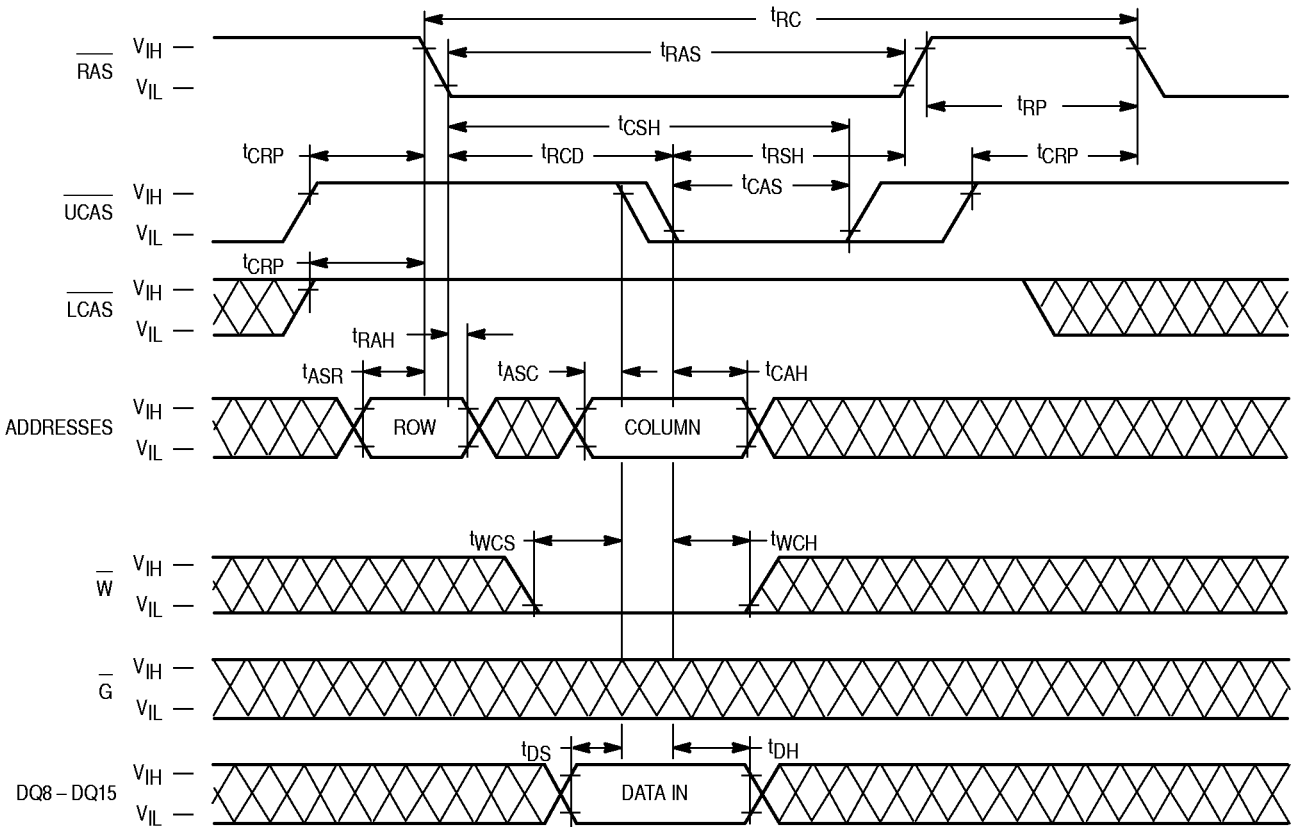
LOWER BYTE READ CYCLE



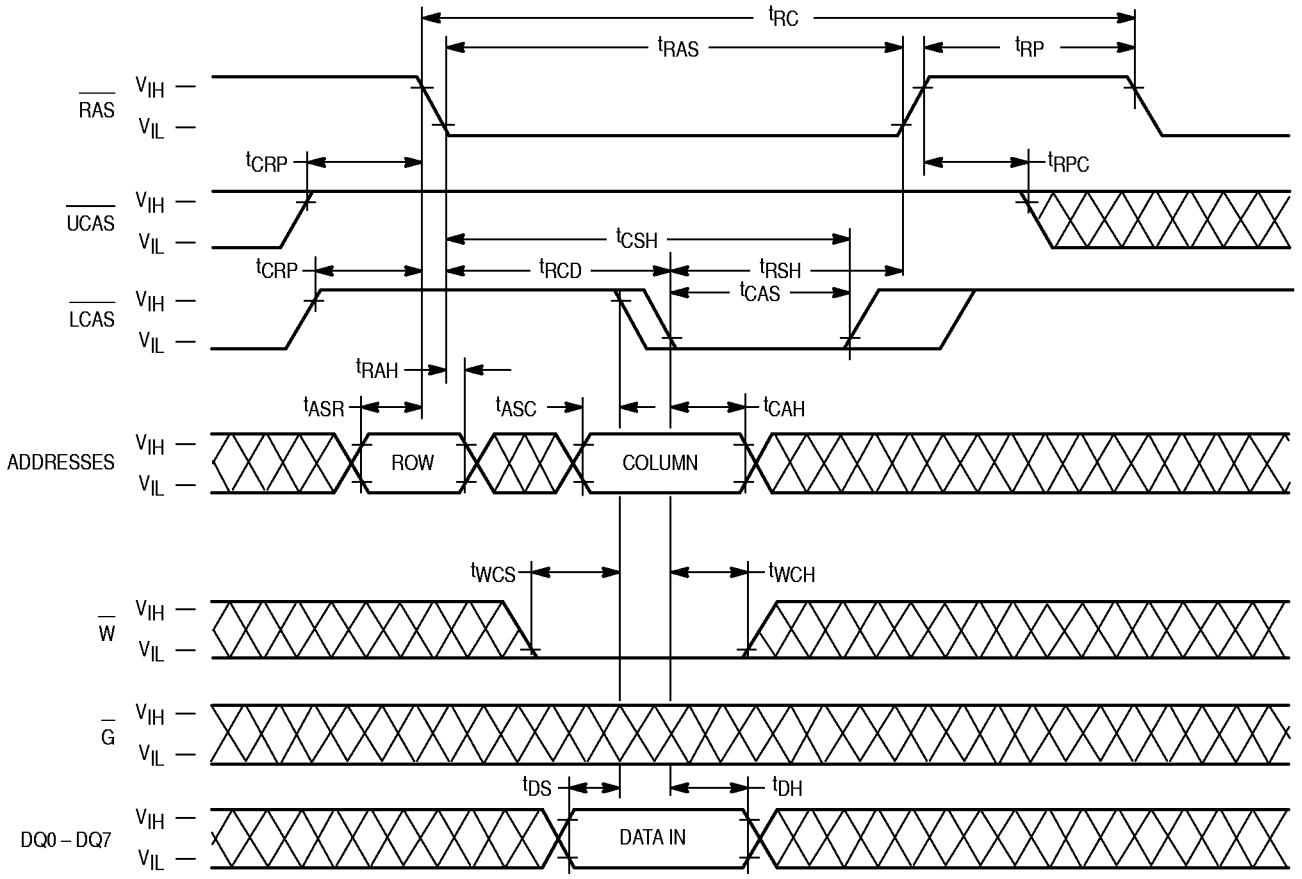
WRITE CYCLE (EARLY WRITE)



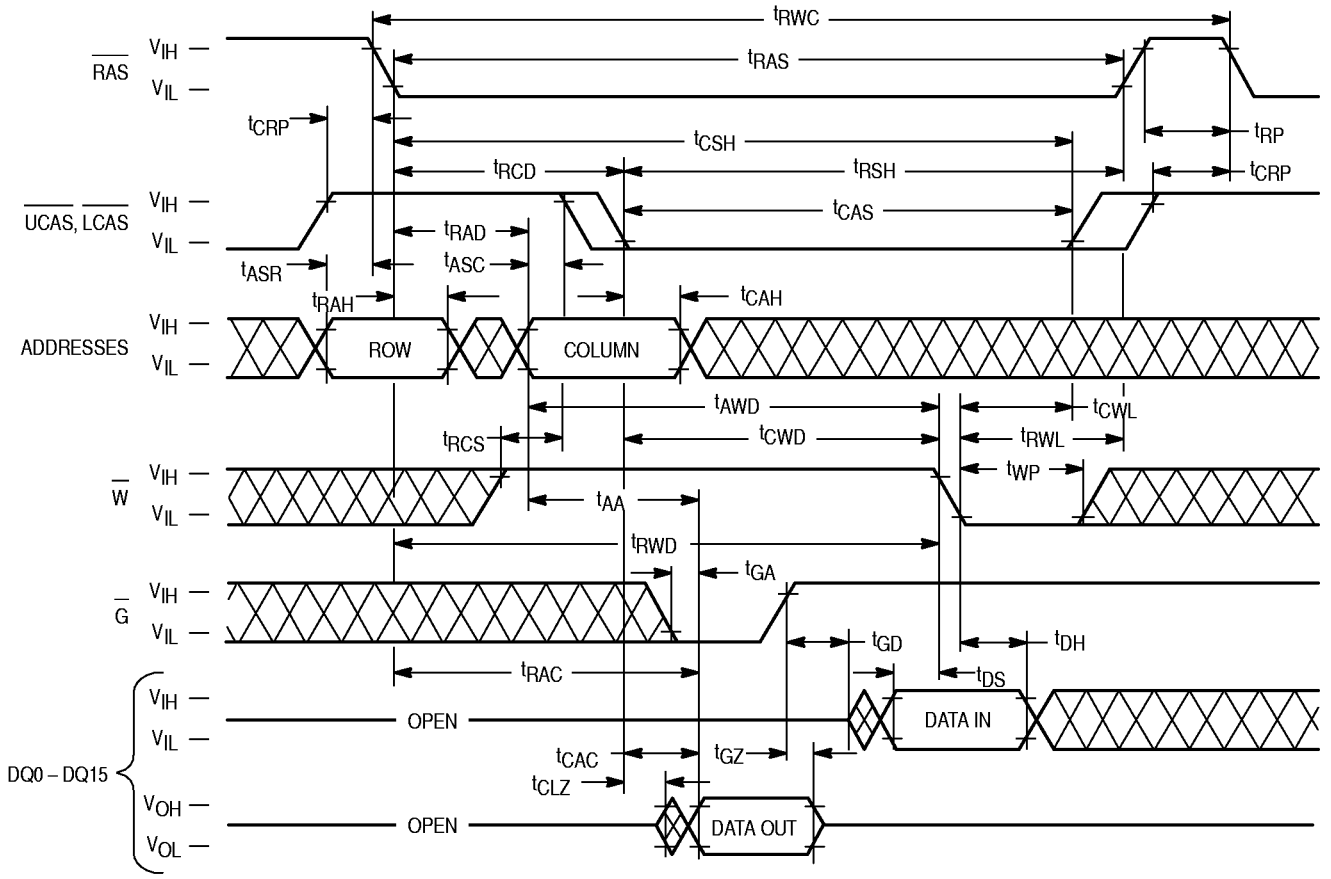
UPPER BYTE WRITE CYCLE (EARLY WRITE)



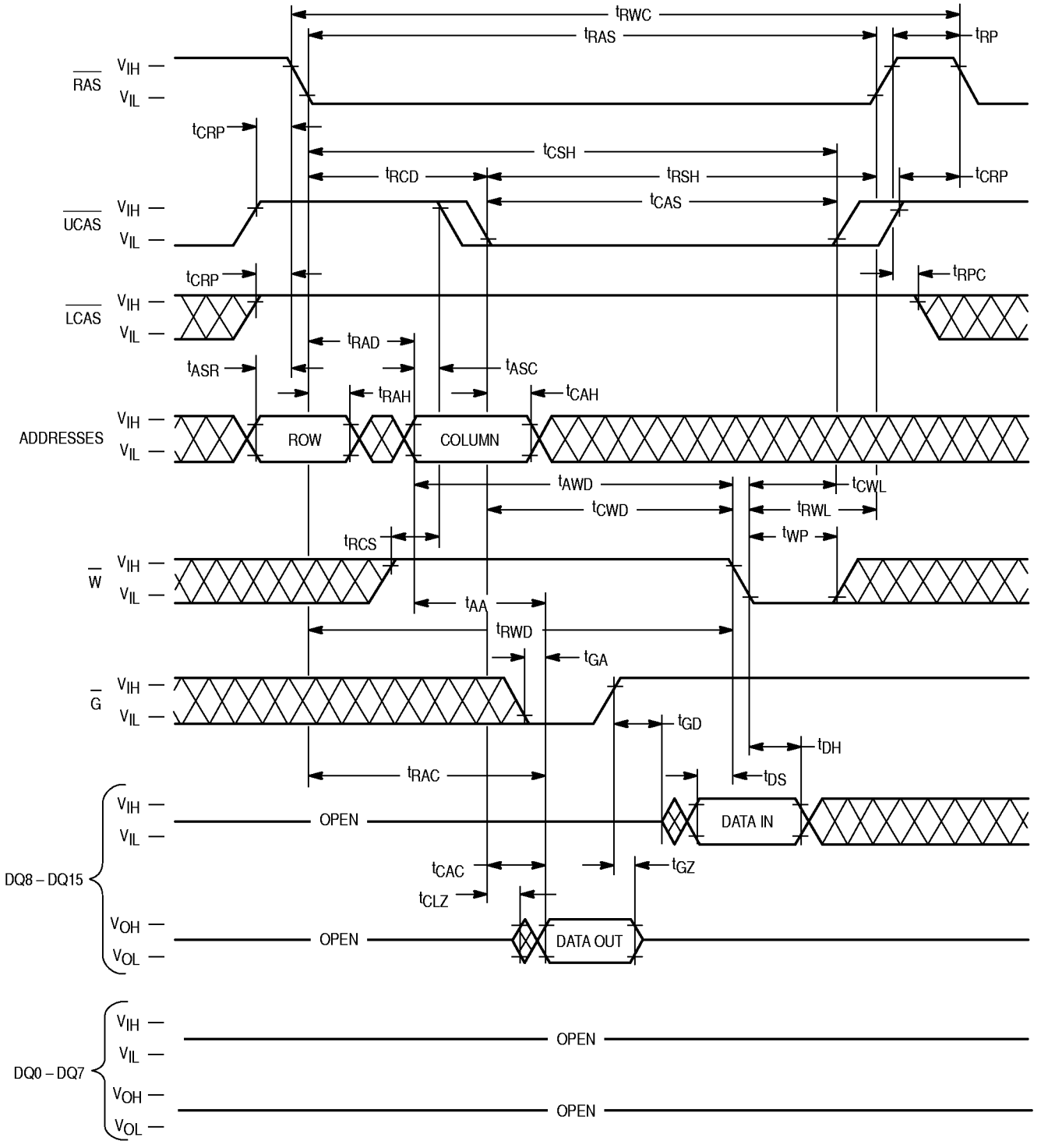
LOWER BYTE WRITE CYCLE (EARLY WRITE)



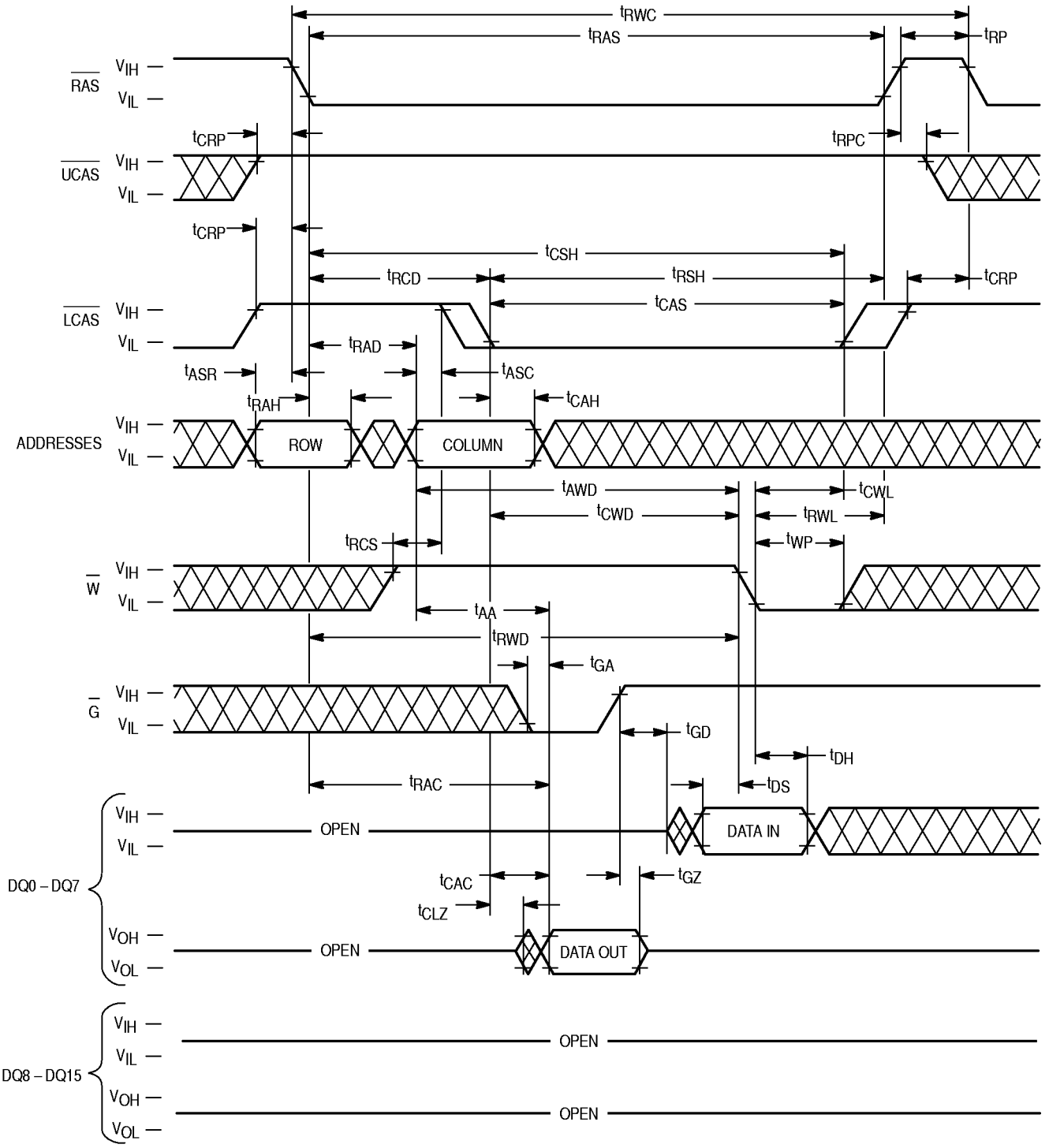
READ–WRITE CYCLE



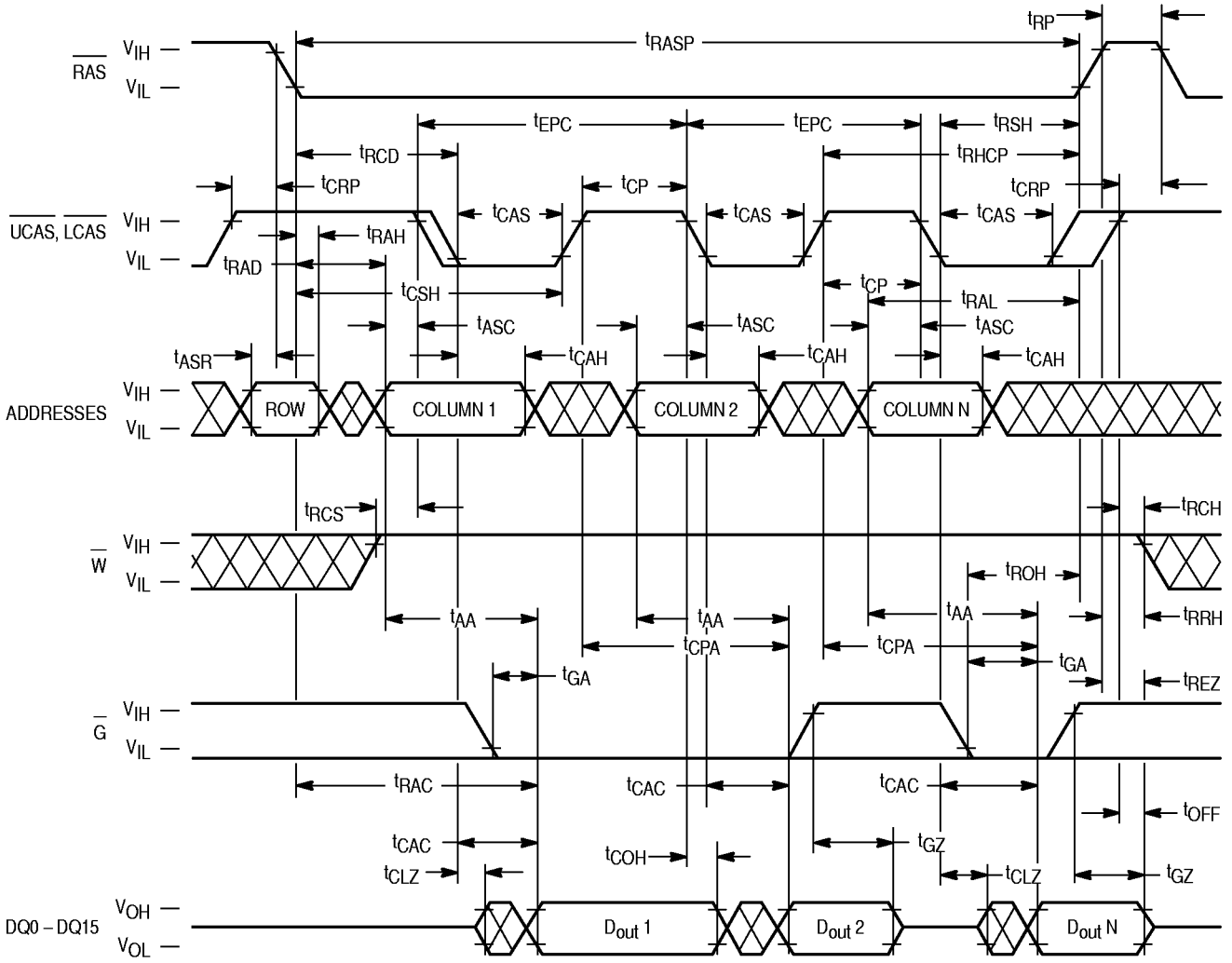
UPPER BYTE READ–WRITE CYCLE



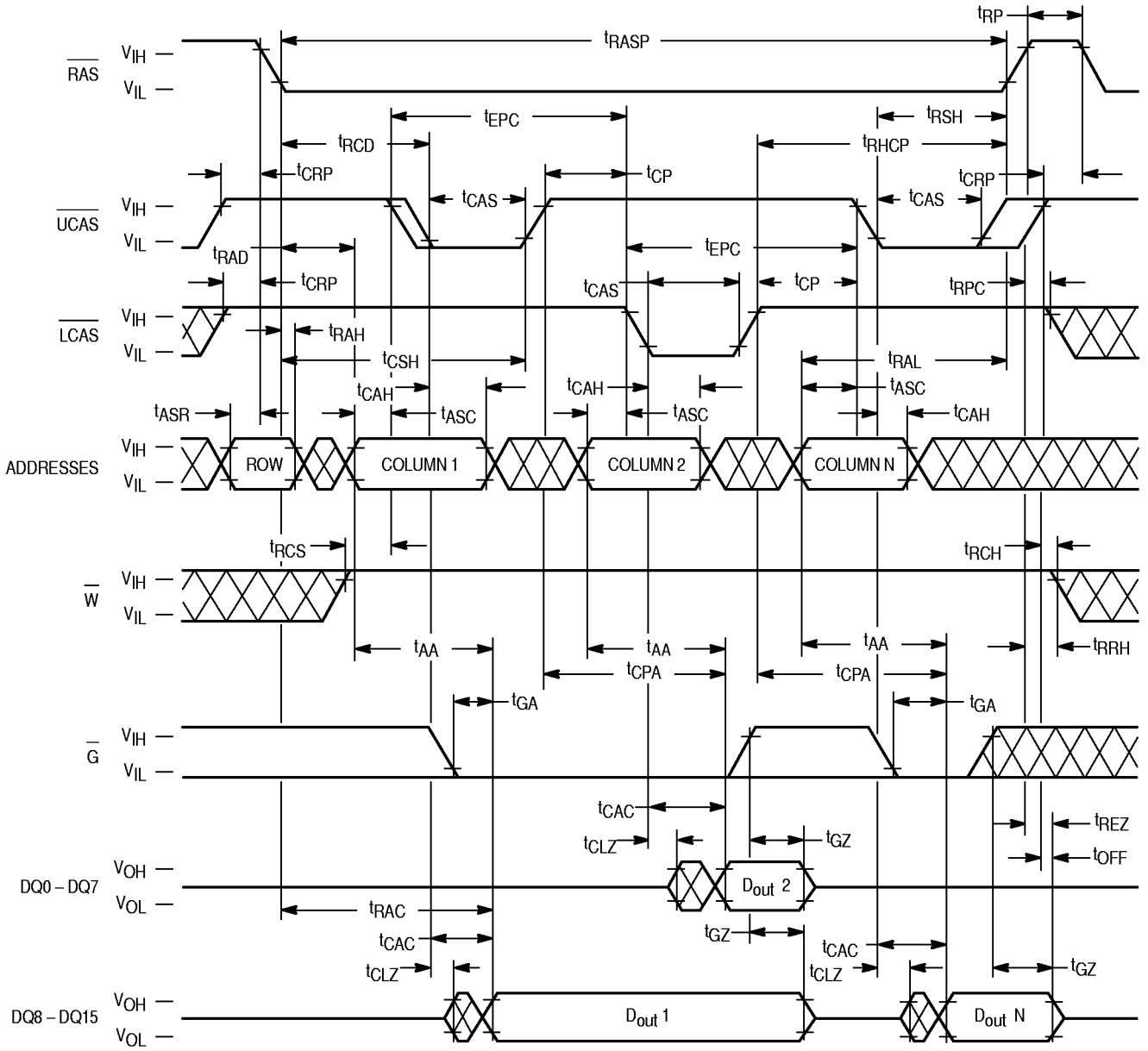
LOWER BYTE READ–WRITE CYCLE



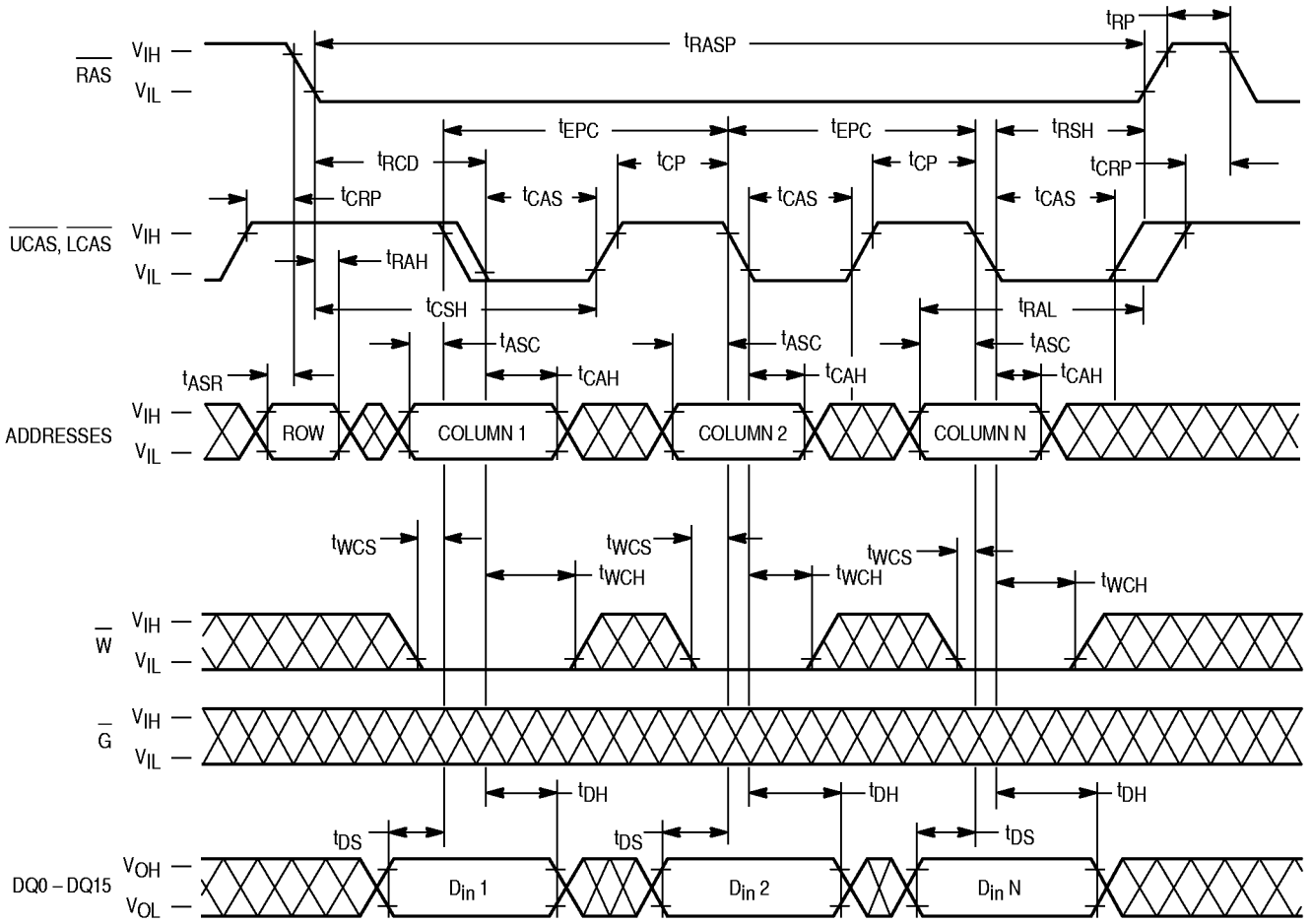
EXTENDED DATA OUT READ CYCLE



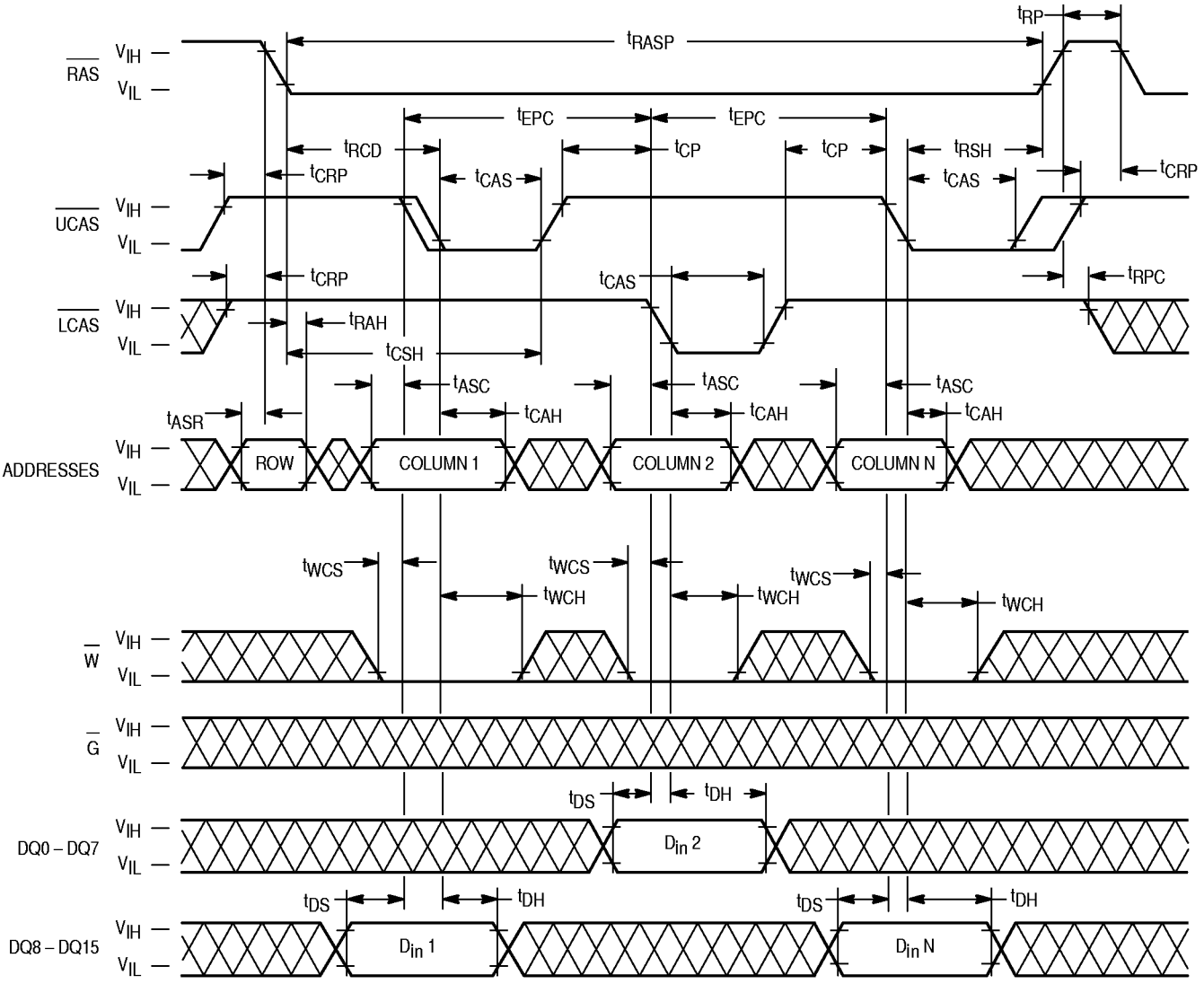
EXTENDED DATA OUT BYTE READ CYCLE



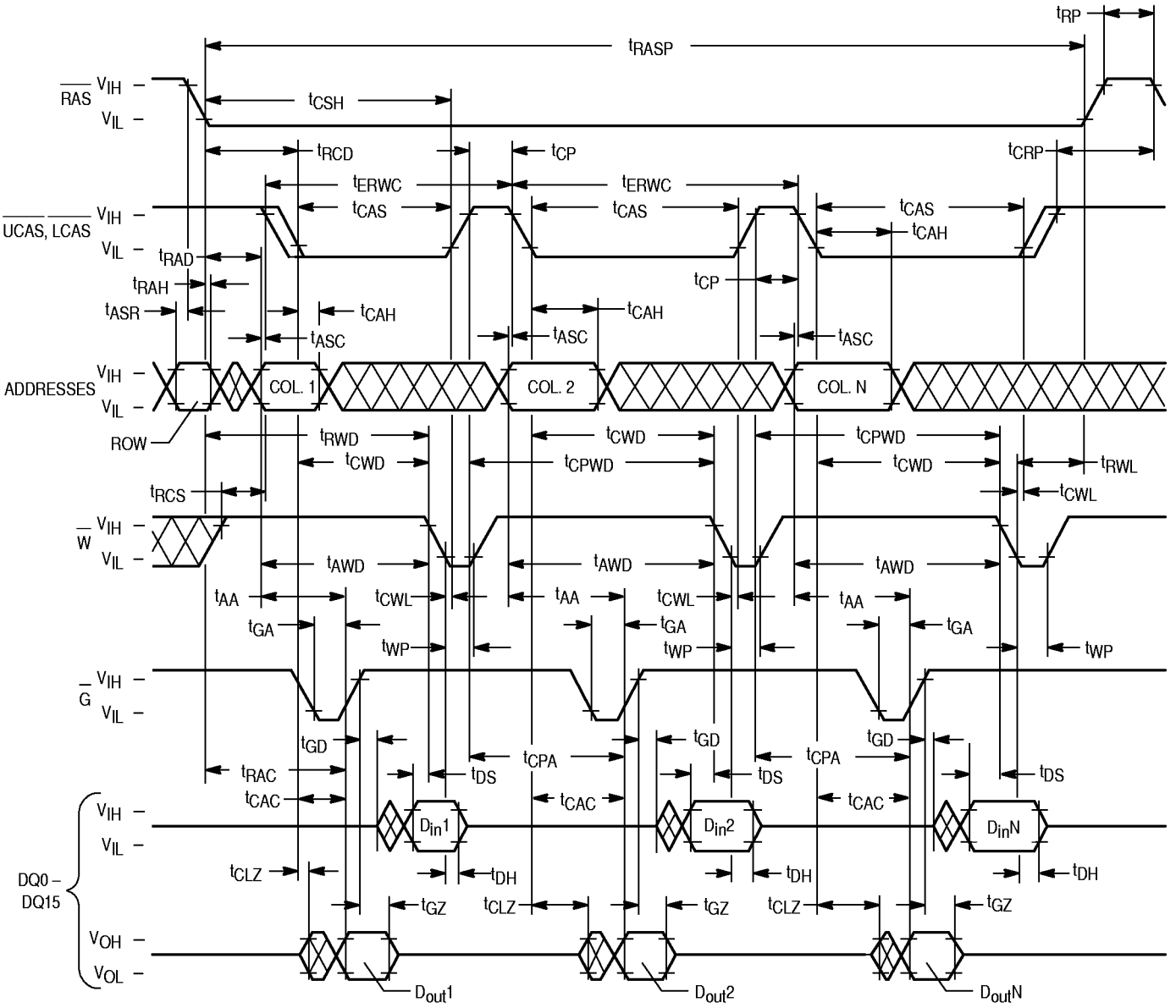
EXTENDED DATA OUT WRITE CYCLE (EARLY WRITE)



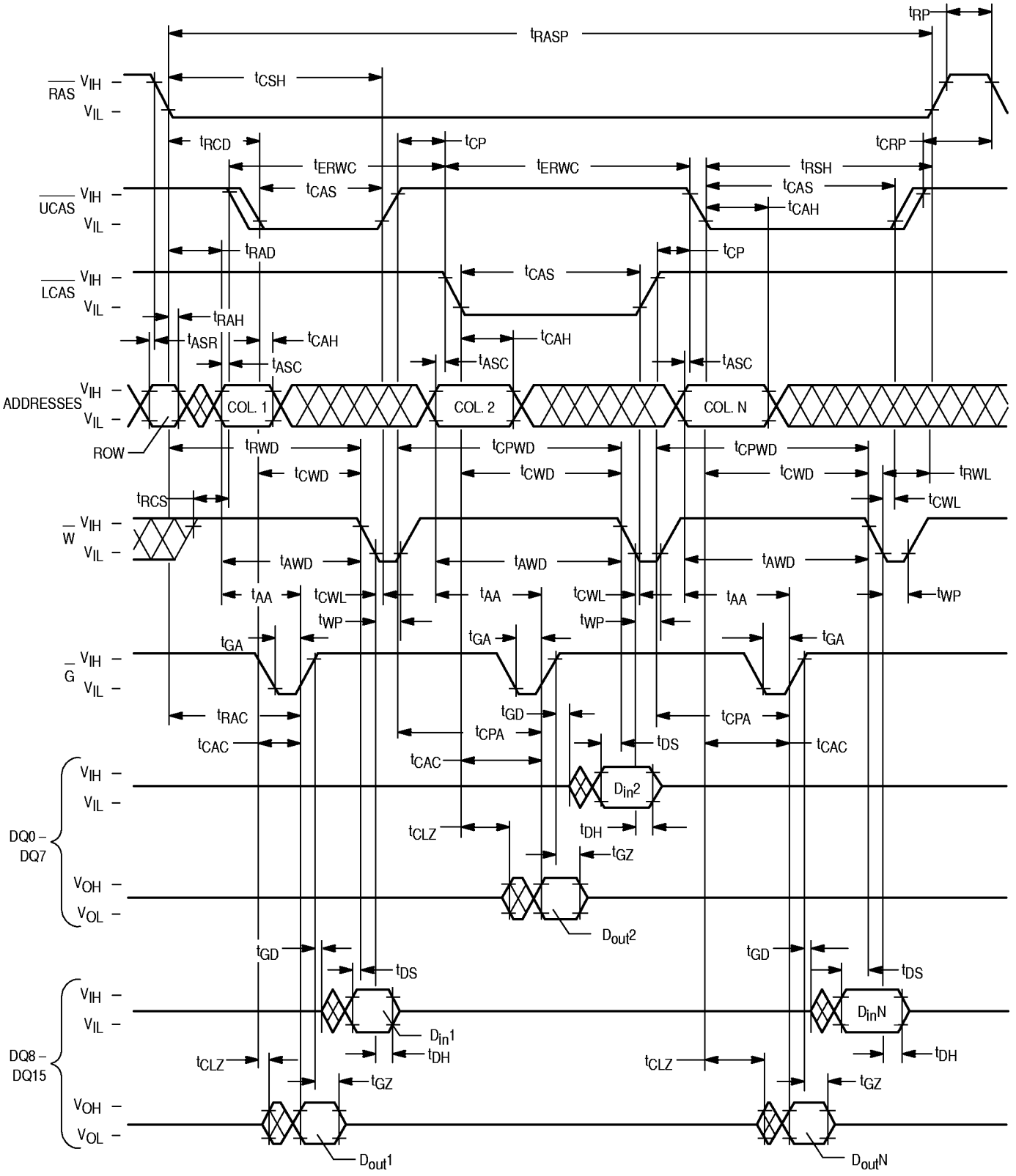
EXTENDED DATA OUT BYTE WRITE CYCLE (EARLY WRITE)



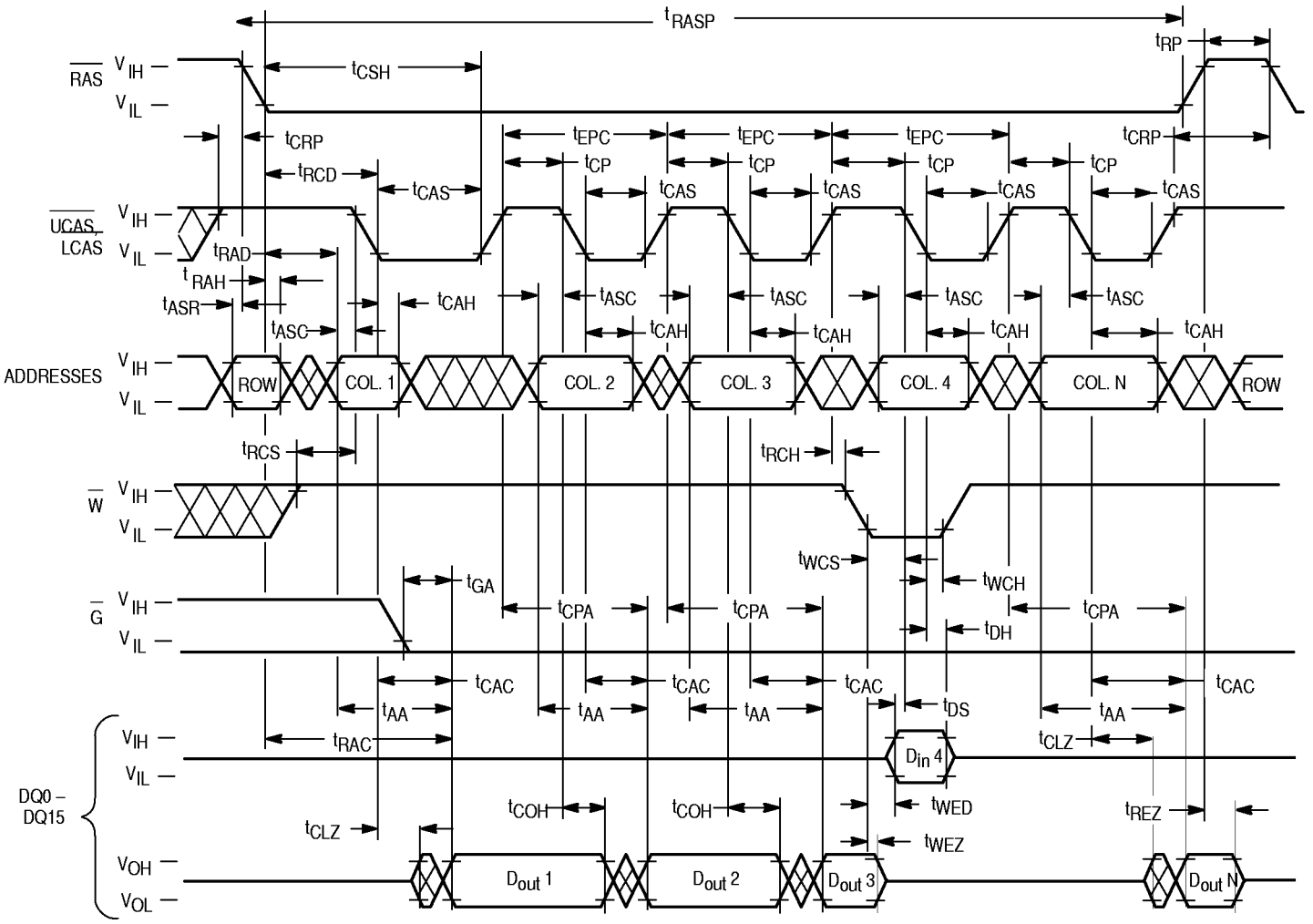
EXTENDED DATA OUT READ–WRITE CYCLE



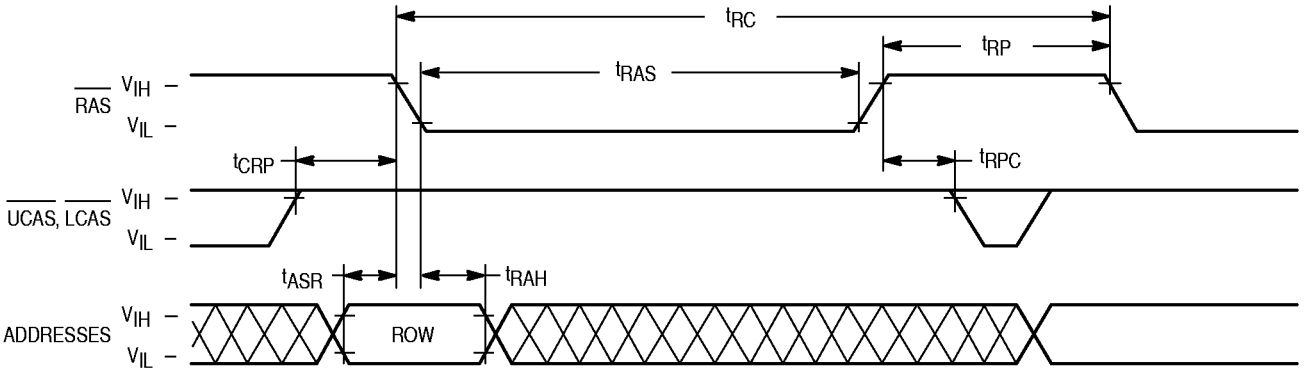
EXTENDED DATA OUT BYTE READ–WRITE CYCLE



EXTENDED DATA OUT READ WRITE MIXED CYCLE

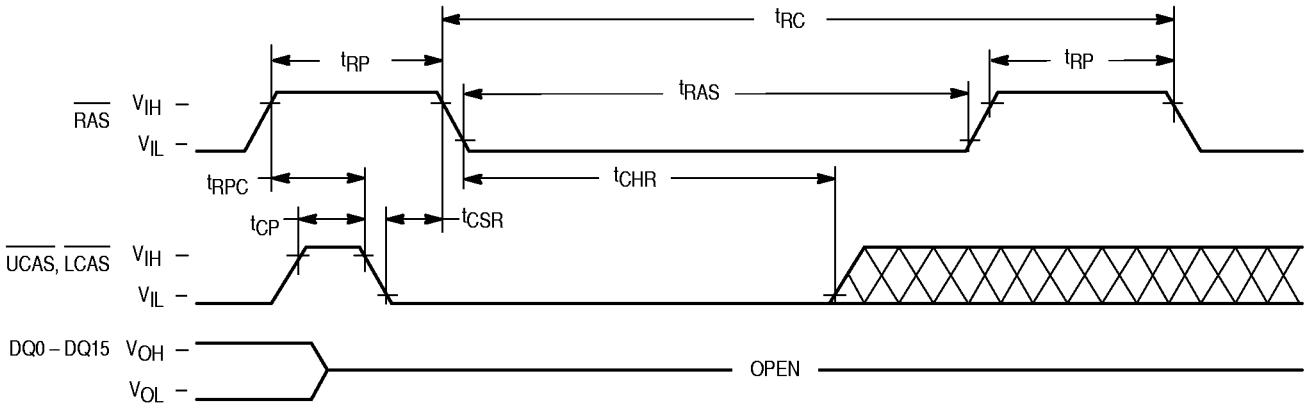


$\overline{\text{RAS}}$–ONLY REFRESH CYCLE



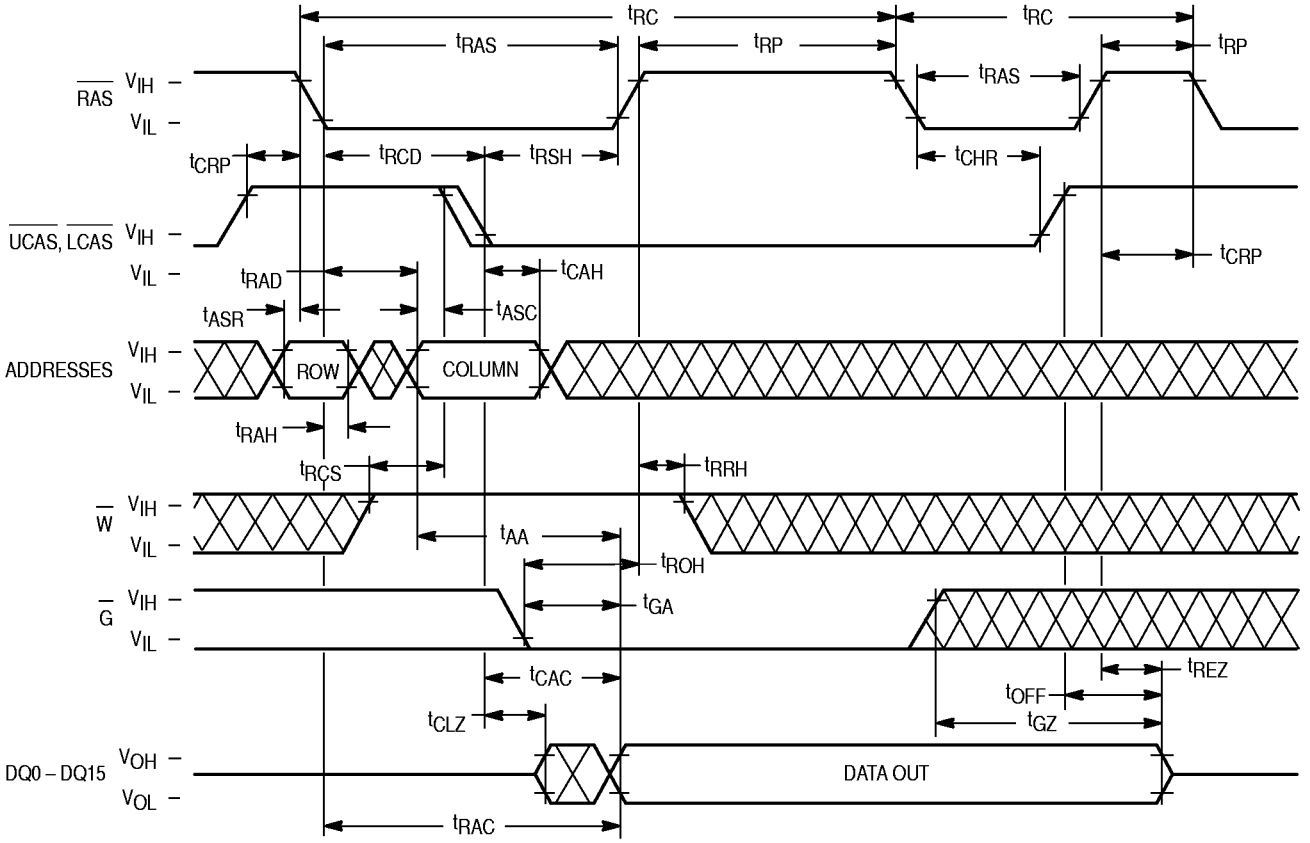
NOTE: $\overline{W}$, $\overline{G}$ = H or L
DQ0 – DQ15 = Open
Addresses: MCM516165B — A0 to A11; MCM318165CV — A0 to A9.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

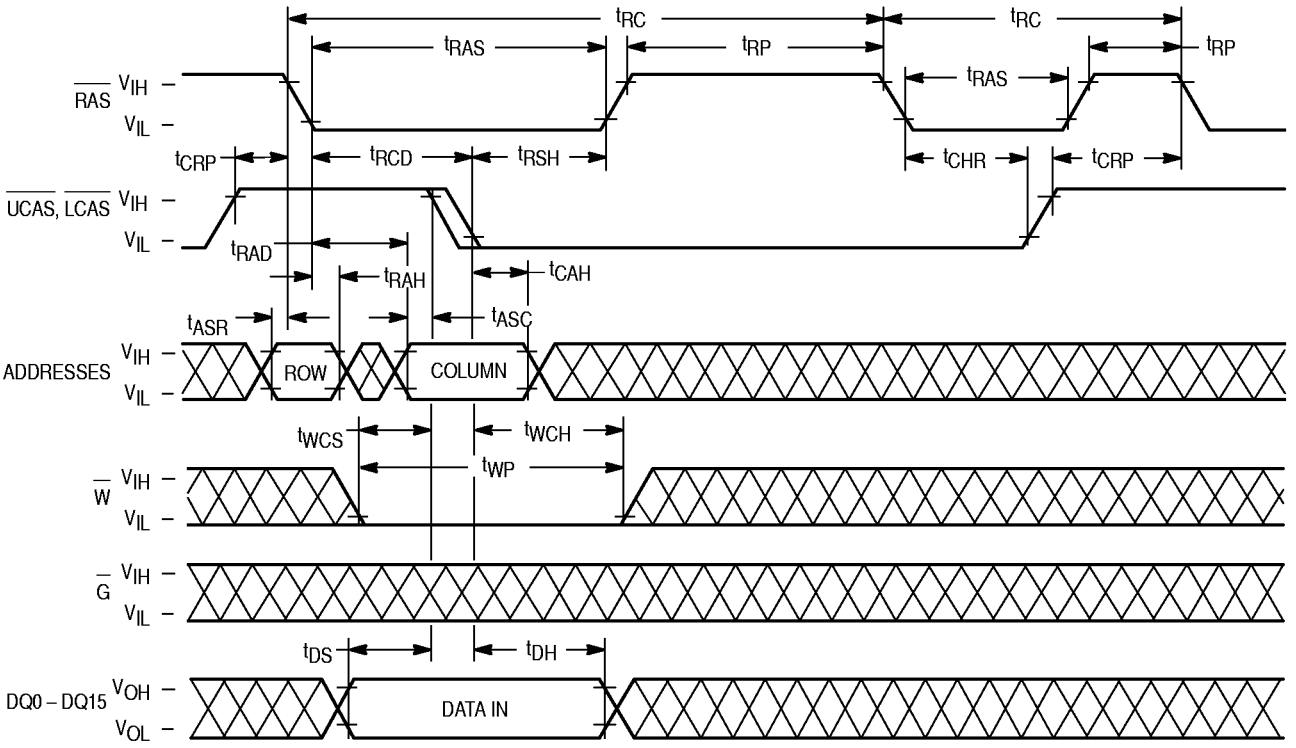


NOTE: $\overline{W}$, $\overline{G}$, Addresses= H or L
CAS before RAS refresh is performed when either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ meets this timing.

HIDDEN REFRESH CYCLE (READ)

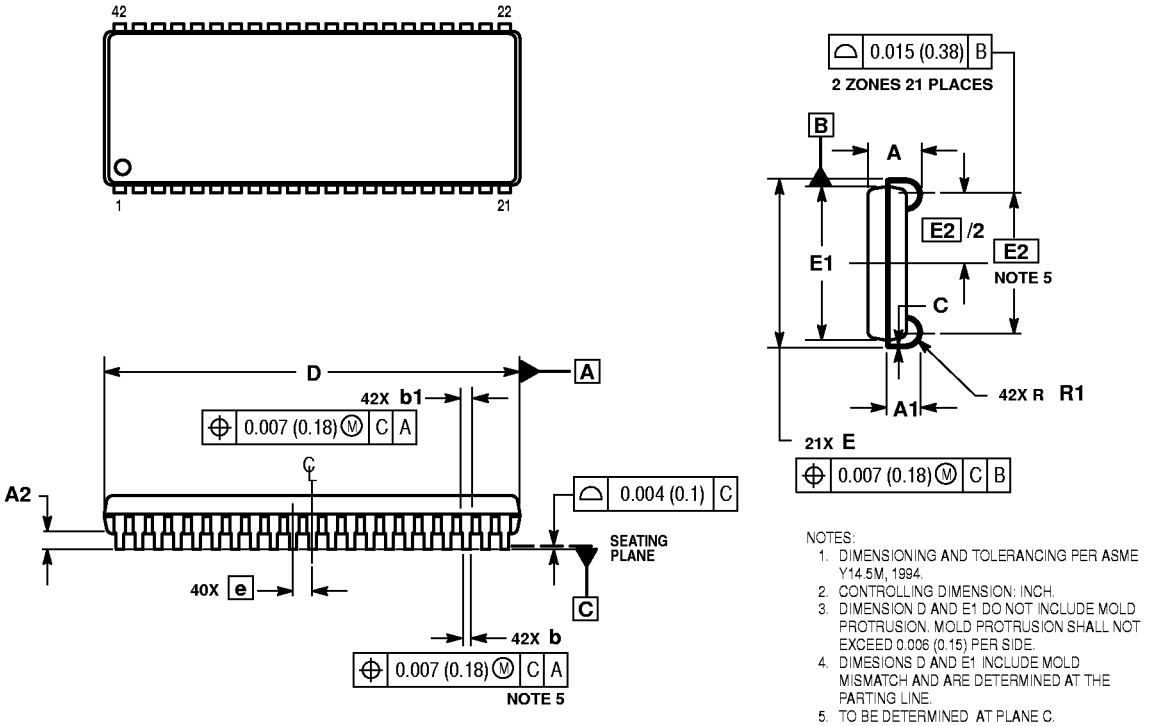


HIDDEN REFRESH CYCLE (WRITE)



PACKAGE DIMENSIONS

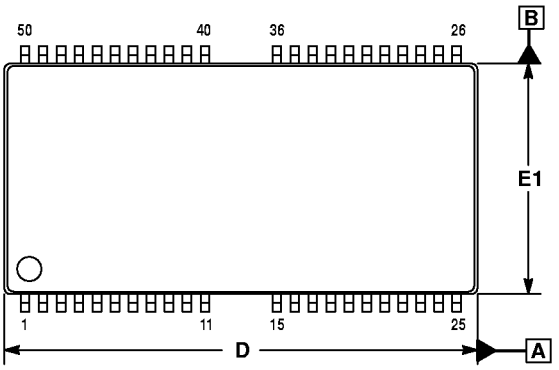
J PACKAGE
400 MIL SOJ
CASE 986B

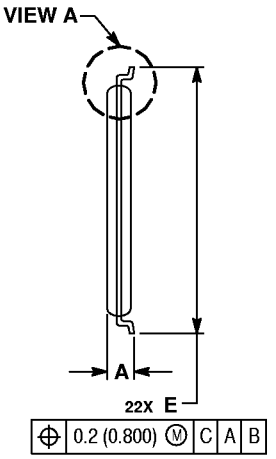


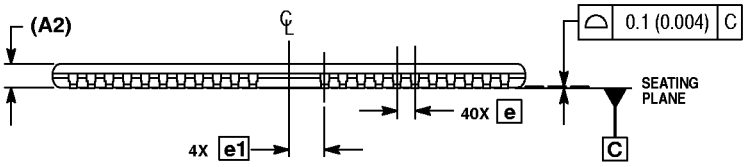
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
4. DIMESIONS D AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
5. TO BE DETERMINED AT PLANE C.
6. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSIONS . DAMBAR PROTRUSION SHALL NOT CAUSE THE b1 DIMENSION TO EXCEED 0.037 (0.94).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.128	0.148	3.25	3.76
A1	0.082	—	2.08	—
A2	0.025	—	0.64	—
b	0.015	0.020	0.38	0.50
b1	0.026	0.032	0.66	0.81
c	0.007	0.013	0.18	0.33
D	1.070	1.080	27.17	27.43
E	0.435	0.445	11.05	11.31
E1	0.395	0.405	10.04	10.29
E2	0.370 BSC		9.40 BSC	
e	0.050 BSC		1.27 BSC	
R1	0.030	0.040	0.76	1.02

T PACKAGE
400 MIL
TSOP II
CASE 985D

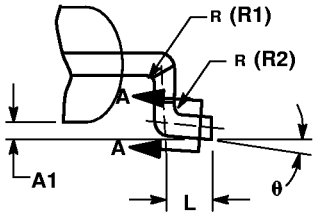




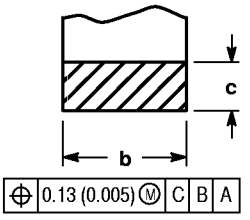


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION IS 0.15 (0.006) MAXIMUM PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.53 (0.021).
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 12, 14, 14, 37, 38, AND 39 ARE NOT USED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.20	—	0.047
A1	0.05	0.20	0.002	0.008
A2	1.00 REF		0.039 REF	
b	0.25	0.45	0.010	0.018
c	0.10	0.18	0.004	0.007
D	20.85	21.05	0.821	0.829
e	0.80 BSC		0.0315 BSC	
e1	1.60 BSC		0.063 BSC	
E	11.56	11.96	0.455	0.471
E1	10.06	10.26	0.396	0.404
L	0.40	0.60	0.016	0.024
R1	0.10 REF		0.004 REF	
R2	0.10 REF		0.004 REF	
θ	0°	10°	0°	10°

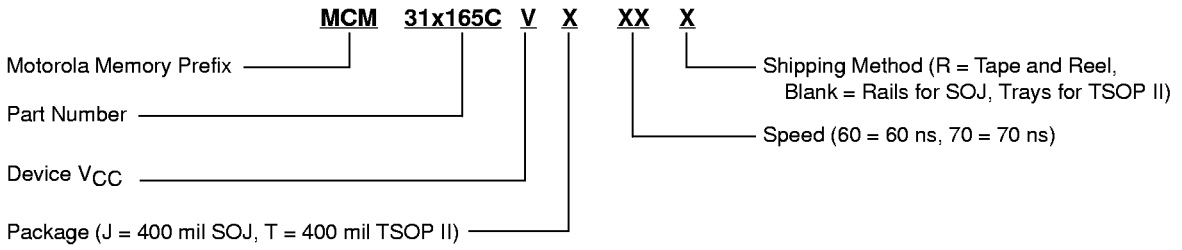


VIEW A
ROTATED 90° CW



SECTION A–A
44 PLACES

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM318165CVJ60 MCM318165CVJ60R MCM318165CVT60 MCM318165CVT60R
MCM318165CVJ70 MCM318165CVJ70R MCM318165CVT70 MCM318165CVT70R

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INTERNET: http://Design–NET.com

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