HARRIS SEMICONDUCTOR

ACTS240MS

High Reliability, Radiation Hardened High-Speed CMOS/SOS

December 1992

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose Up to 1 Mega-RAD (Si)
- Dose Rate Upset >10^{11} RADs/Sec. 20ns Pulse
- Cosmic Ray Upset Immunity < 1 x 10^{-11} Errors/Gate Day (Typ)
- Latch Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
  - CMOS Input Compatibility Ii ≤ 5μA at VOL, VOH

Description

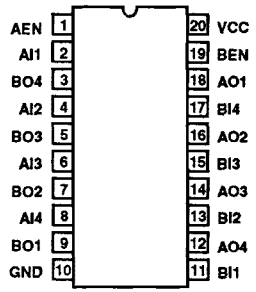
The Harris ACTS240MS is a Radiation Hardened octal inverting tri-state buffer having two active low enable inputs.

The ACTS240MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

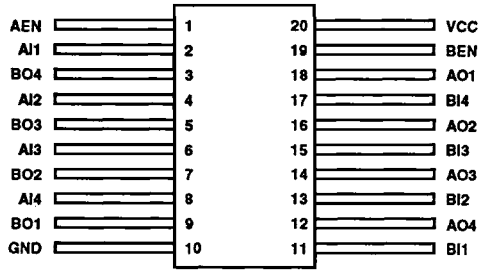
The ACTS240MS is supplied in a 20 lead Ceramic flatpack (K suffix) or a Dual-In-Line Ceramic Package (D suffix).

Pinouts

20 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 PIN CERAMIC FLAT PACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW

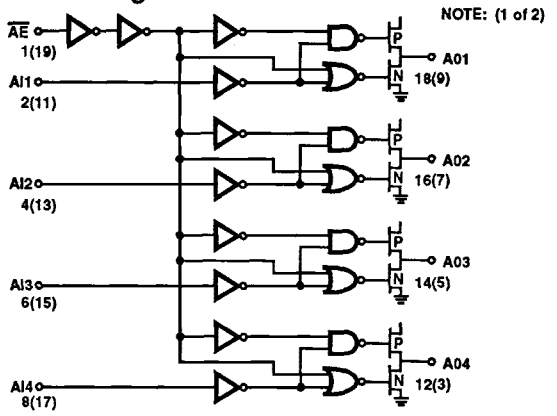


Truth Table

INPUTS		OUTPUT
$\overline{AE}$, $\overline{BE}$	AIn, BIn	AOn, BOn
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3186**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +6.0V
Input Voltage Range, All Inputs ..... -0.5V to VCC +0.5V
DC Input Current, Any One Input ..... ±10mA
DC Drain Current, Any One Output ..... ±50mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +265°C
Junction Temperature (TJ) ..... +175°C
ESD Classification ..... Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
DIC	75°C/W	16°C/W
Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C ..... Derate Linearly at 12mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage ..... +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) ..... 10ns/V Max
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0.0V to 0.8V
Input High Voltage (VIH) ..... VCC to VCC/2

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0 (Note 2)	1	+25°C	16	-	mA
			2, 3	+125°C, -55°C	12	-	
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V VIL = 0 (Note 2)	1	+25°C	-16	-	mA
			2, 3	+125°C, -55°C	-12	-	
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, IOL = 50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, IOH = -50µA, VIL = 0V	1, 2, 3	+25°C, +125°C, -55°C	VCC-0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C	-	±35	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = VCC/2, VIL = 0.8V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTE:

1. All voltage referenced to device GND.
2. Force/Measure function may be interchanged.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH	VCC = 4.5V, VIH = 3V, VIL = 0V	9	+25°C	1	8.5	ns
			10, 11	+125°C, -55°C	1	9.5	
	TPHL		9	+25°C	1	11.5	ns
			10, 11	+125°C, -55°C	1	13.0	
Tri-State Test	TPZL	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	2	14.0	ns
			10, 11	+125°C, -55°C	2	16.0	
	TPZH		9	+25°C	2	10.5	ns
			10, 11	+125°C, -55°C	2	11.5	
	TPLZ	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	2	14.0	ns
			10, 11	+125°C, -55°C	2	14.5	
	TPHZ		9	+25°C	2	14.5	ns
			10, 11	+125°C, -55°C	2	15.5	
Output Transition Time	TTLH	VCC = 4.5V, VIH = 3V, VIL = 0	9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	
	TTHL		9	+25°C	1	5.0	ns
			10, 11	+125°C, -55°C	1	5.0	

NOTES:

1. All voltage referenced to device GND.
2. Measurements made with CL = 50pF, RL = 500Ω, Input TR = TF = 3ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	Typical 40		pF
			1	+125°C	Typical 40		pF
Input Capacitance	CIN	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	18	pF
			1	+125°C	-	18	pF
Output Capacitance	COUT	VCC = 5V, VIH = 5V, VIL = 0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	1 MEG LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VIN = 5.5V, VIN = VCC or GND	+25°C	-	0.4	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0, (Note 2)	+25°C	12	-	mA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0, (Note 2)	+25°C	-12	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOL = 50µA	+25°C	-	0.1	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOL = 50µA		-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 4.5V, VIL = 0V, IOH = -50µA	+25°C	VCC-0.1	-	V
		VCC = 5.5V, VIH = 5.5V, VIL = 0V, IOH = -50µA		VCC-0.1	-	V
Tri-State Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional	FN	VCC = 4.5V, VIL = 0.8V, VIH = VCC/2 (Note 3)	+25°C	-	-	-
Propagation Delay	TPLH	VCC = 4.5V, VIH = 3V, VIL = 0V	+25°C	1	9.5	ns
	TPHL			1	13	ns
Tri-State Test	TPZL	VCC = 4.5V, VIH = 3V, VIL = 0V	+25°C	2	16	ns
	TPZH			2	11.5	ns
	TPLZ			2	14.5	ns
	TPHZ			2	15.5	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	±4µA
IOL/IOH	5	±15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/6005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A testing in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	1, 2, 4, 6, 8, 10, 11, 13, 15, 17, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 5, 7, 9, 12, 14, 16, 18	10	-	1, 2, 4, 6, 8, 11, 13, 15, 17, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 1)					
-	1, 10, 19	3, 5, 7, 9, 12, 14, 16, 18	20	-	2, 4, 6, 8, 11, 13, 15, 17

NOTES:

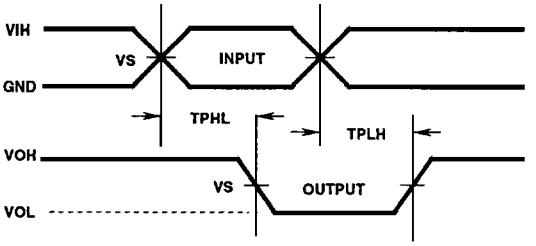
1. Each pin except VCC and GND will have a resistor of 680KΩ ± 5% for burn-in.

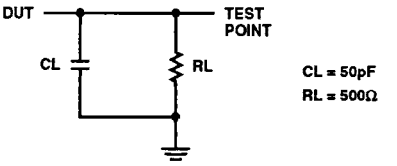
TABLE 9. RADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 5, 7, 9, 12, 14, 16, 18	6, 8, 10, 15, 17, 19	1, 2, 4, 11, 13, 20

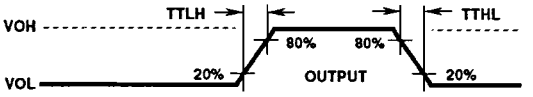
NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Propagation Delay Timing Diagram and Load Circuit





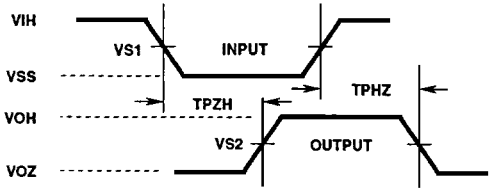
Transition Timing Diagram

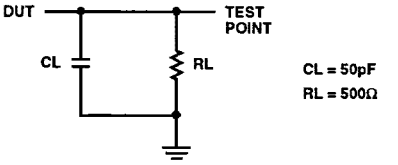


AC VOLTAGE LEVELS

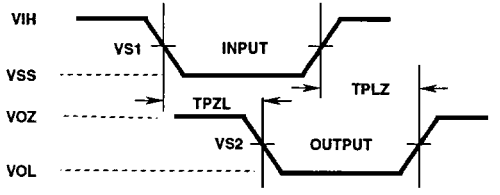
PARAMETER	ACTS	UNITS
VCC	4.50	V
VIH	3.00	V
VIL	0.0	V
VS	1.30	V
GND	0.0	V

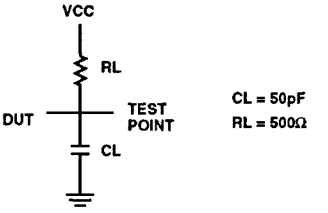
Tri-State High Timing Diagram and Load Circuit





Tri-State Low Timing Diagram and Load Circuit





TRI-STATE VOLTAGE LEVELS

	TPLH	TPHL	TPZL	TPZH	TPHZ	TPLZ
VIH	3V	3V	3V	3V	3V	3V
VS1	1.3V	1.3V	1.3V	1.3V	1.3V	1.3V
VS2	1.3V	1.3V	1.3V	1.3V	80% VCC	20% VCC
VIL	GND	GND	GND	GND	GND	GND

Die Characteristics

DIE DIMENSIONS:
100 x 100 mils
2.54 x 2.54 mm

METALLIZATION:
Type: AlSiCu
Metal 1 Thickness: 7.5kÅ ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Glass

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
110µm x 110µm
4.4 mils x 4.4 mils

Metallization Mask Layout

ACTS240MS