MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Order this document
by MCM516165BV/D

1M x 16

MCM516165BV
EDO
4096 Cycle Refresh

MCM518165BV
EDO
1024 Cycle Refresh

Advance Information

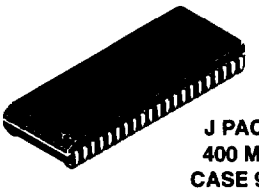
16M CMOS Wide DRAM Family

EDO, 1M x 16, 1K, and 4K Refresh

The family of 16M Dynamic RAMs is fabricated using 0.50µ CMOS high–speed silicon–gate process technology. It includes devices organized as 1,048,576 sixteen–bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The x16 with 4096 cycle refresh (MCM516165BV) require 12 address lines (12 rows, 8 columns), while the x16 device with 1024 cycle refresh (MCM518165BV) require only 10 address lines (10 rows, 10 columns).

These devices are packaged in a standard 400 mil J–lead small outline package (SOJ) and a standard 400 mil thin–small–outline package (TSOP).



J PACKAGE
400 MIL SOJ
CASE 986A–01

T PACKAGE
400 MIL TSOP II
CASE 985A–01

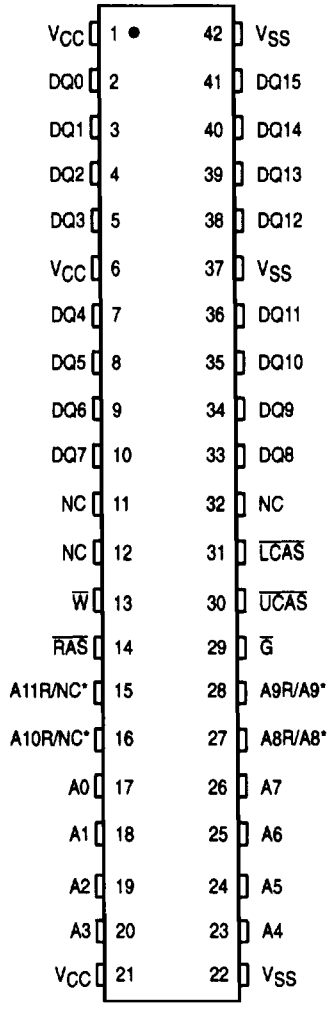
- Single 3.3 V ± 0.3 V Power Supply
- Three–State Data Outputs, x16 Configuration
- Extended Data Out (EDO)
- TTL–Compatible Inputs and Outputs
- $\overline{RAS}$–Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 4096 Cycle Refresh:
  MCM516165BV = 64 ms
- 1024 Cycle Refresh:
  MCM518165BV = 16 ms
- Fast Access Time (t_{RAC}):
  MCM51xxxxBV–60 = 60 ns (Max)
  MCM51xxxxBV–70 = 70 ns (Max)
- Low Active Power Dissipation:
  MCM516165BV–60 = 324 mW (Max)
  MCM516165BV–70 = 270 mW (Max)
  MCM518165BV–60 = 630 mW (Max)
  MCM518165BV–70 = 522 mW (Max)
- Low Standby Power Dissipation:
  All Devices = 3.6 mW (Max, TTL Levels)
  All Devices = 1.8 mW (Max, CMOS Levels)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

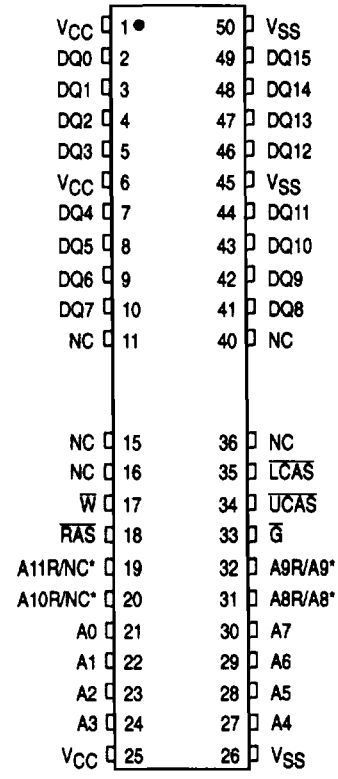
3/96

PIN ASSIGNMENTS

400 MIL SOJ



400 MIL TSOP

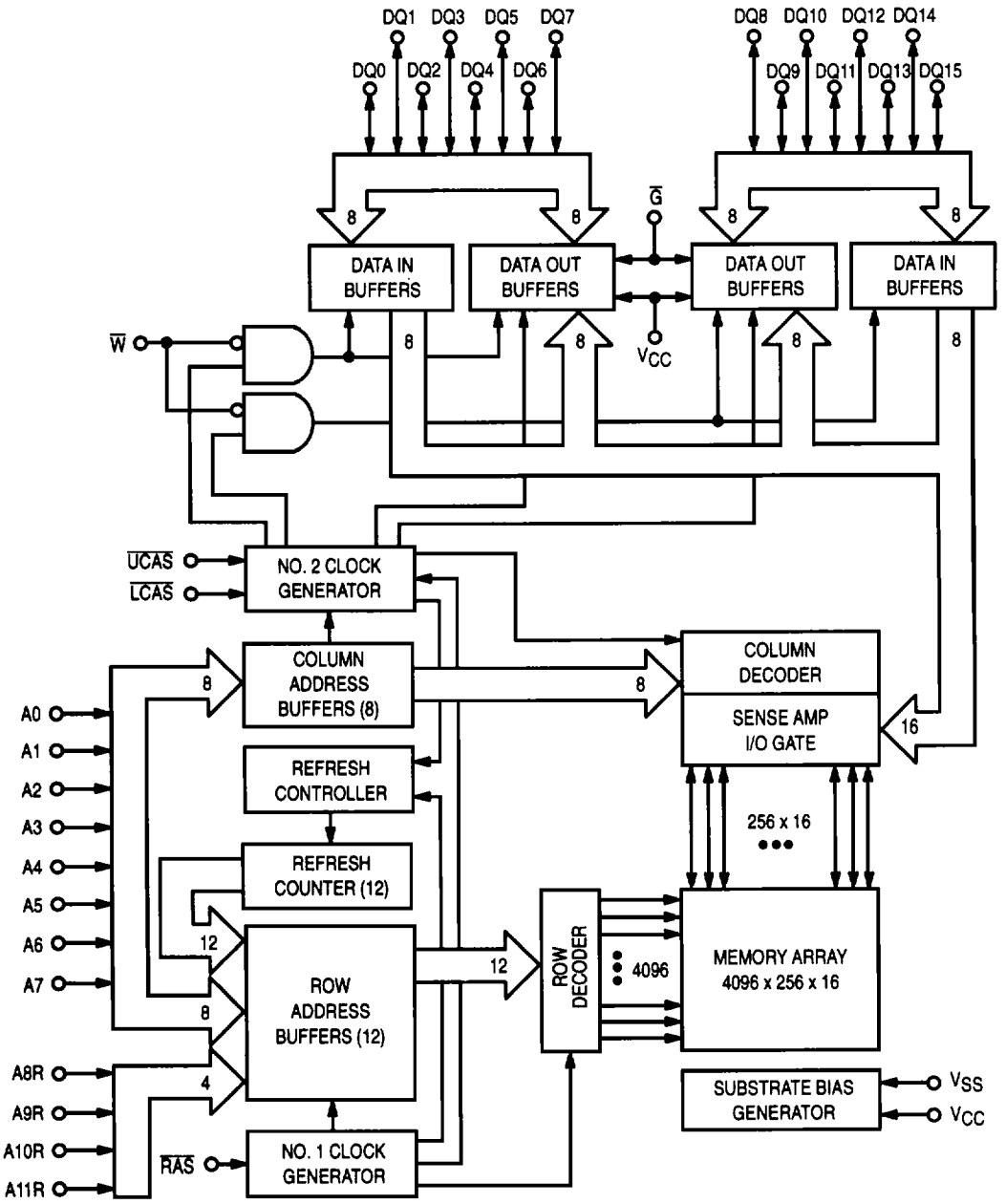


*4096 Cycle Refresh or 1024 Cycle Refresh (R Suffix = Row Address)

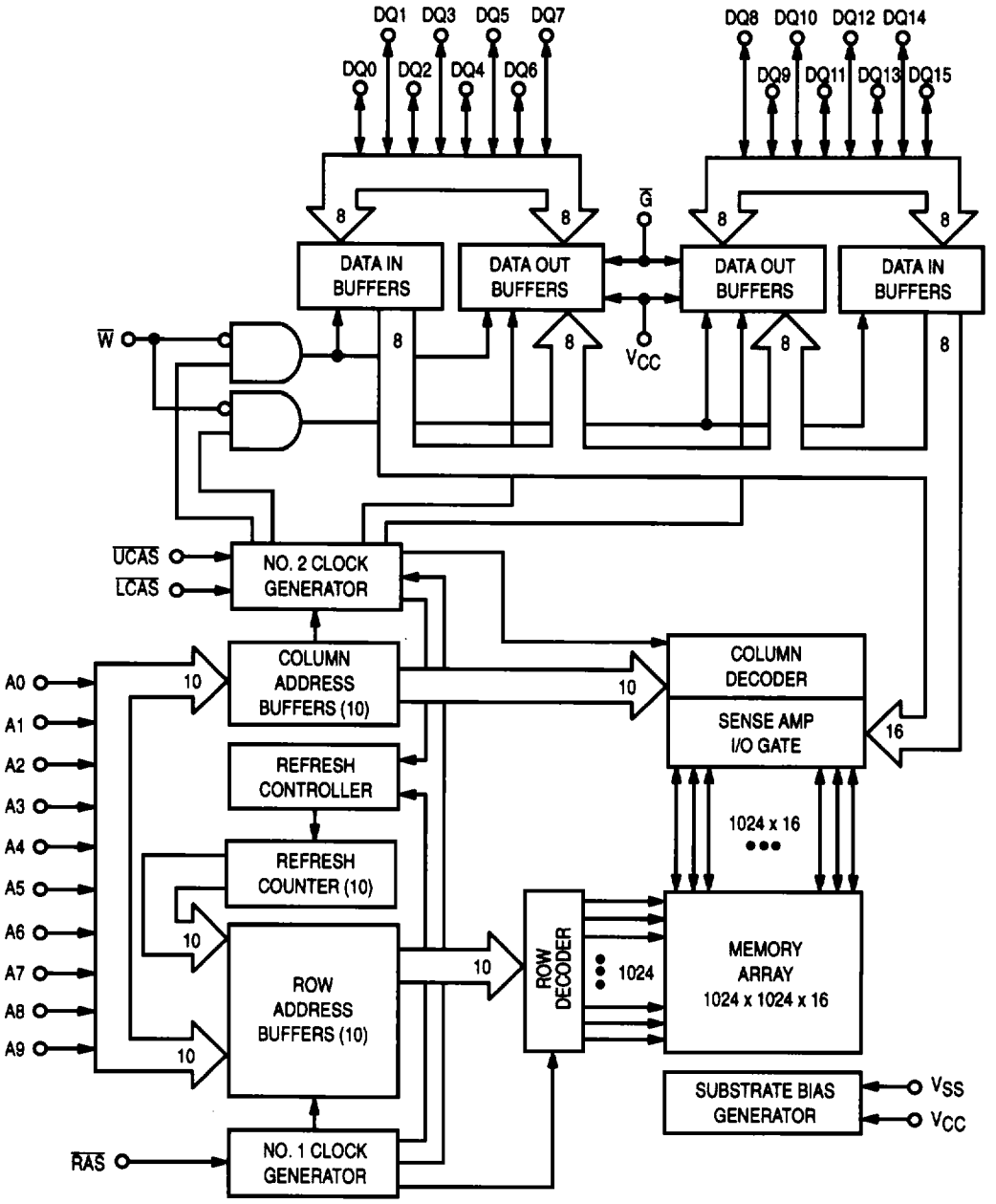
PIN NAMES	
A0 – A11 ..... Address Input	LCAS ..... Column Address Strobe
DQ0 – DQ15 ..... Data Input/Output	UCAS ..... Column Address Strobe
G ..... Output Enable	VCC ..... Power Supply (+ 3.3 V)
W ..... Read/Write Enable	VSS ..... Ground
RAS ..... Row Address Strobe	NC ..... No Connection

BLOCK DIAGRAMS

MCM516165BV BLOCK DIAGRAM
1M x 16, 4096 CYCLE REFRESH



MCM518165BV BLOCK DIAGRAM
1M x 16, 1024 CYCLE REFRESH



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	– 0.3 to + 4.6	V
Voltage Relative to V_{SS}, Any Pin Except V_{CC}		V_{in}, V_{out}	– 0.3 to V_{CC} + 0.3	V
Data Out Current		I_{out}	50	mA
Soldering Temperature x Time		T_{solder}	260 x 10	°C x s
Power Dissipation	MCM516165BV MCM518165BV	P_D	600 800	mW
Operating Temperature Range		T_A	0 to + 70	°C
Storage Temperature Range		T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.3**	—	0.8	V

* V_{CC} + 1.2 V at pulse width ≤ 20 ns.
** – 1.2 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages referenced to V_{SS})

Characteristic		Symbol	MCM516165BV–60 MCM518165BV–60		MCM516165BV–70 MCM518165BV–70		Unit	Notes
			Min	Max	Min	Max		
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min)	MCM516165BV–xx MCM518165BV–xx	I_{CC1}	— —	90 175	— —	75 145	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH})		I_{CC2}	—	1	—	1	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}, t_{RC} = t_{RC} Min)	MCM516165BV–xx MCM518165BV–xx	I_{CC3}	— —	90 175	— —	75 145	mA	1, 2
V_{CC} Power Supply Current During Extended Data Out Cycle ($\overline{RAS}$ = V_{IL})		I_{CC4}	— —	85 110	— —	75 100	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{CC} – 0.2 V)		I_{CC5}	—	0.5	—	0.5	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (t_{RC} = t_{RC} Min)	MCM516165BV–xx MCM518165BV–xx	I_{CC6}	— —	90 175	— —	75 145	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(I)}$	–10	10	–10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ V_{CC}, Output Disable)		$I_{lkg(O)}$	–10	10	–10	10	µA	
Output High Voltage (I_{OH} = – 2 mA)		V_{OH}	2.4	—	2.4	—	V	
Output Low Voltage (I_{OL} = 2 mA)		V_{OL}	—	0.4	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Address may be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less during t_{EPC}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 3.3 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A11	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$		7	
Input/Output Capacitance ($\overline{UCAS}$, $\overline{LCAS}$ = V_{IH} to Disable Output)	DQ0 – DQ15	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM516165BV–60 MCM518165BV–60		MCM516165BV–70 MCM518165BV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	104	—	124	—	ns	5
Read–Write Cycle Time	t_{RELREL}	t_{RWC}	135	—	157	—	ns	5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7, 11, 12
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	17	—	20	ns	6, 8, 11
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9, 12
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	ns	10, 16
Transition Time (Rise and Fall)	t_T	t_T	1	50	1	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	40	—	50	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	10	10 k	12	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	14	43	14	50	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	12	30	12	35	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	12	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed. If using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, instead of 8 $\overline{RAS}$ only refresh cyces are required.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min), t_{RWC} (min), and t_{EPC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 1 TTL (– 2 mA, + 2 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max), t_{REZ} (max), t_{WEZ} (max), and t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (Continued)

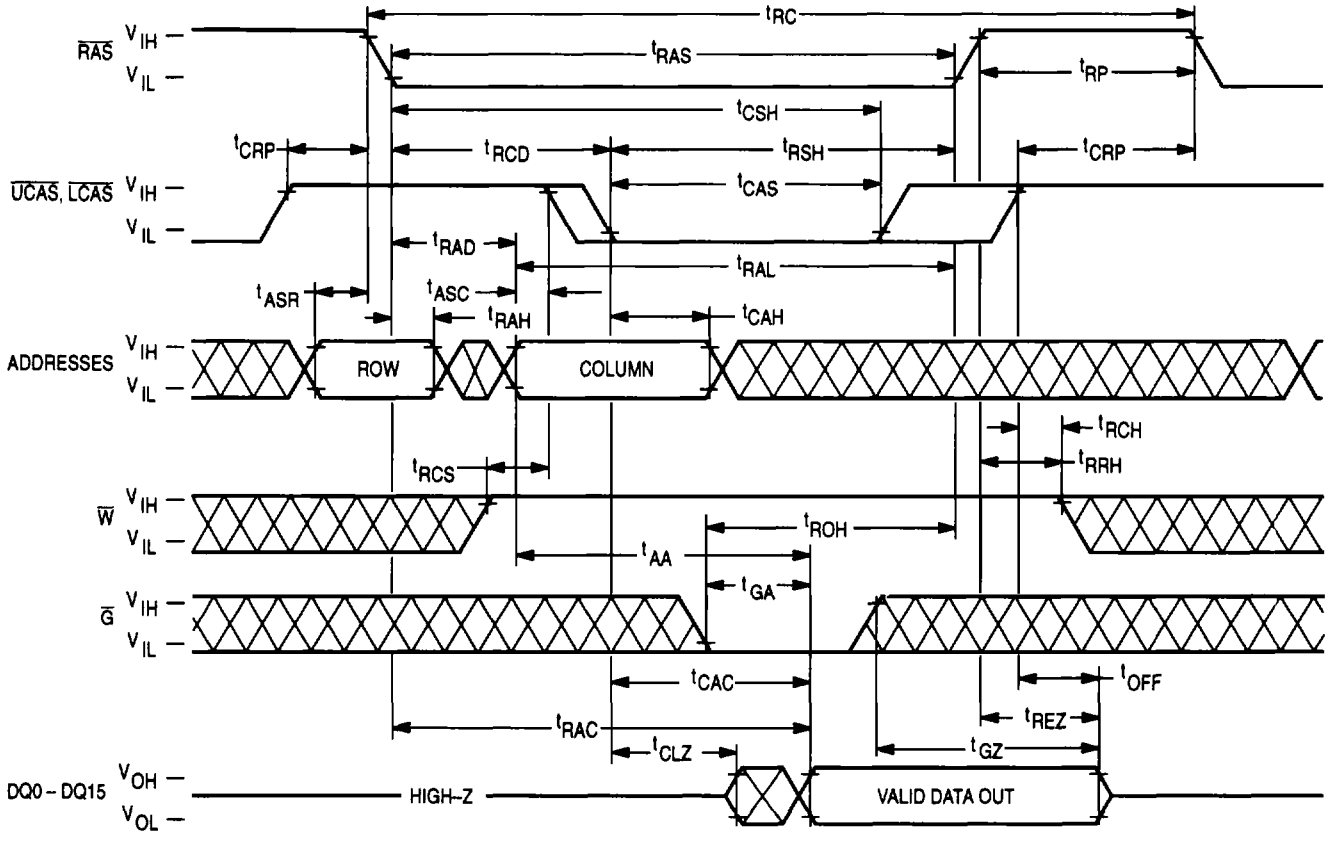
Parameter	Symbol		MCM516165BV–60 MCM518165BV–60		MCM516165BV–70 MCM518165BV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	12	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	12	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	10	—	12	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	10	—	12	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	12	—	ns	14
Refresh Period MCM516165BV MCM518165BV	t_{RVRV}	t_{RFSH}	— —	64 16	— —	64 16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	36	—	39	—	ns	15
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	79	—	89	—	ns	15
Column Address to Write Delay	t_{AVWL}	t_{AWD}	49	—	54	—	ns	15
$\overline{CAS}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	54	—	59	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{CELCEL}	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	15	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	20	—	20	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	15	—	20	ns	6
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	15	—	15	—	ns	
Output Buffer Turn–Off Delay from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	15	0	15	ns	10
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	10	—	12	—	ns	
Output Disable Setup Time	t_{GHCEL}	t_{GDS}	0	—	0	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Extended Data Out)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{RAS}$ Pulse Width (Extended Data Out)	t_{RELREH}	t_{RASP}	60	100 k	70	100 k	ns	
$\overline{RAS}$ to Next $\overline{CAS}$ Delay (Extended Data Out)	t_{RELCEL}	t_{RNCD}	60	—	70	—	ns	
Extended Data Out Cycle Time	t_{CELCEL}	t_{EPC}	25	—	30	—	ns	
Extended Data Out Read–Write Cycle Time	t_{CELCEL}	t_{ERWC}	68	—	75	—	ns	
Output Data Hold Time	t_{CELQZ}	t_{COH}	5	—	5	—	ns	
Output Buffer Turn–Off Delay from $\overline{RAS}$	t_{REHQZ}	t_{REZ}	0	15	0	15	ns	10, 16
Output Buffer Turn–Off Delay from $\overline{WE}$	t_{WLQZ}	t_{WEZ}	0	15	0	15	ns	10
$\overline{WE}$ to Data Delay	t_{WLDV}	t_{WED}	15	—	15	—	ns	
$\overline{G}$ to Pulse Width	t_{GLGH}	t_G	15	—	20	—	ns	
$\overline{G}$ Precharge Time	t_{GHGL}	t_{GP}	10	—	12	—	ns	
$\overline{CAS}$ to $\overline{G}$ Precharge Time	t_{CEHGL}	t_{CPG}	5	—	5	—	ns	

NOTES:

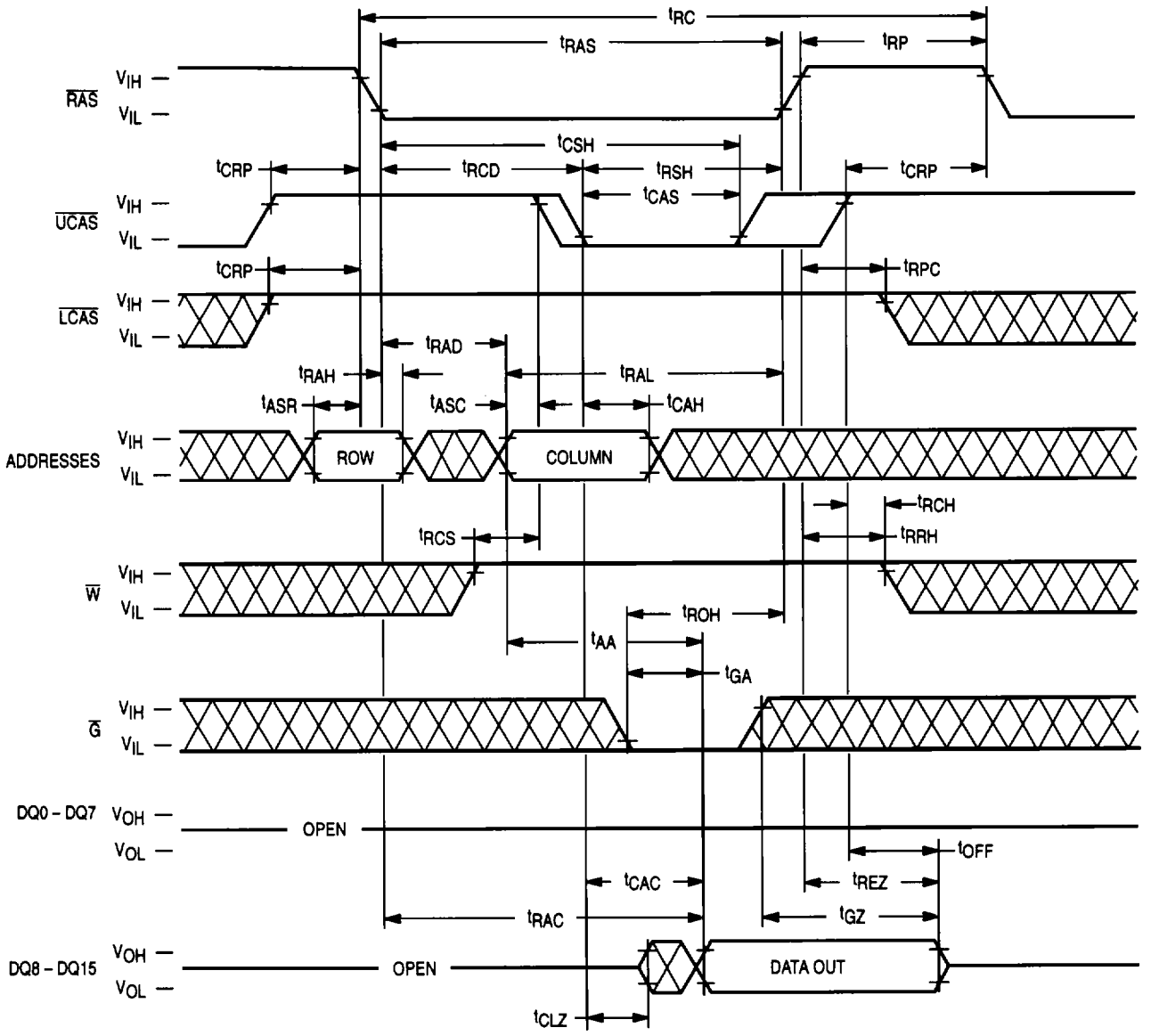
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write or read–write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (extended data out), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the open circuit condition is controlled by $\overline{CAS}$ going high (t_{OFF}). If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the open circuit condition is controlled by $\overline{RAS}$ going high (t_{REZ}).

TIMING DIAGRAMS

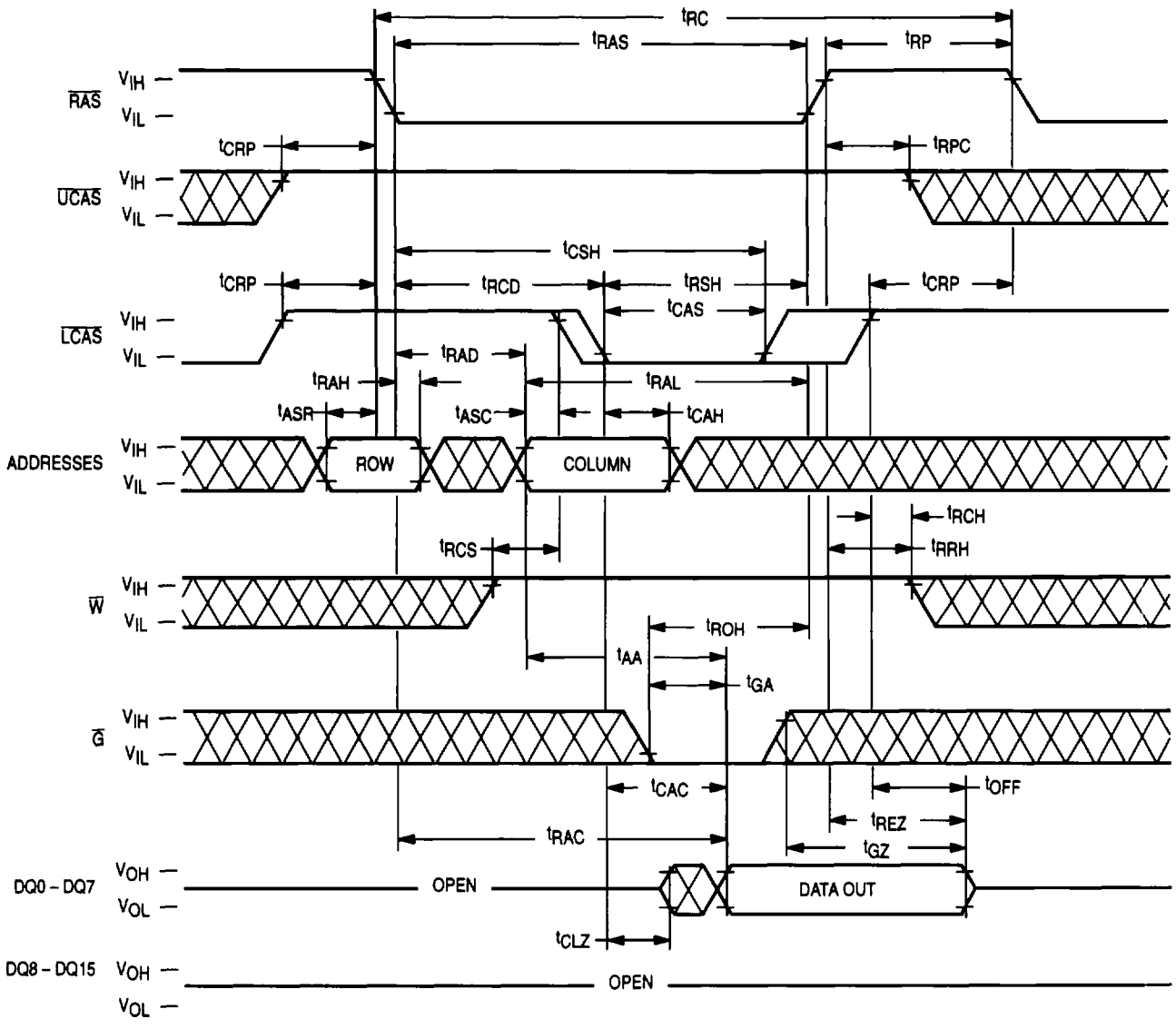
READ CYCLE



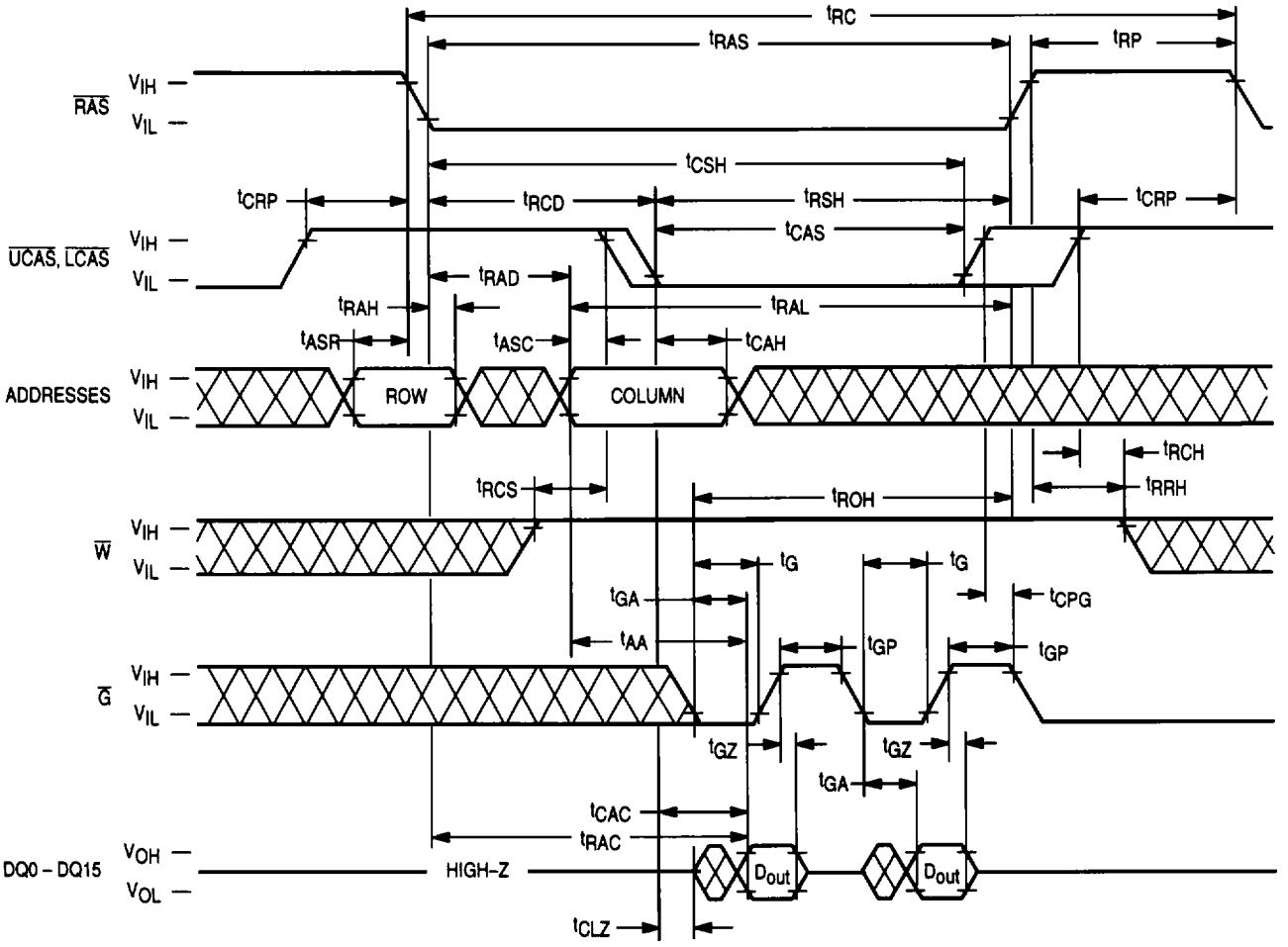
UPPER BYTE READ CYCLE



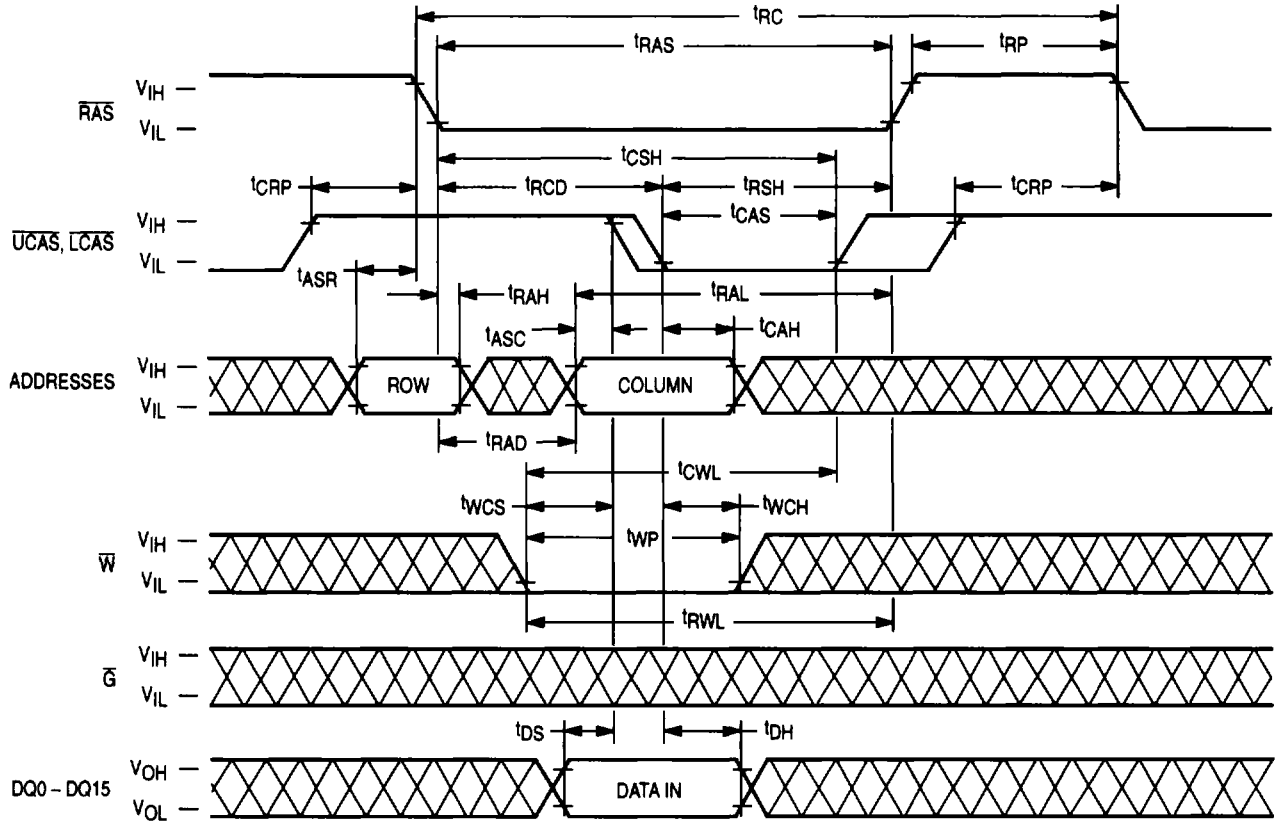
LOWER BYTE READ CYCLE



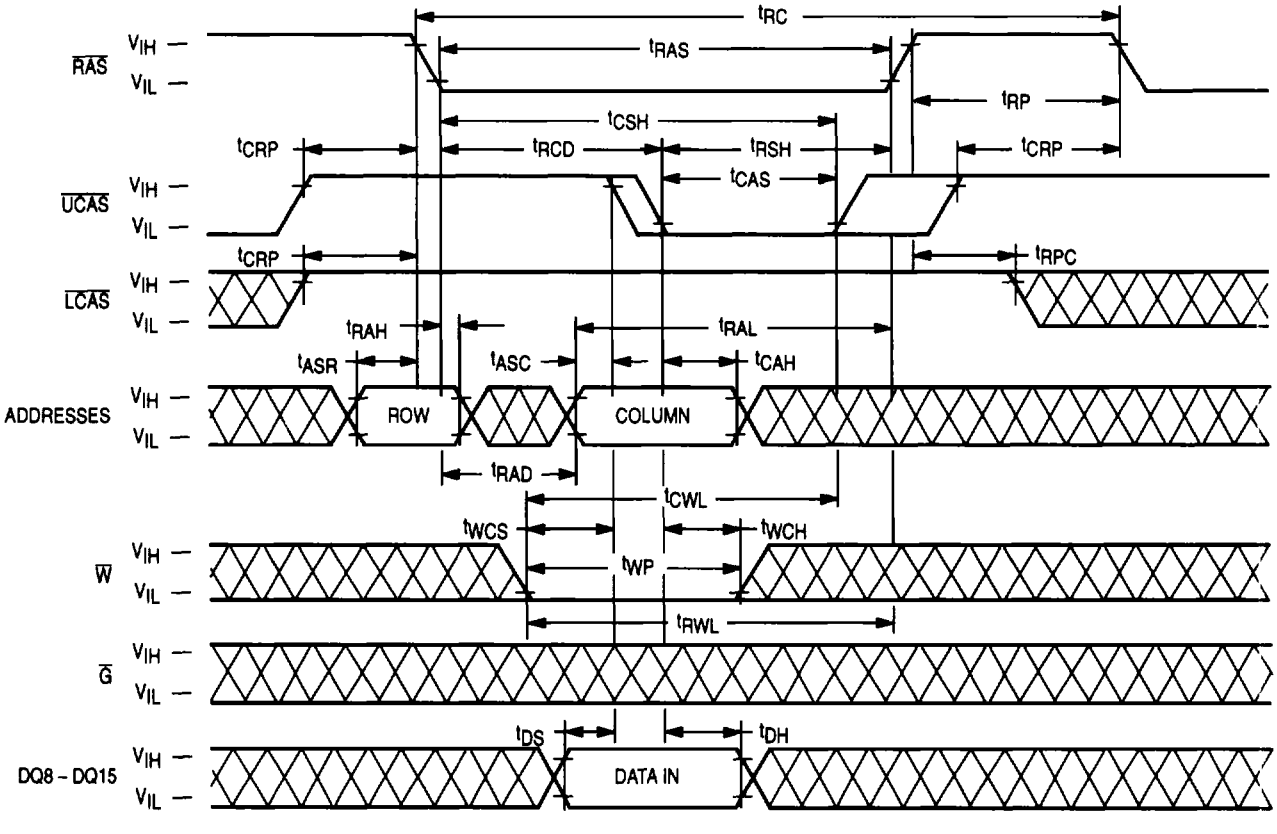
READ CYCLE ($\overline{G}$ CONTROLLED READ)



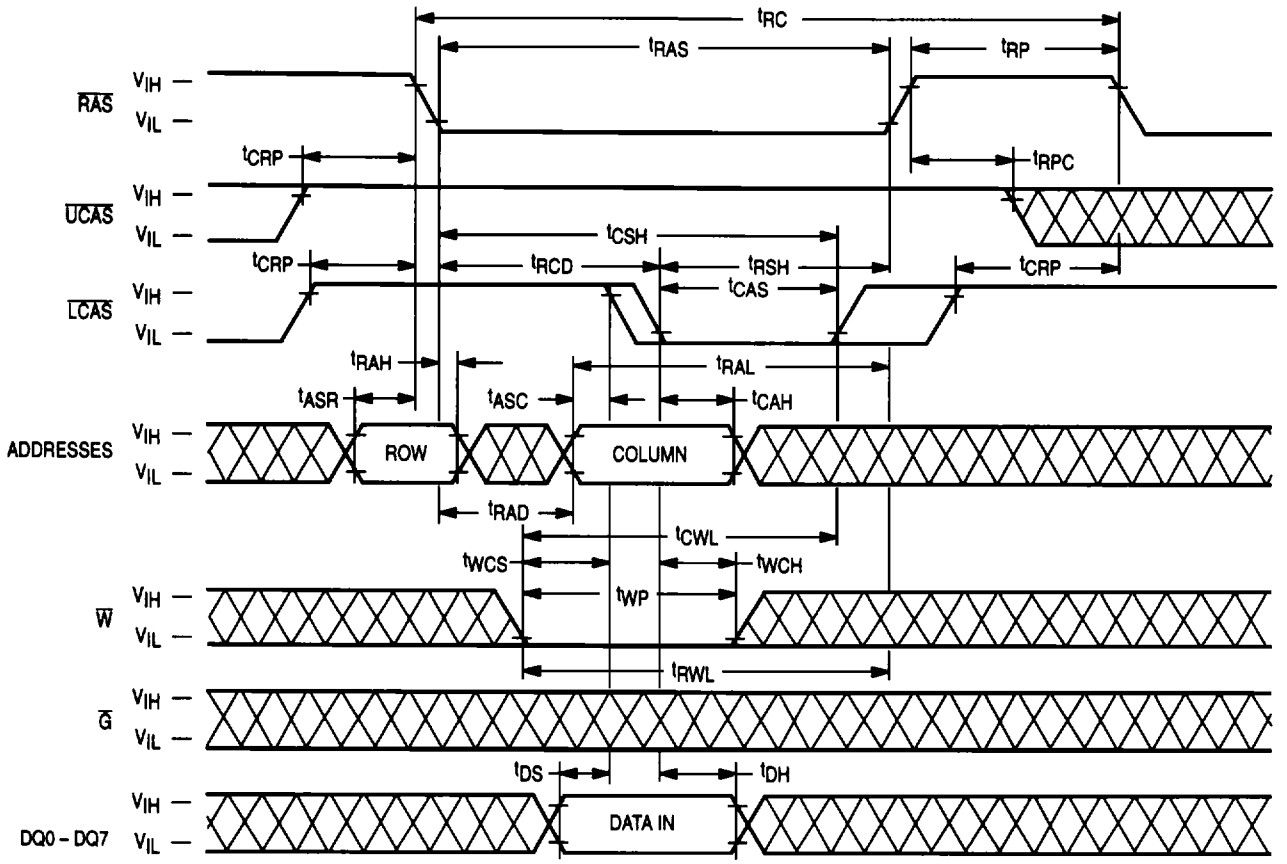
WRITE CYCLE (EARLY WRITE)



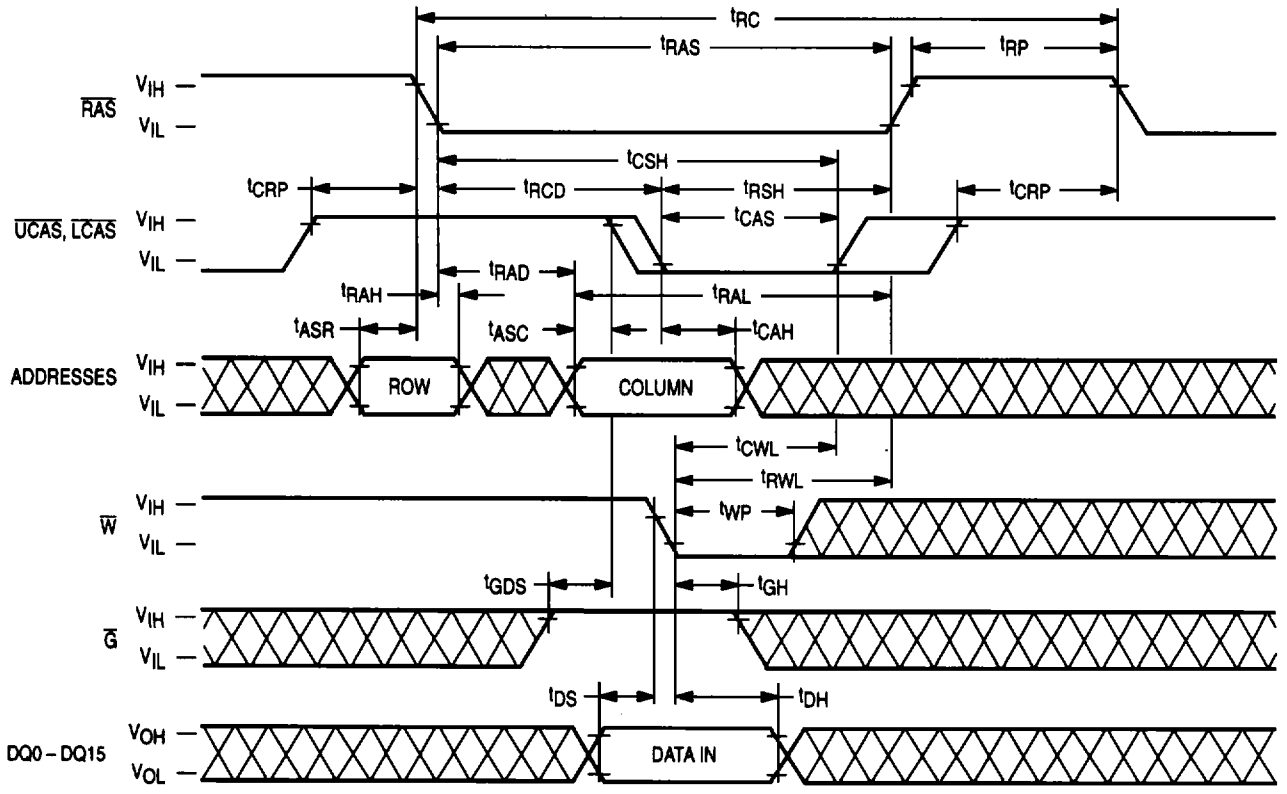
UPPER BYTE WRITE CYCLE (EARLY WRITE)



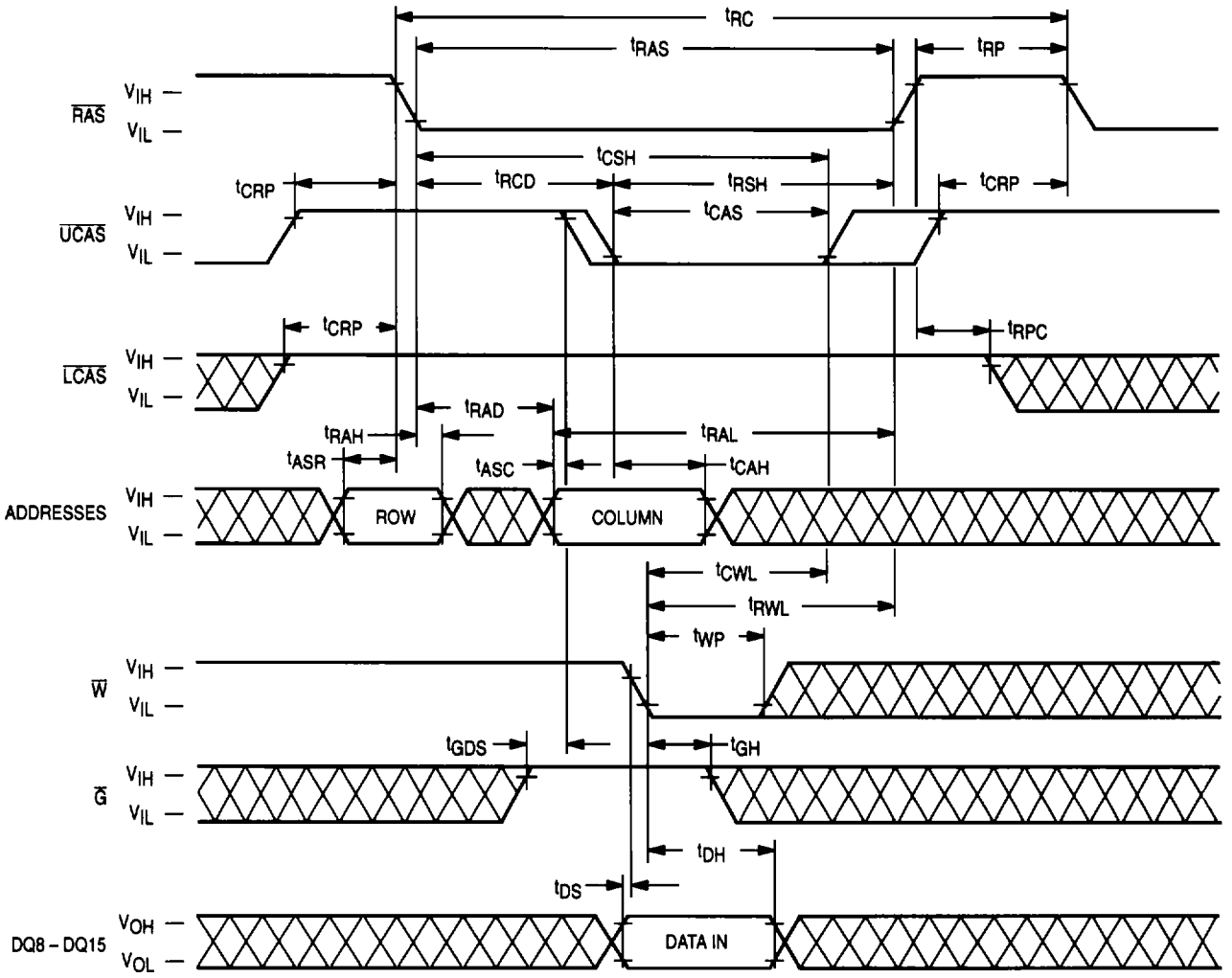
LOWER BYTE WRITE CYCLE (EARLY WRITE)



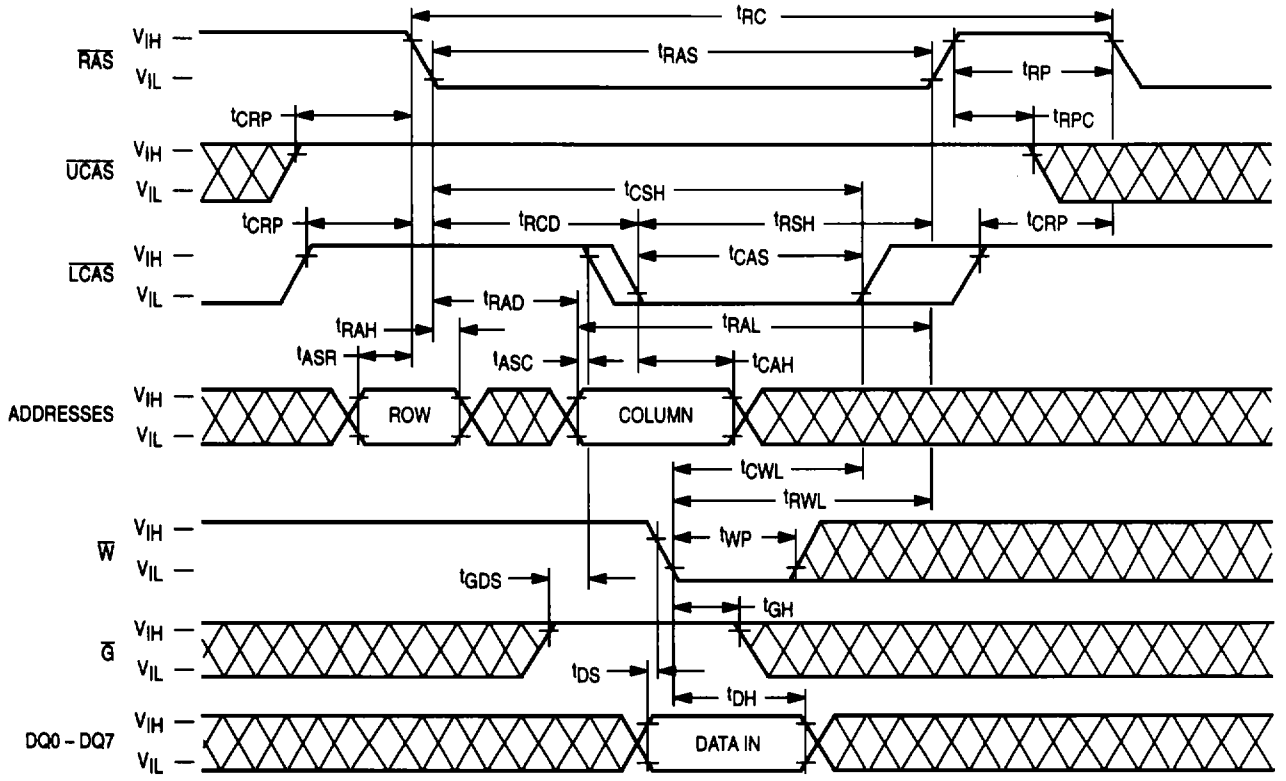
WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



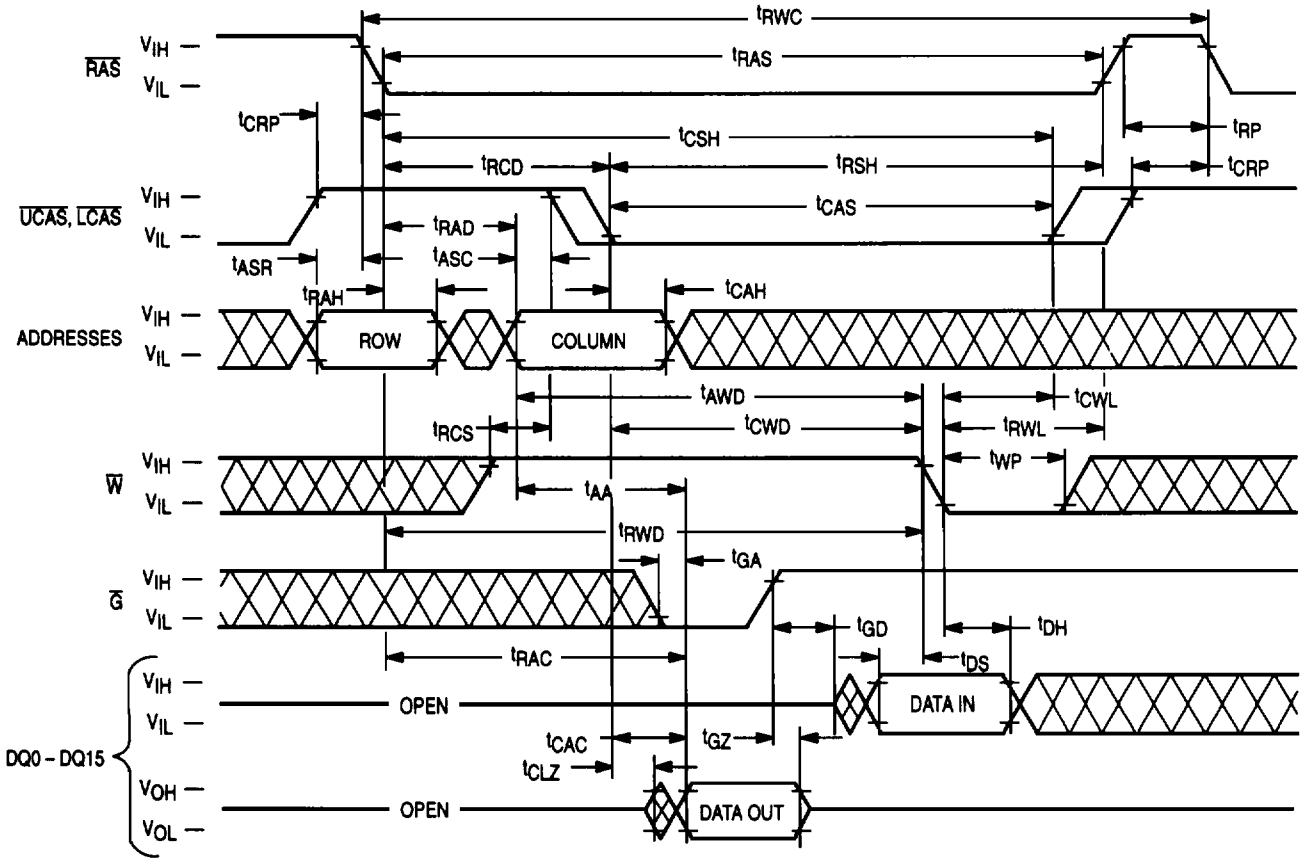
UPPER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



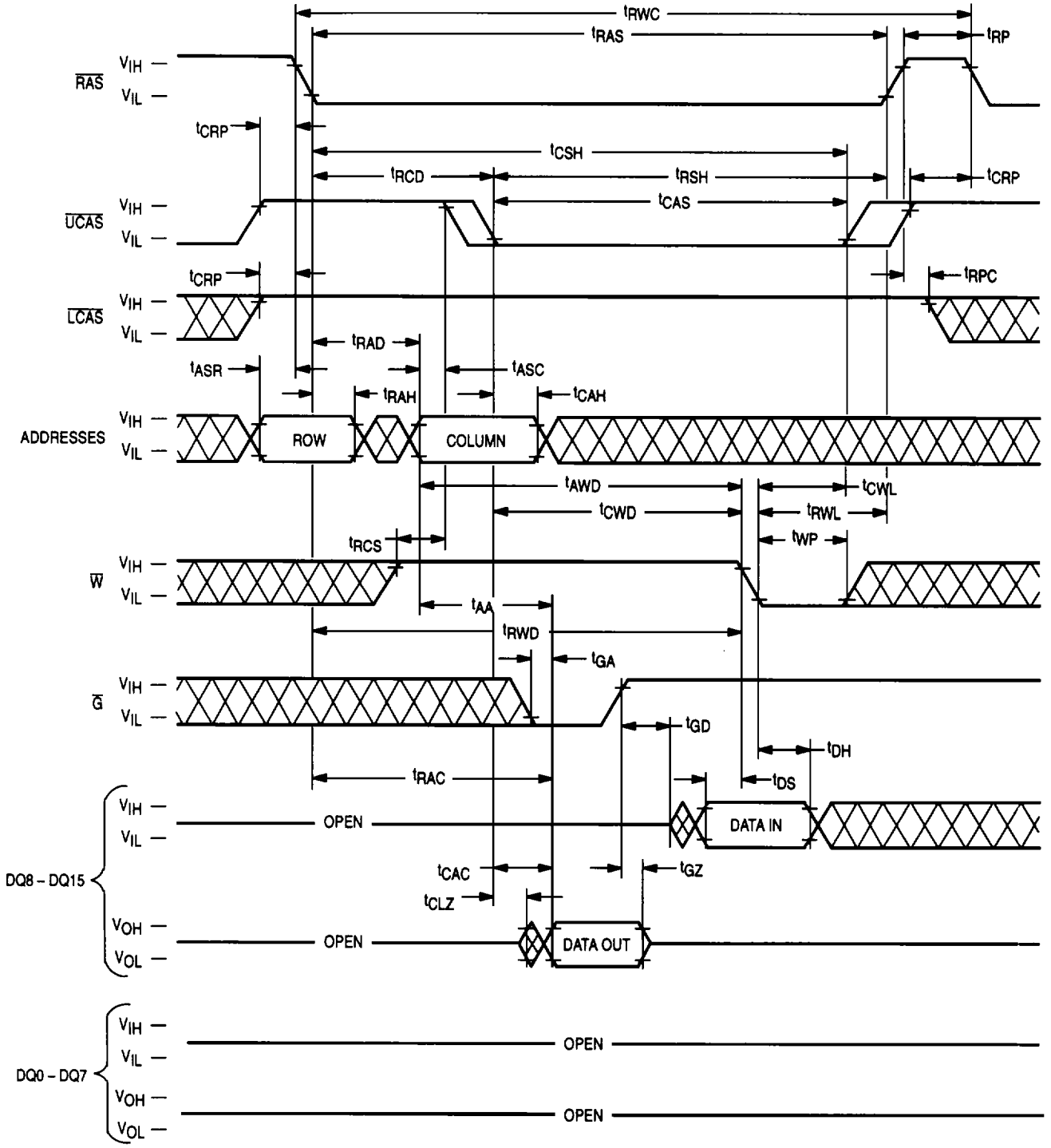
LOWER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



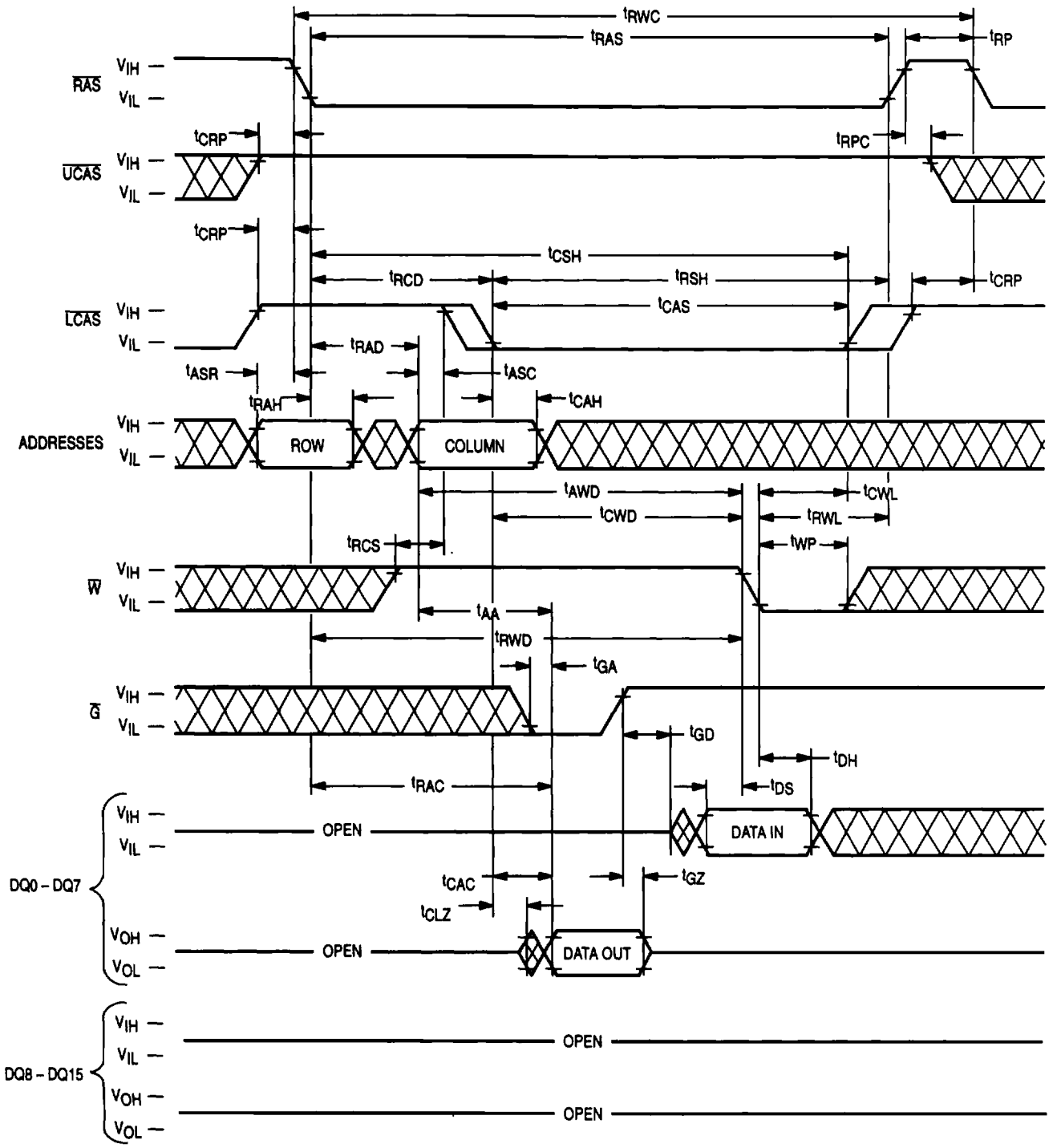
READ–WRITE CYCLE



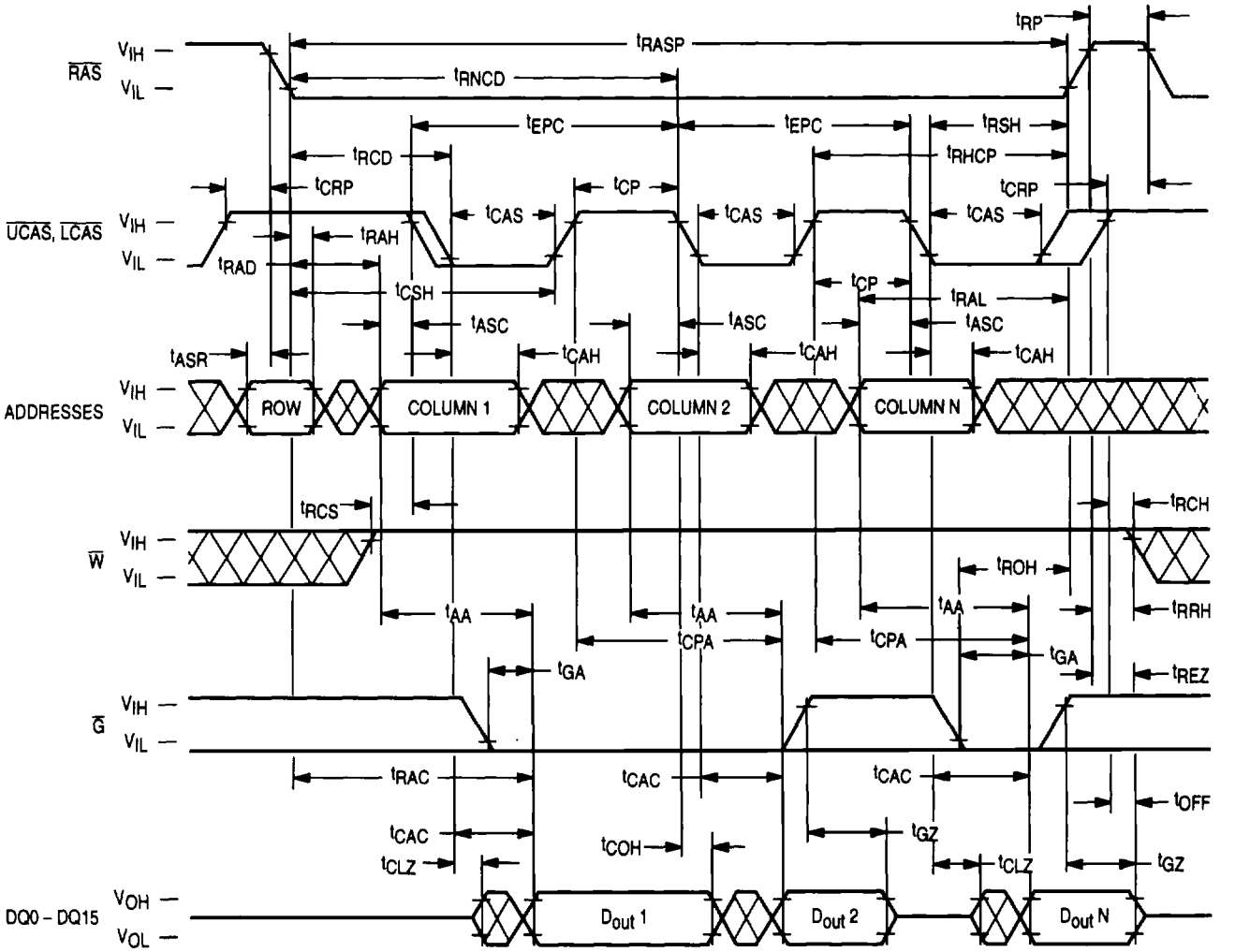
UPPER BYTE READ–WRITE CYCLE



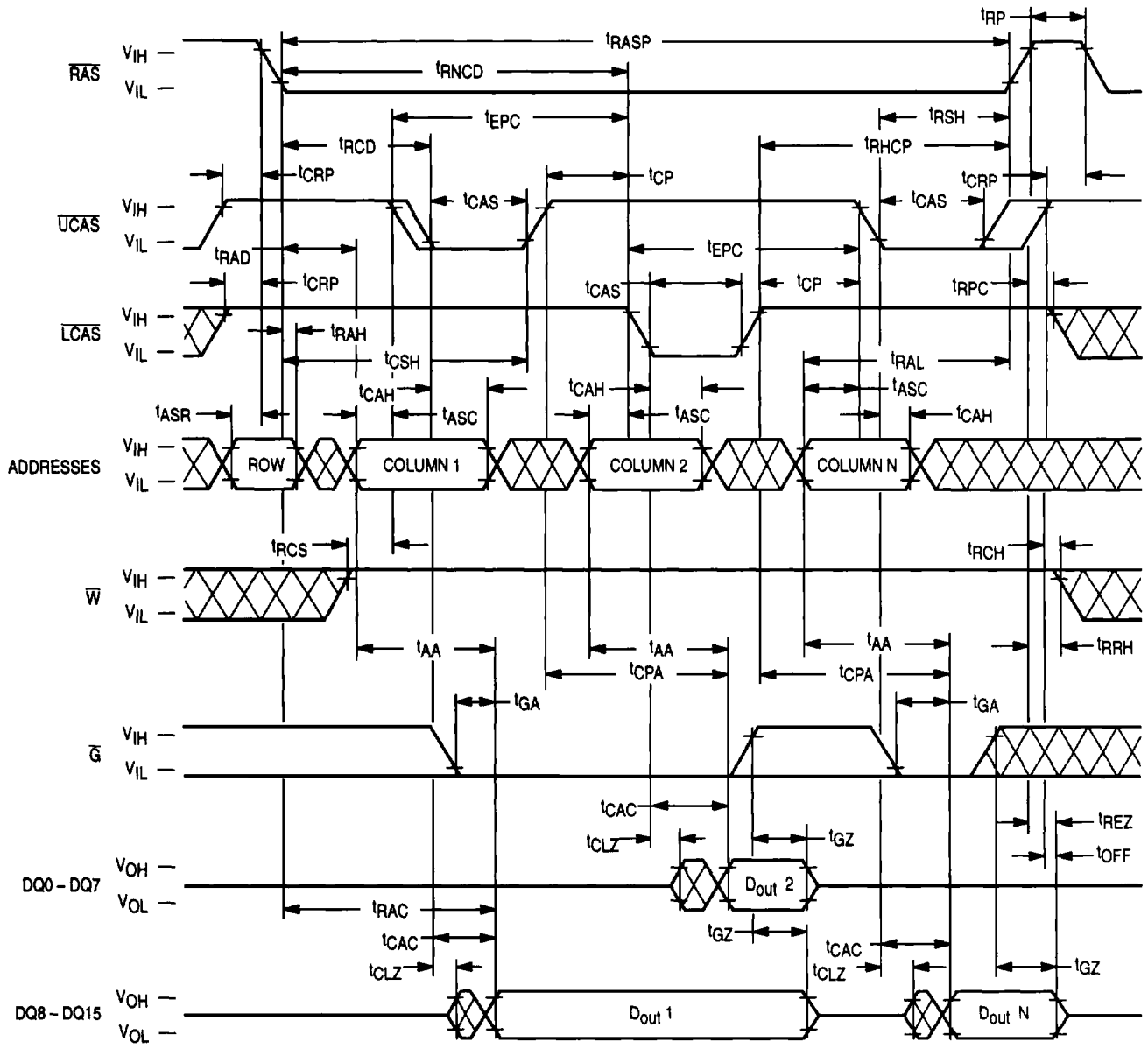
LOWER BYTE READ–WRITE CYCLE



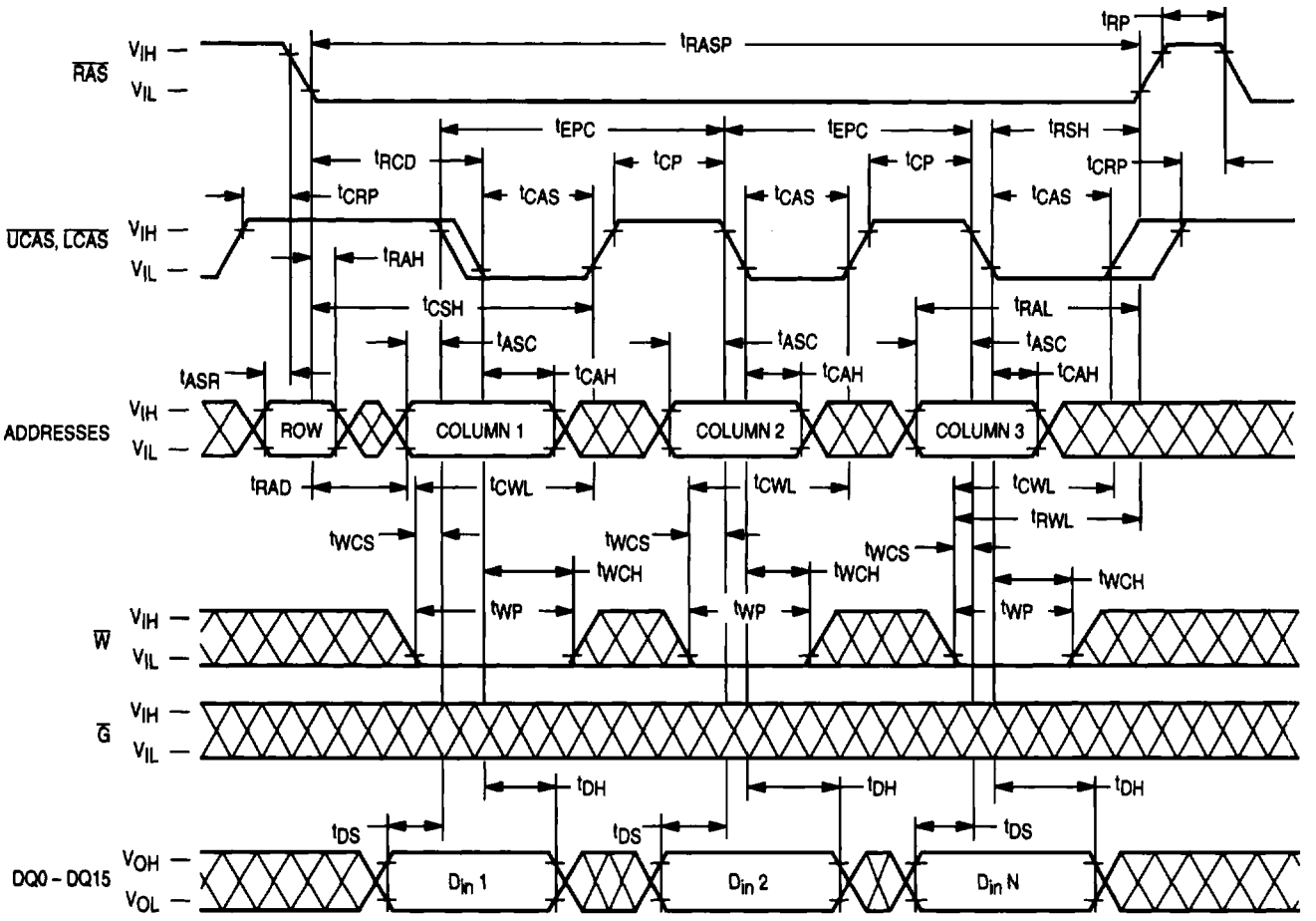
EXTENDED DATA OUT READ CYCLE



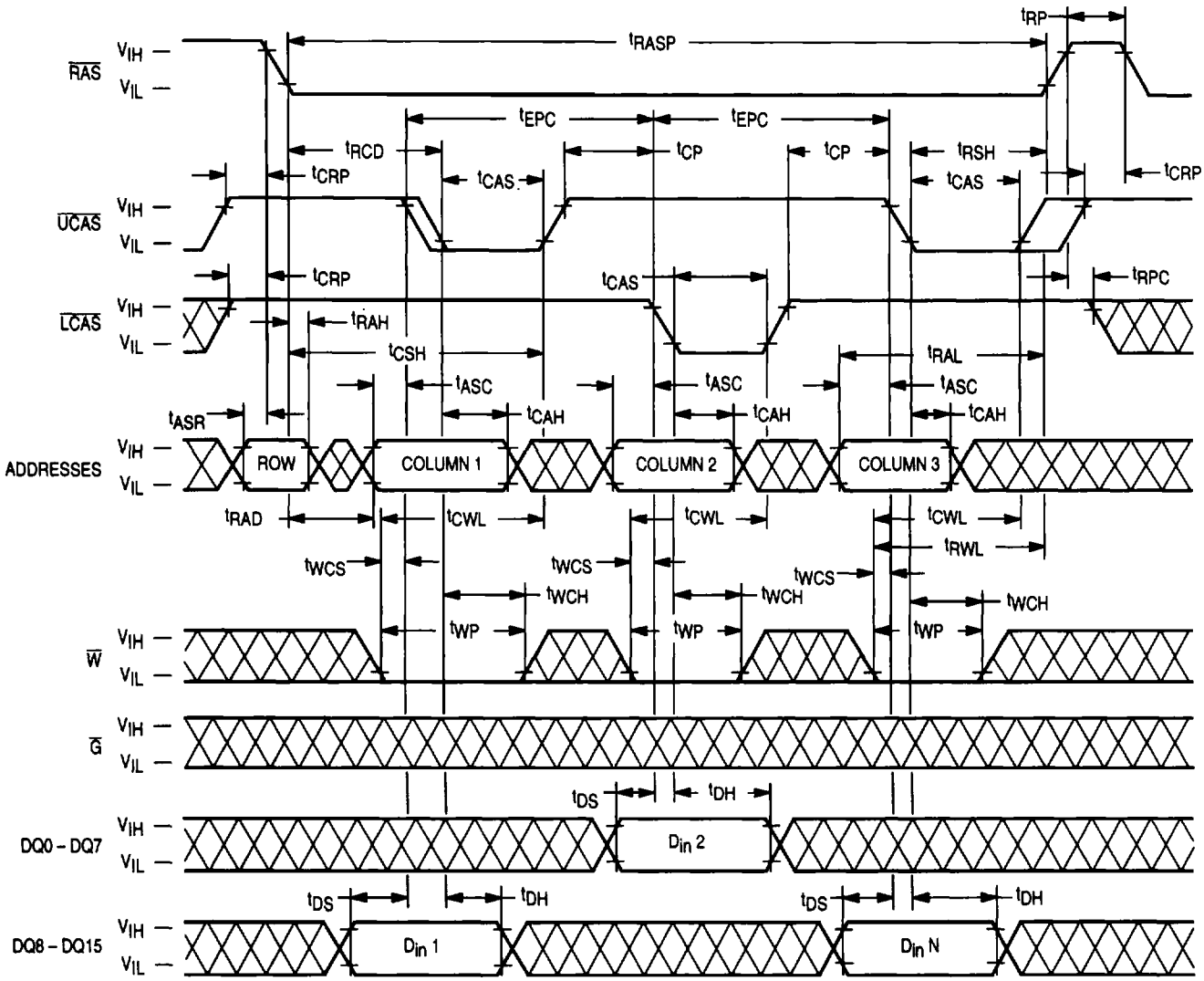
EXTENDED DATA OUT BYTE READ CYCLE



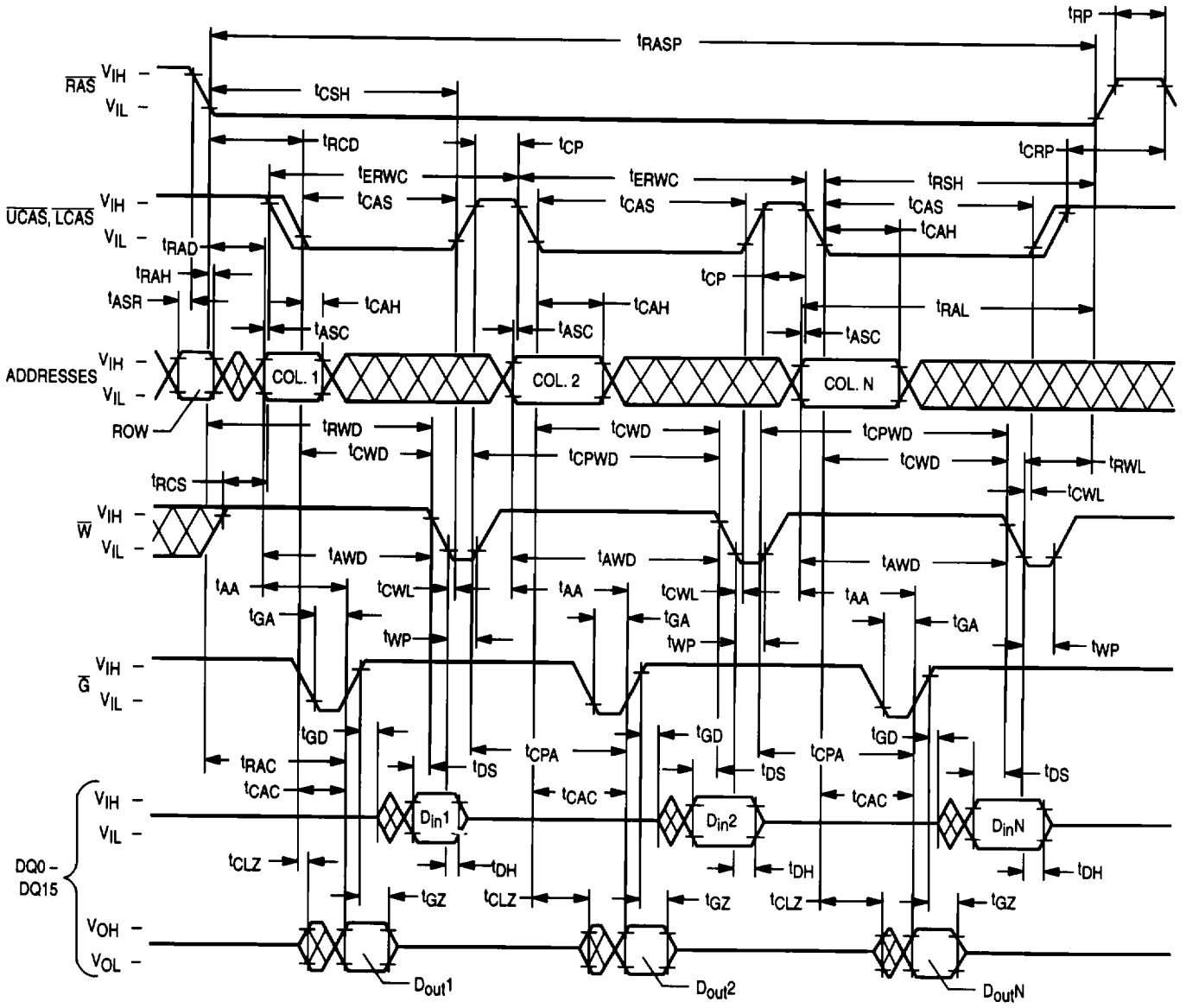
EXTENDED DATA OUT WRITE CYCLE (EARLY WRITE)



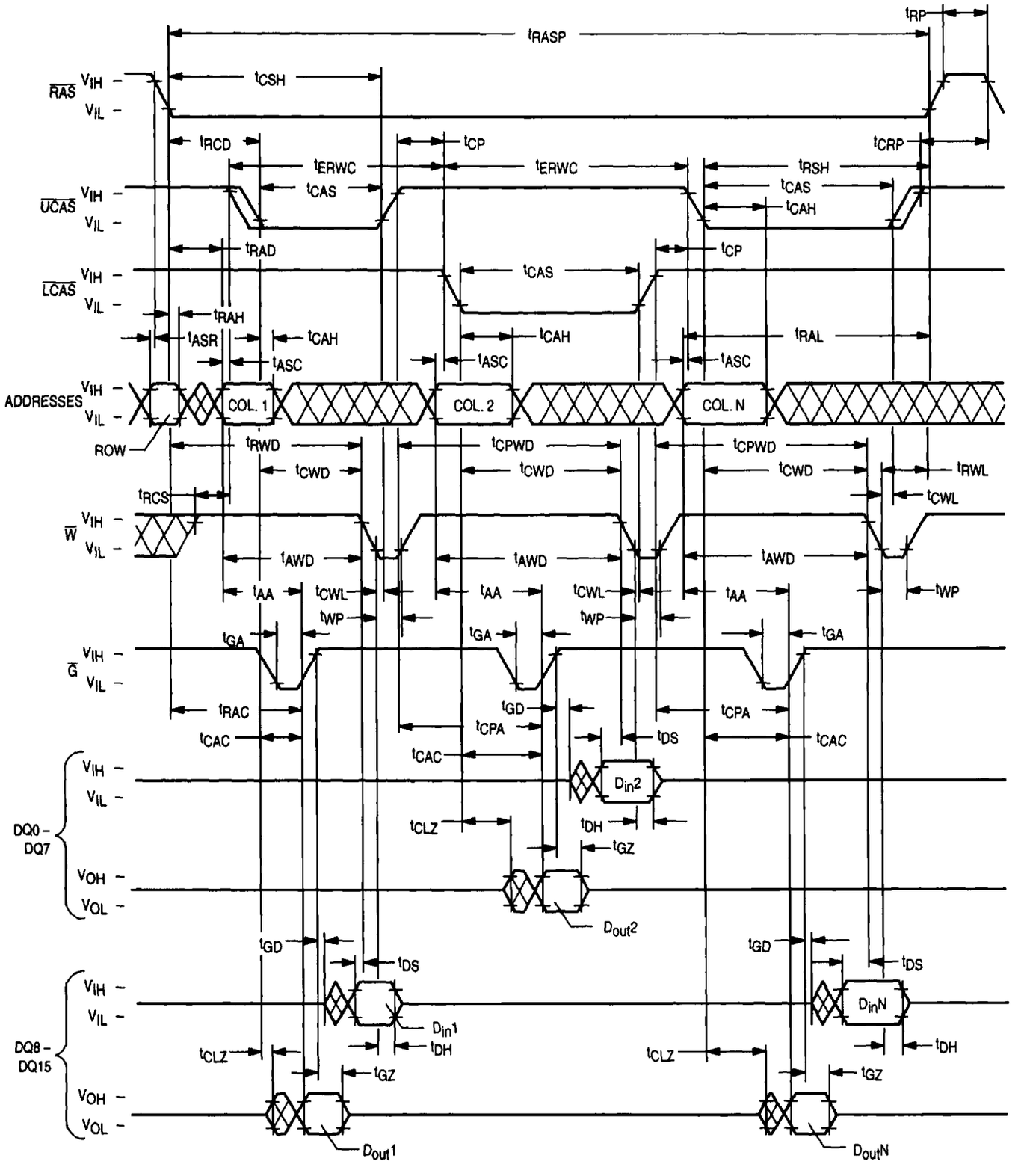
EXTENDED DATA OUT BYTE WRITE CYCLE (EARLY WRITE)



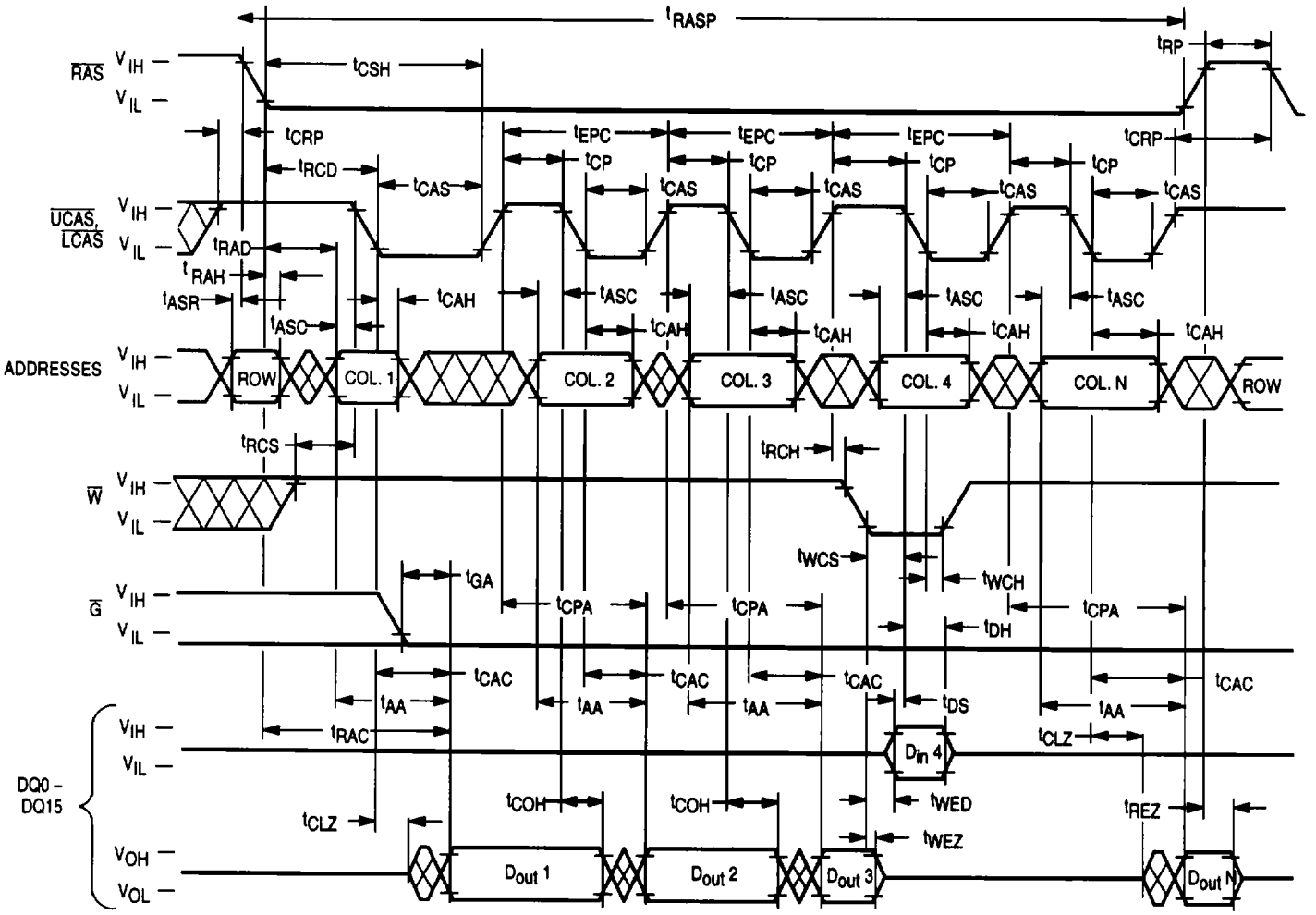
EXTENDED DATA OUT READ–WRITE CYCLE



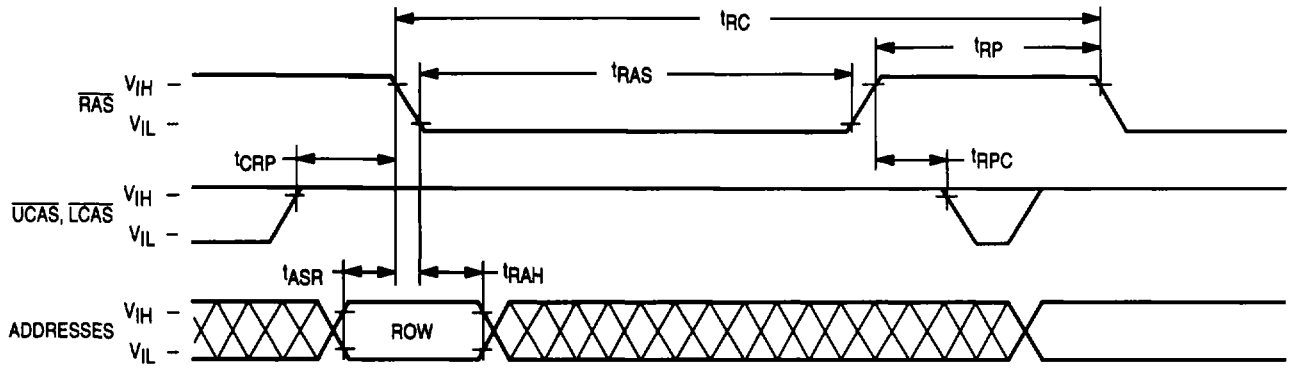
EXTENDED DATA OUT BYTE READ–WRITE CYCLE



EXTENDED DATA OUT READ WRITE MIXED CYCLE

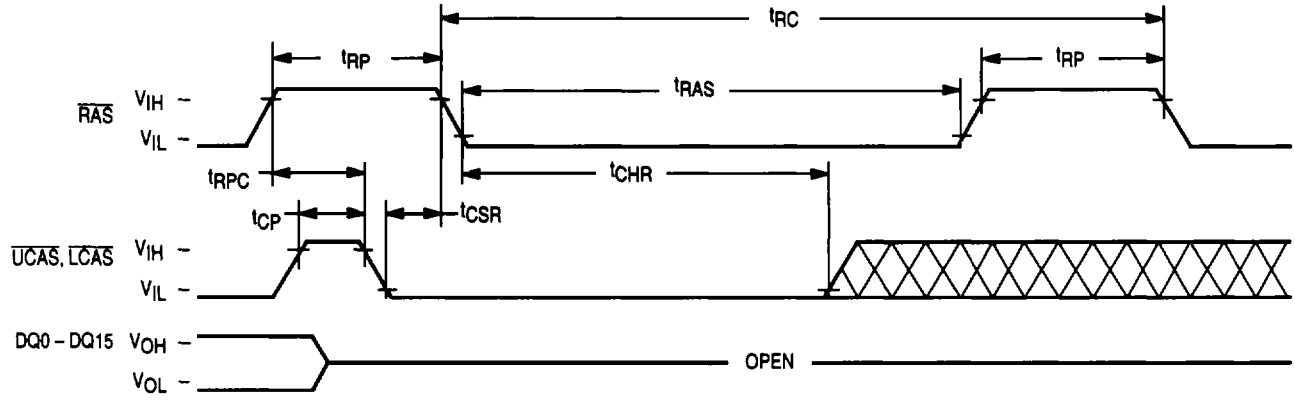


$\overline{RAS}$-ONLY REFRESH CYCLE



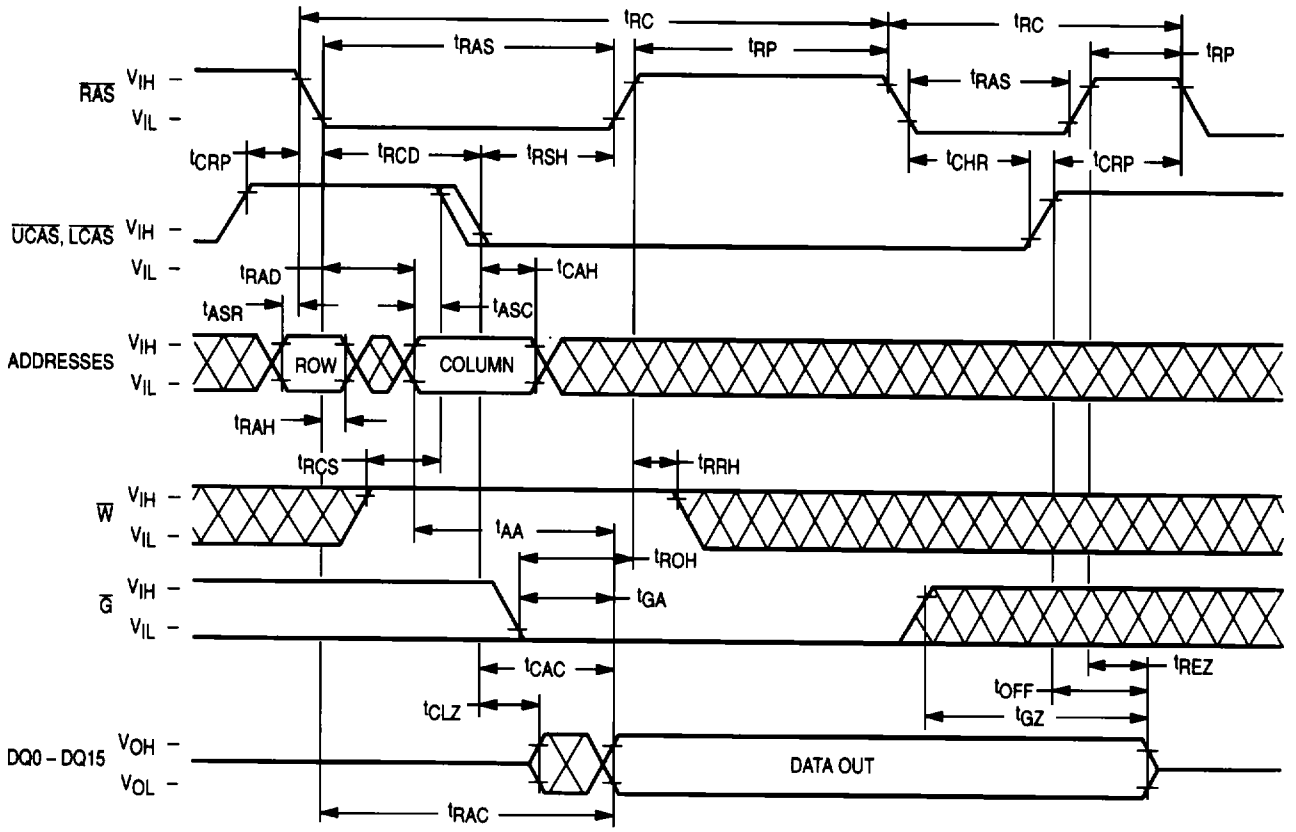
NOTE: $\overline{W}$, $\overline{G}$ = H or L
DQ0 – DQ15 = Open
Addresses: MCM516165BV — A0 to A11; MCM518165BV — A0 to A9.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

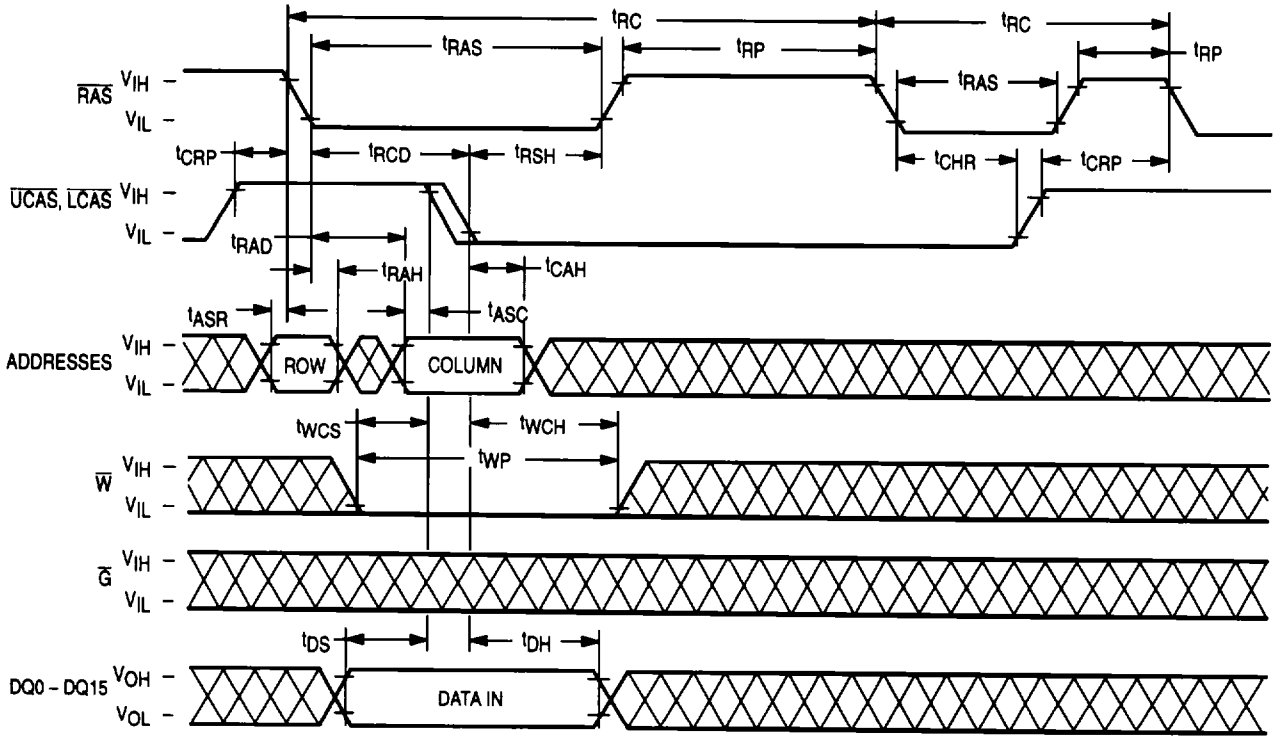


NOTE: $\overline{W}$, $\overline{G}$, Addresses= H or L
$\overline{CAS}$ before $\overline{RAS}$ refresh is performed when either $\overline{UCAS}$ or $\overline{LCAS}$ meets this timing.

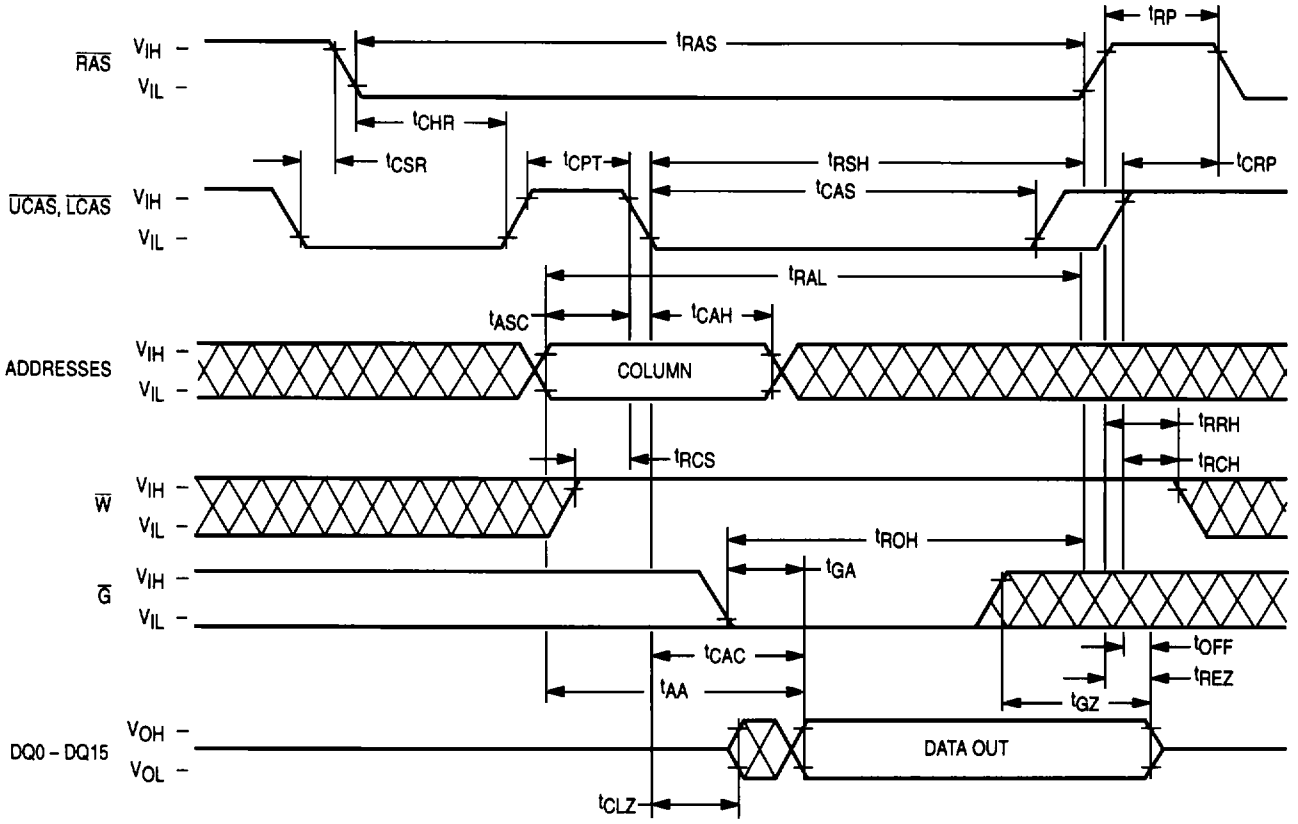
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

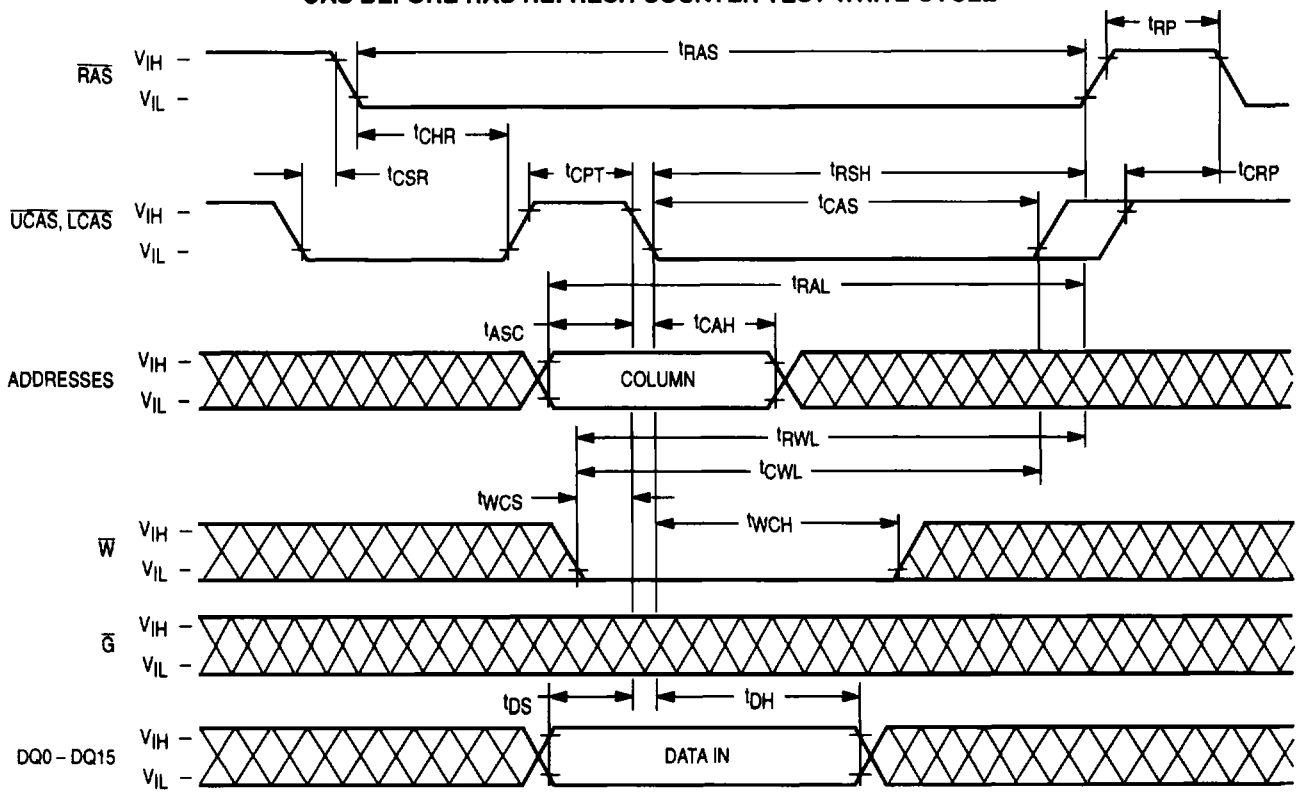


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



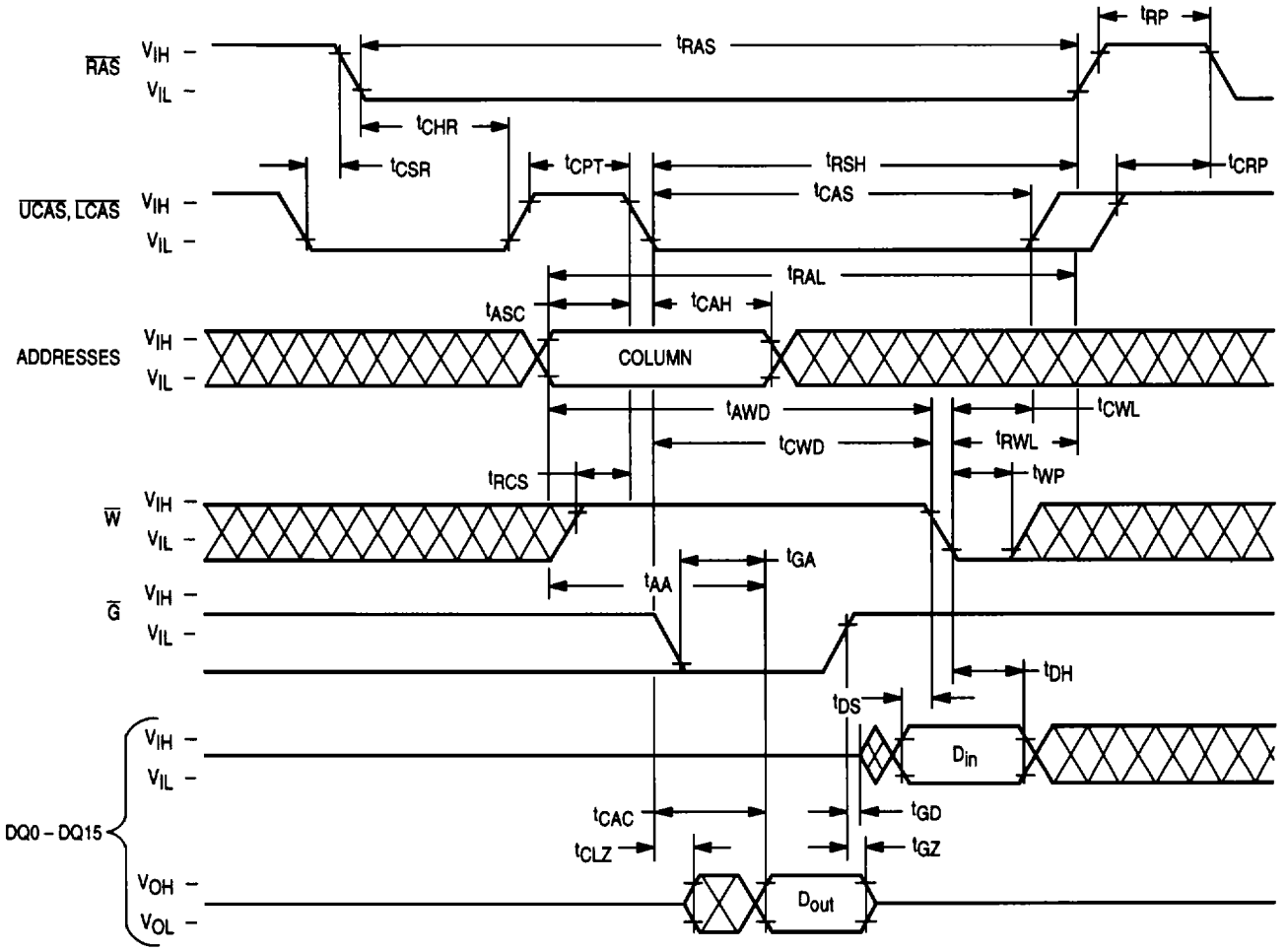
NOTE: Addresses: MCM516165BV — A0 to A7; MCM518165BV — A0 to A9

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



NOTE: Addresses: MCM516165BV — A0 to A7; MCM518165BV — A0 to A9

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ–WRITE CYCLE



NOTE: Addresses: MCM516165BV — A0 to A7; MCM518165BV — A0 to A9.

ORDERING INFORMATION
(Order by Full Part Number)

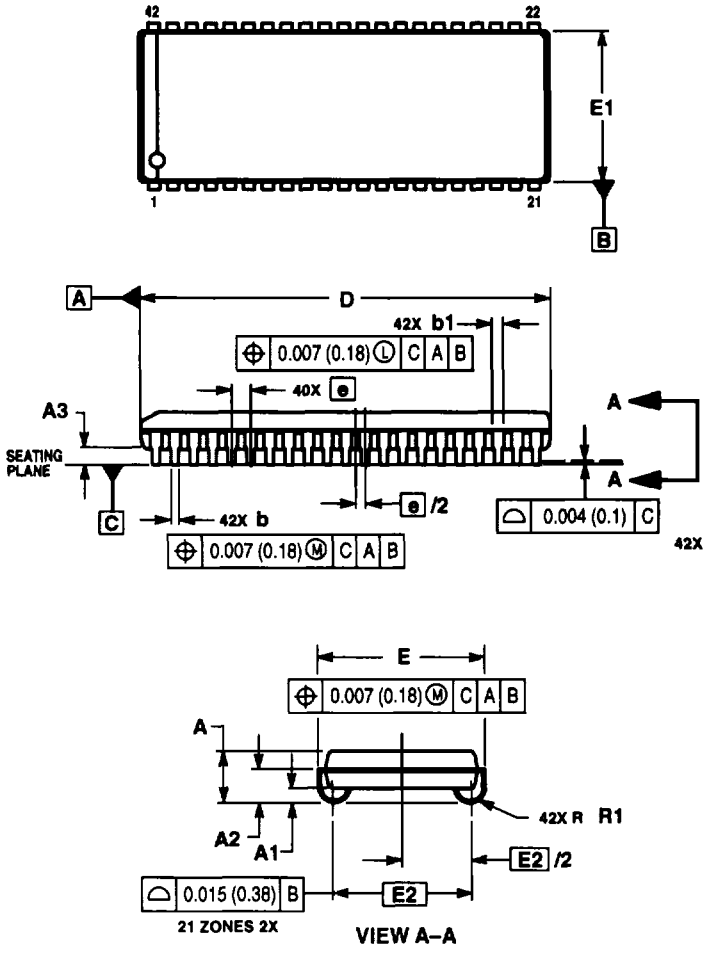
MCM 51x165BV X XX X

- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails for SOJ, Trays for TSOP II)
- Speed (60 = 60 ns, 70 = 70 ns)
- Package (J = 400 mil SOJ, T = 400 mil TSOP II)

Full Part Numbers –				
	MCM516165BVJ60	MCM516165BVJ60R	MCM516165BVT60	MCM516165BVT60R
	MCM516165BVJ70	MCM516165BVJ70R	MCM516165BVT70	MCM516165BVT70R
	MCM518165BVJ60	MCM518165BVJ60R	MCM518165BVT60	MCM518165BVT60R
	MCM518165BVJ70	MCM518165BVJ70R	MCM518165BVT70	MCM518165BVT70R

PACKAGE DIMENSIONS

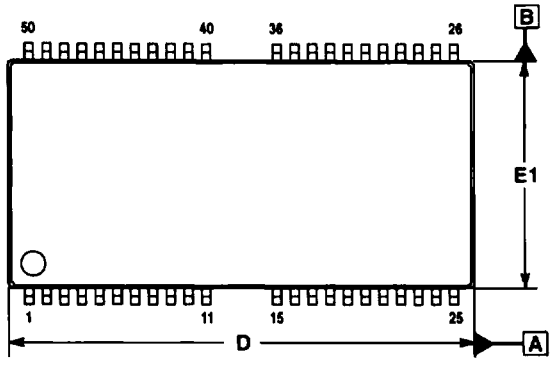
J PACKAGE
400 MIL SOJ
CASE 986A–01

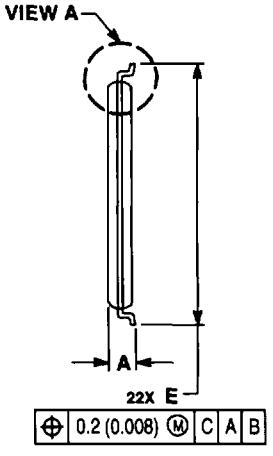


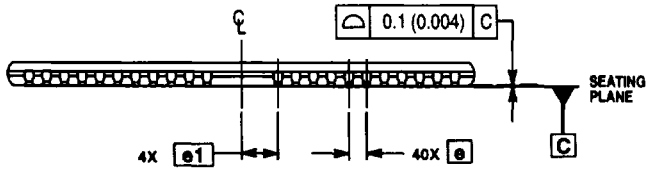
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006 (0.15) PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010 (0.25) PER SIDE.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 AND, HENCE, DATUMS A AND B, ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DIMENSIONS b1 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE SHOULDER WIDTH TO EXCEED b1 MAX BY MORE THAN 0.005 (0.13). THE DAMBAR INTRUSION(S) SHALL NOT REDUCE THE SHOULDER WIDTH TO LESS THAN 0.001 (0.03 BELOW b2 MIN.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.130	0.146	3.30	3.70
A1	0.031	0.047	0.80	1.20
A2	0.092	—	2.35	—
A3	0.031	—	0.80	—
b	0.016	0.020	0.41	0.50
b1	0.026	0.032	0.66	0.81
D	1.070	1.080	27.19	27.43
E	0.430	0.440	10.92	11.18
E1	0.395	0.405	10.03	10.29
E2	0.366 BSC		9.30 BSC	
e	0.050 BSC		1.27 BSC	
R1	0.025	0.035	0.63	0.89

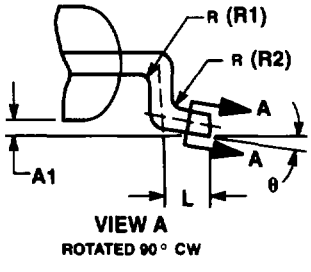
T PACKAGE
400 MIL TSOP II
CASE 985A–01



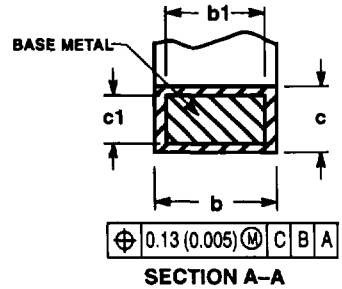




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MM.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION IS 0.15 (0.006) MAXIMUM PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.58 (0.023).
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 12, 13, 14, 37, 38 AND 39 ARE NOT USED.



VIEW A
ROTATED 90° CW



SECTION A–A
44 PLACES

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
b	0.25	0.45	0.010	0.018
b1	0.25	0.40	0.010	0.016
c	0.12	0.25	0.005	0.010
c1	0.10	0.20	0.004	0.008
D	20.85	21.06	0.821	0.829
e	0.80 BSC		0.0315 BSC	
e1	1.60 BSC		0.063 BSC	
E	11.56	11.96	0.455	0.471
E1	10.06	10.26	0.396	0.404
L	0.40	0.60	0.016	0.024
R1	0.10 REF		0.004 REF	
R2	0.10 REF		0.004 REF	
θ	0°	10°	0°	10°

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