UMC

UM6167 Series

16K × 1 High Speed CMOS SRAM

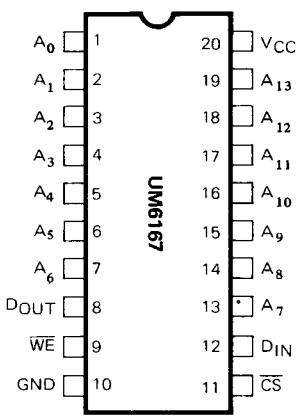
Features

- Single +5 volt power supply
- Access times: 55/70 ns (max.)
- Current:
  Standard version: Operating: 60 mA (max.)
  Standby: 2 mA (max.)
  Low power version: Operating: 50 mA (max.)
  Standby: 50 μA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Available in 20 pin DIP package
- Available in standard (UM6167) and low power (UM6167L) versions. (See ordering information)

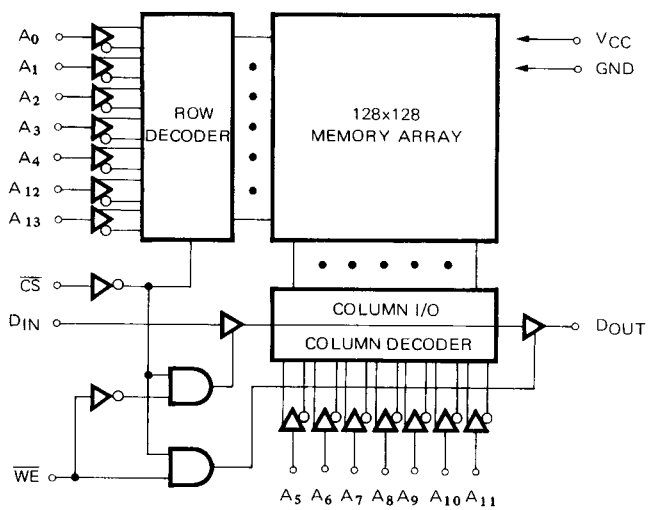
General Description

The UM6167 is a 16,384-bit static random access memory organized as 16,384 words by 1 bit and operates from a single 5 volt supply. It is built with UMC's high performance, twin tub, CMOS process. The inputs and three-state outputs are TTL compatible. The UM6167 is packaged in a standard 20-pin DIP.

Pin Configuration



Block Diagram



Pin Description

Designation	Description
$A_0 - A_{13}$	Address Input
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC} + 0.5V	V
V_{IL}	Input Low Voltage	−0.3	0	+0.8	V

Absolute Maximum Ratings *

V_{CC} to GND . . . . . −0.5V to +7.0V
IN, IN/OUT volt to GND . . . . . −0.5V to V_{CC} +0.5V
Operating Temperature, T_{opr} . . . . . 0°C to +70°C
Temperature Under Bias, T_{bias} . . . . . −10°C to +85°C
Storage Temperature, T_{stg} . . . . . −55°C to +125°C
Power Dissipation, P_T 1.0W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM6167/-1		UM6167L/-1L		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	–	2	–	2	μA	V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current	–	2	–	2	μA	$\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}
I_{CC}	Active Power Supply Current	–	60	–	50	mA	$\overline{CS}$ = V_{IL}, I_O = 0 mA
I_{CC1}	Dynamic Operating Current	–	60	–	50	mA	Min. Cycle, Duty = 100% $\overline{CS}$ = V_{IL}, I_O = 0mA
I_{SB}	Standby Power Supply Current	–	20	–	20	mA	$\overline{CS}$ = V_{IH}
I_{SB1}		–	2	–	0.05	mA	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	–	0.4	–	0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4	–	2.4	–	V	I_{OH} = −4 mA

Truth Table

Mode	$\overline{CS}$	$\overline{WE}$	Output Operation	V_{CC} Current
Standby	H	X	High Z	I_{SB}, I_{SB1}
Read	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	L	D_{IN}	I_{CC}, I_{CC1}

Note: X : H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
C_{OUT}*	Output Capacitance		8	pF	V_{OUT} = 0V

* This parameter is sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

READ CYCLE

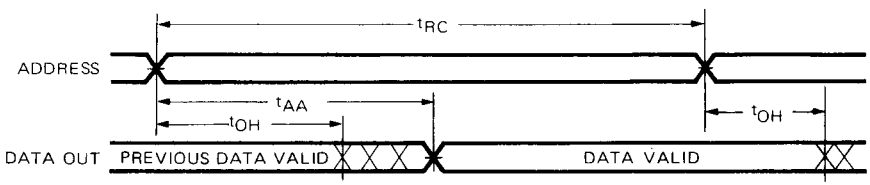
Symbol	Parameter	UM6167/L		UM6167-1/-1L		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	70	–	55	–	ns
t_{AA}	Address Access Time	–	70	–	55	ns
t_{ACS}	Chip Select Access Time	–	70	–	55	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	30	0	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	35	–	35	ns

WRITE CYCLE

Symbol	Parameter	UM6167/L		UM6167-1/-1L		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	70	–	55	–	ns
t_{CW}	Chip Selection to End of Write	60	–	45	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	ns
t_{AW}	Address Valid to End of Write	60	–	45	–	ns
t_{WP}	Write Pulse Width	45	–	35	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z	0	30	0	30	ns
t_{DW}	Data to Write Time Overlap	30	–	25	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	ns
t_{OW}	Output Active from End of Write	0	–	0	–	ns

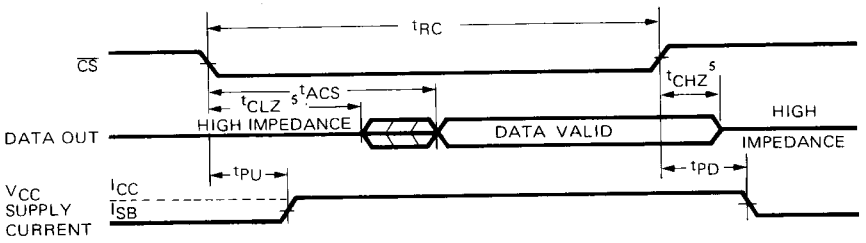
Timing Waveforms

READ CYCLE 1 (1, 2)

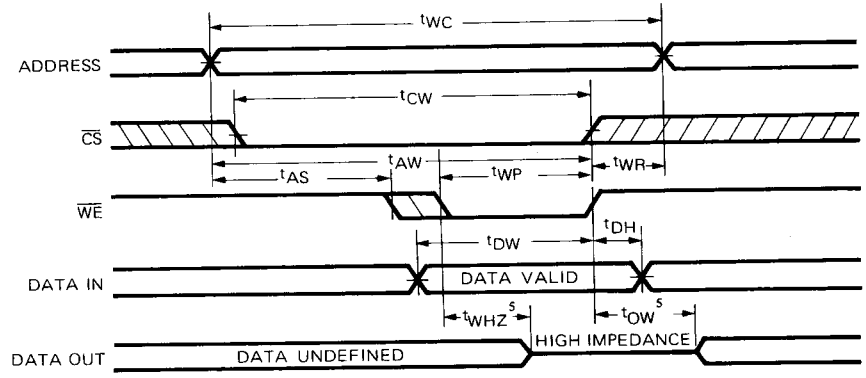


Timing Waveforms (Continued)

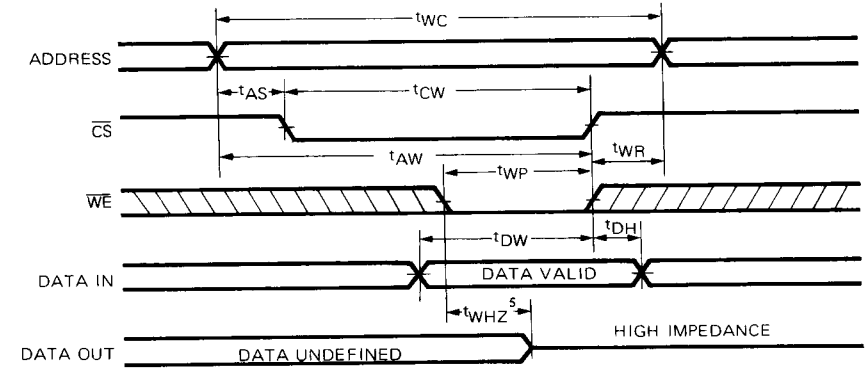
READ CYCLE 2 (1, 3)



WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (4)



WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED) (4)



Notes:

1. $\overline{WE}$ is high for READ cycle.
2. Device is continously selected $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high the output remains in a high impedance state.
5. Transition is measured ±500 mV from steady state. This parameter is sampled and not 100% tested.

A.C. Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

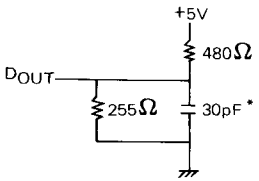


Figure 1. Output Load

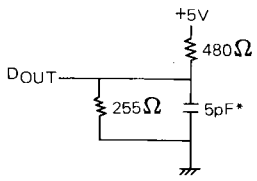


Figure 2. Output Load (for t_{CHZ}, t_{CLZ}, t_{WHZ}, and t_{OW})

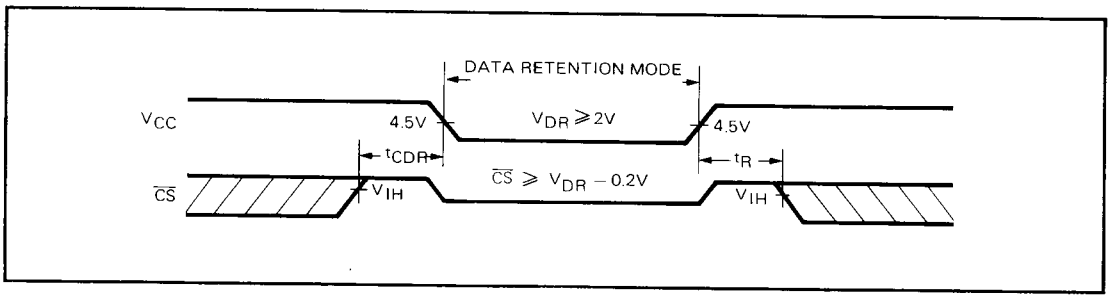
* Including scope and jig.

Low V_{CC} Data Retention Characteristics (For L Versions Only) (T_A = 0°C to 70°C)

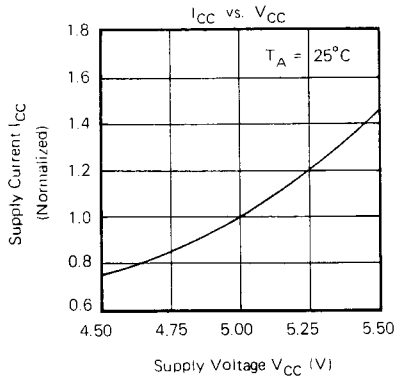
Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
V_{DR}	V_{CC} for Data Retention	2.0	–	5.5	V	$\overline{CS} \geq V_{CC} - 0.2V$
I_{CCDR}	Data Retention Current	– –	0.5[2] 1.0[3]	20[2] 30[3]	μA	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$
t_{CDR}	Chip Deselect to Data Retention Time	0	–	–	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}[4]	–	–	ns	See Retention Waveform

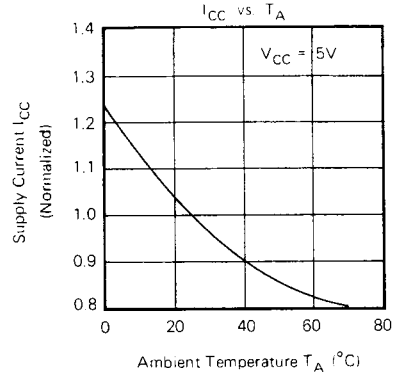
Notes: 1. T_A = 25°C, 2. at V_{CC} = 2V, 3. V_{CC} = 3V, 4. t_{RC} = Read Cycle Time

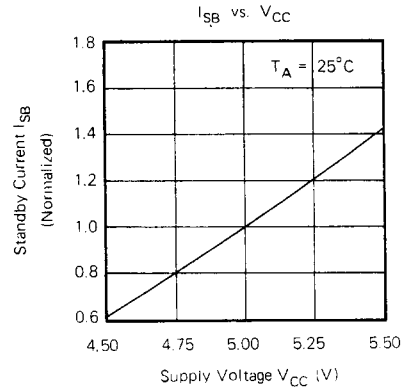
Timing Waveform Low V_{CC} Data Retention

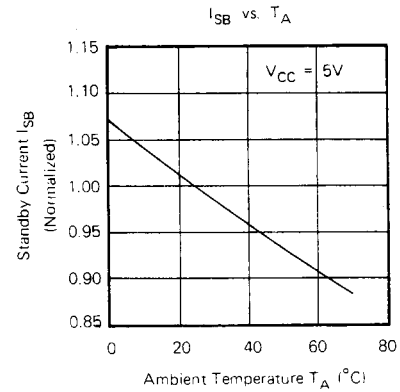


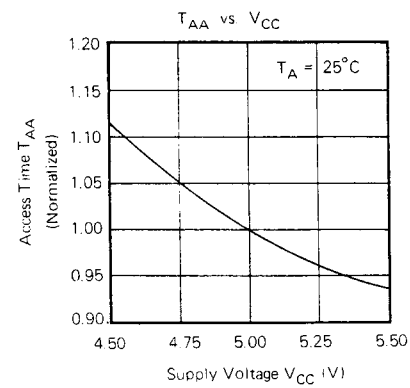
Characteristic Curves

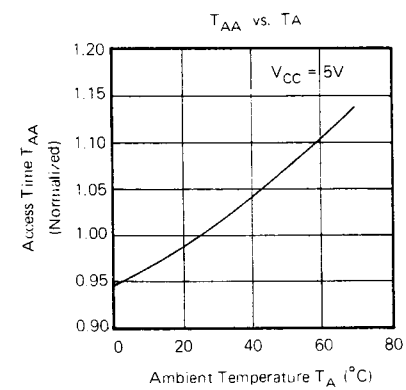












Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM6167	70	60	2	20L DIP
UM6167-1	55	60	2	20L DIP
UM6167L	70	50	0.05	20L DIP
UM6167-1L	55	50	0.05	20L DIP