



8-Channel Constant Current LED Driver

FEATURES

- 8 Constant current-sink channels
- Serial interface up to 25MHz clock frequency
- 3V to 5.5V logic supply
- LED current range from 2mA to 100mA
- LED current set by external RSET resistor
- 300mV LED dropout at 30mA
- Thermal shutdown protection
- Available in RoHS-compliant 16-lead SOIC (150 and 300mil wide), and TSSOP packages

APPLICATIONS

- Billboard Display
- Marquee Display
- Instrument Display
- General Purpose Display

For Ordering Information details, see page 13.

DESCRIPTION

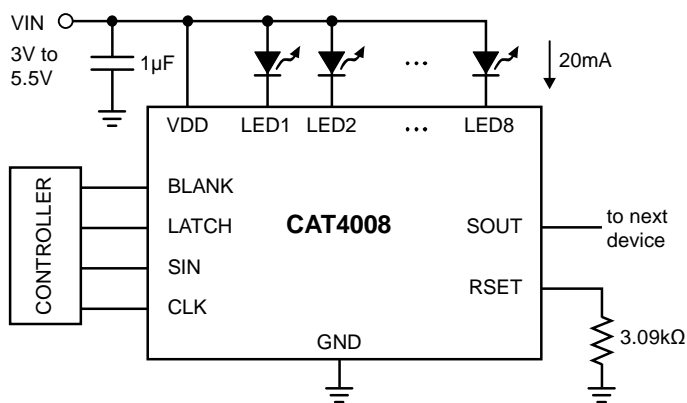
The CAT4008 is an 8 channel constant current driver for LED billboard and other general display applications. LED channel currents are programmed together via an external RSET resistor. Low output voltage operation on the LED channels as low as 0.4V (for 2 to 100mA LED current) allows for more power efficient designs.

A high-speed 4-wire serial interface of up to 25MHz clock frequency controls each individual channel using a shift register and latch configuration. A serial output data pin (SOUT) allows multiple devices to be cascaded and programmed via one serial interface. The device also includes a blanking control pin (BLANK) that can be used to disable all channels independently of the interface.

Thermal shutdown protection is incorporated in the device to disable the LED outputs if the die temperature exceeds a set limit.

The device is available in the 16-lead SOIC (narrow and wide), and TSSOP packages.

TYPICAL APPLICATION CIRCUIT

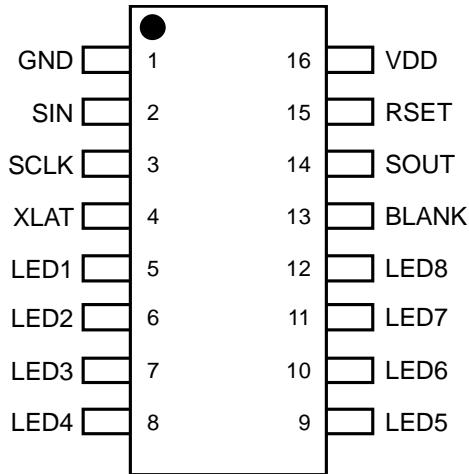


ORDERING INFORMATION

Part Number	Package	Quantity per Reel	Package Marking
CAT4008W-T2	SOIC16 (N) ⁽¹⁾	2,000	CAT4008W
CAT4008V-T1	SOIC16 (W) ⁽¹⁾⁽²⁾	1,000	CAT4008V
CAT4008Y-T2	TSSOP16 ⁽¹⁾⁽²⁾	2,000	CAT4008Y
CAT4008Y-GT2	TSSOP16 ⁽³⁾	2,000	CAT4008Y

PIN CONFIGURATION

16-Lead SOIC (W, V), TSSOP (Y)



Notes:

- (1) Matte-Tin Plated Finish (RoHS-compliant).
- (2) Contact factory for package availability.
- (3) NiPdAu Plated Finish (RoHS-compliant).

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
V _{DD} Supply Voltage	6	V
Logic input/output voltage (SIN, SOUT, CLK, BLANK, LATCH)	-0.3V to V _{DD} +0.3V	V
LEDn voltage	6	V
DC output current on LED1 to LED8	150	mA
Storage Temperature Range	-55 to +160	°C
Junction Temperature Range	-40 to +150	°C
Lead Soldering Temperature (10sec.)	300	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Range	Units
V _{DD}	3.0 to 5.5	V
Voltage applied to LED1 to LED8	0.4 to 5.5	V
LED current RSET control range	up to 100	mA
Ambient Temperature Range	-40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS

DC CHARACTERISTICS

V_{DD} = 5.0V, T_{AMB} = 25 °C, over recommended operating conditions unless specified otherwise.

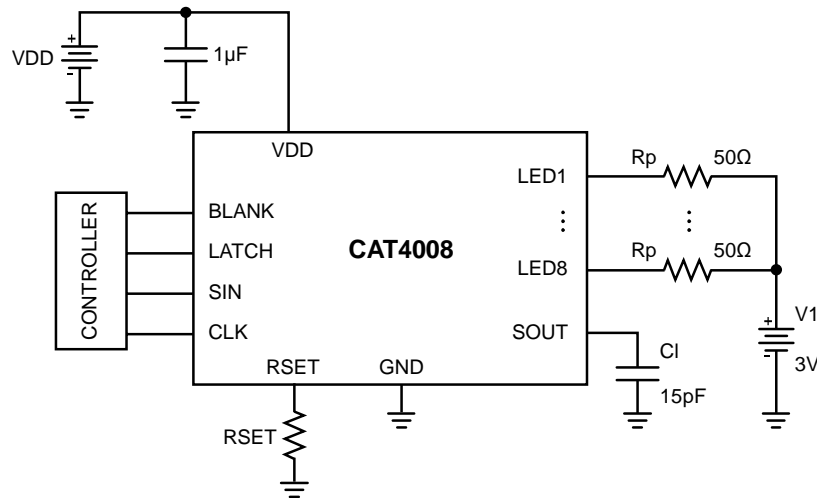
Symbol	Name	Conditions	Min	Typ	Max	Units
I _{LED-ACC}	LED Current (any channel)	V _{LED} = 1V, R _{SET} = 3.08kΩ	18	20	22	mA
		V _{LED} = 1V, R _{SET} = 1.54kΩ	36	40	44	
		V _{LED} = 1V, R _{SET} = 769Ω		80		
I _{LED-MAT}	LED Current Matching (I _{LED} - I _{LEDAVR}) / I _{LEDAVR}	V _{LED} = 1V, R _{SET} = 3.08kΩ		±1.5		%
		V _{LED} = 1V, R _{SET} = 1.54kΩ	-6.0	±1.5	+6.0	
		V _{LED} = 1V, R _{SET} = 769Ω		±2.0		
ΔI _{VDD}	LED current regulation vs. V _{DD}	V _{DD} within 4.5V and 5.5V LED current 30mA		±0.1		% / V
ΔI _{VLED}	LED current regulation vs. V _{LED}	V _{LED} within 1V and 3V LED current 30mA		±0.05		% / V
I _{DDOFF}	Supply Current (all outputs off)	R _{SET} = 3.08kΩ		2	8	mA
		R _{SET} = 769Ω		5.5		mA
I _{DDON}	Supply Current (all outputs on)	R _{SET} = 3.08kΩ		2.5	9	mA
		R _{SET} = 769Ω		6.2		mA
I _{LKG}	LEDn output Leakage	V _{LED} = 5V, outputs off	-1		1	μA
R _{LATCH}	LATCH Pull-down Resistance		100	180	300	kΩ
R _{BLANK}	BLANK Pull-up Resistance		100	180	300	kΩ
V _{IH}	Logic high input voltage		0.7xV _{DD}			V
V _{IL}	Logic low input voltage				0.3xV _{DD}	V
V _{HYS}	Logic input hysteresis voltage			0.1xV _{DD}		V
I _{IL}	Logic Input leakage current (CLK, SIN)	V _I = V _{DD} or GND	-5	0	5	μA
V _{OH} V _{OL}	SOUT logic high output voltage SOUT logic low output voltage	I _{OH} = -1mA I _{OL} = 1mA	V _{CC} -0.3V		0.3	V
V _{RSET}	RSET Regulated Voltage	BLANK high, outputs off	1.17	1.20	1.23	V
T _{SD}	Thermal Shutdown			160		°C
T _{HYST}	Thermal Hysteresis			20		°C

TIMING CHARACTERISTICS

For $3.0V \leq V_{DD} \leq 5.5V$, $T_{AMB} = 25\text{ }^{\circ}\text{C}$, unless specified otherwise.

Symbol	Name	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
CLK						
f_{clk}	CLK Clock Frequency				25	MHz
t_{cwh}	CLK Pulse Width High		20			ns
t_{cwl}	CLK Pulse Width Low		20			ns
SIN						
t_{ssu}	Setup time SIN to CLK		4			ns
t_{sh}	Hold time SIN to CLK		4			ns
LATCH						
t_{lwh}	LATCH Pulse width		20			ns
T_{lh}	Hold time LATCH to CLK		4			ns
T_{lsu}	Setup time LATCH to CLK	Channel Stagger Delay	400			ns
LEDn						
t_{ld}	LED1 Propagation delay	LATCH to LED1 off/on		40	300	ns
t_{ls}	LED Propagation delay stagger	LED(n) to LED(n+1)		17	40	ns
t_{lst}	LED Propagation delay stagger total	LED1 to LED8		120		ns
t_{bd}	BLANK Propagation delay	BLANK to LED(n) off/on		60	300	ns
t_{lr}	LED rise time (10% to 90%)	Pull-up resistor = 50Ω to 3.0V		40	200	ns
t_{lf}	LED fall time (90% to 10%)	Pull-up resistor = 50Ω to 3.0V		30	250	ns
SOUT						
t_{or}	SOUT rise time (10% to 90%)	$C_L = 15\text{pF}$		5		ns
t_{of}	SOUT fall time (90% to 10%)	$C_L = 15\text{pF}$		5		ns
t_{od}	Propagation delay time SOUT	CLK to SOUT	8	15	25	ns

TEST CIRCUIT FOR AC CHARACTERISTICS



Notes:

- (1) All min and max values are guaranteed by design.
- (2) $V_{DD} = 5V$, LED current 30mA.

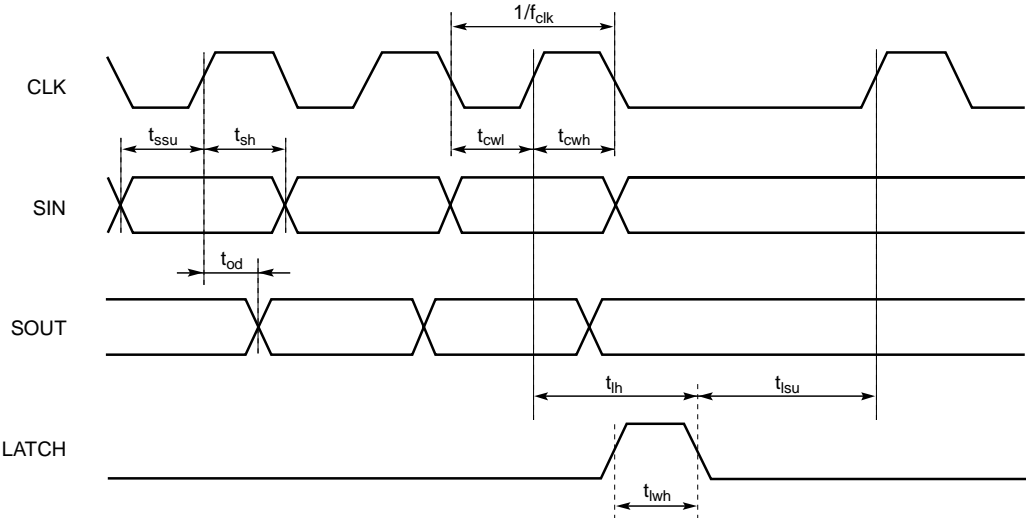


Figure 1. Serial Input Timing Diagram

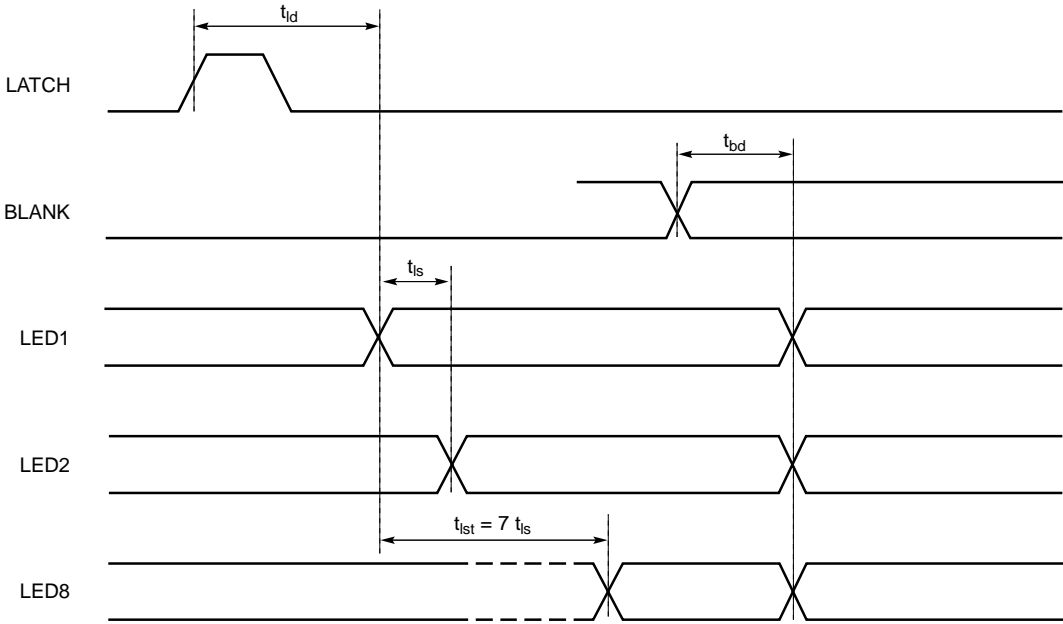
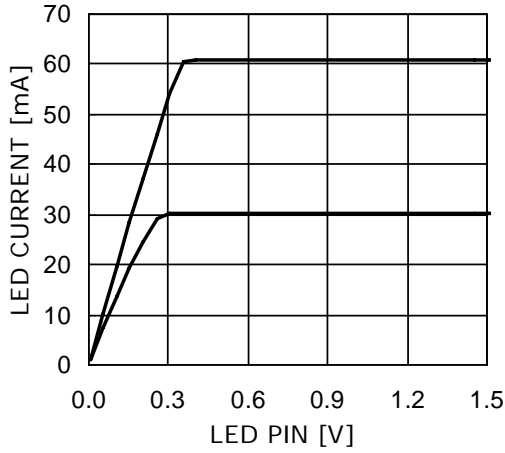


Figure 2. LED Output Timing Diagram

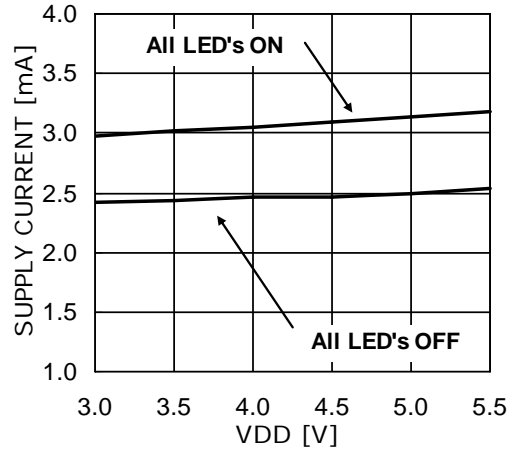
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 5.0V$, LED current 30mA, all LEDs On, $T_{AMB} = 25^{\circ}C$ unless otherwise specified.

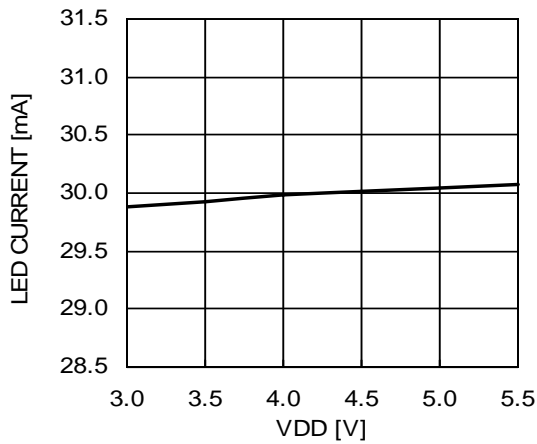
LED Current vs. LED Pin Voltage



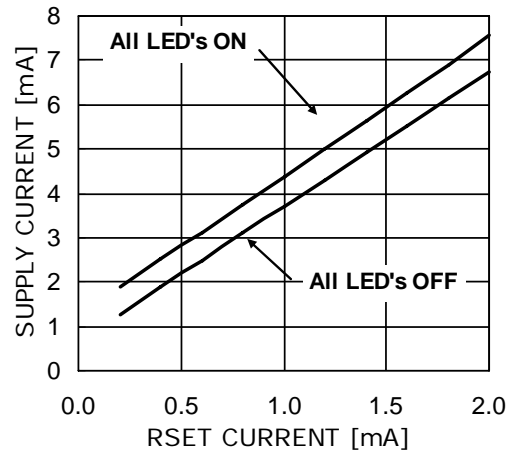
Supply Current vs. VDD Pin Voltage



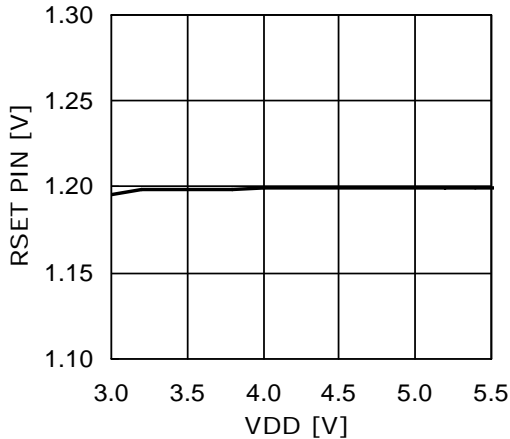
LED Current vs. VDD Pin Voltage



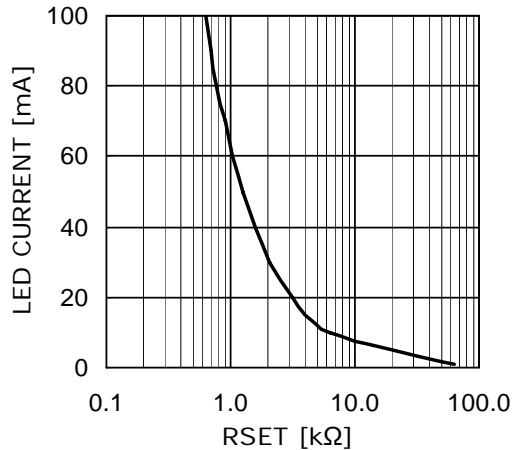
Supply Current vs. RSET Current



RSET Voltage vs. VDD Pin Voltage

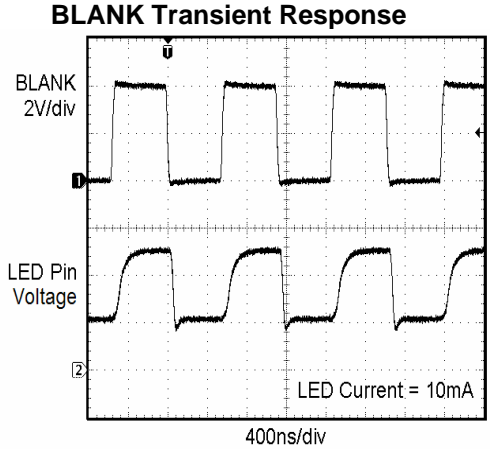
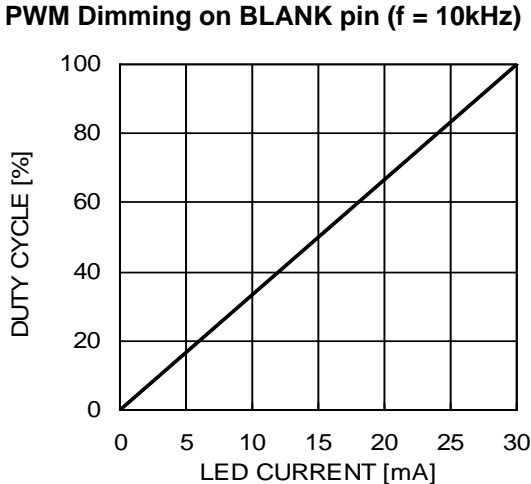
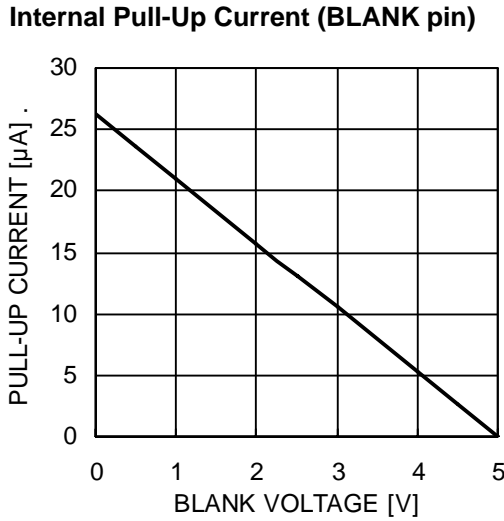
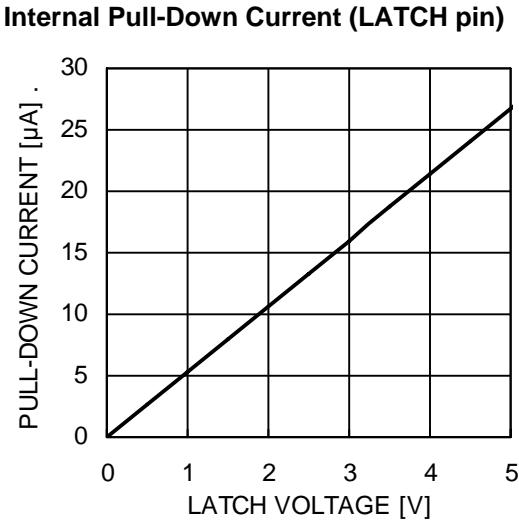
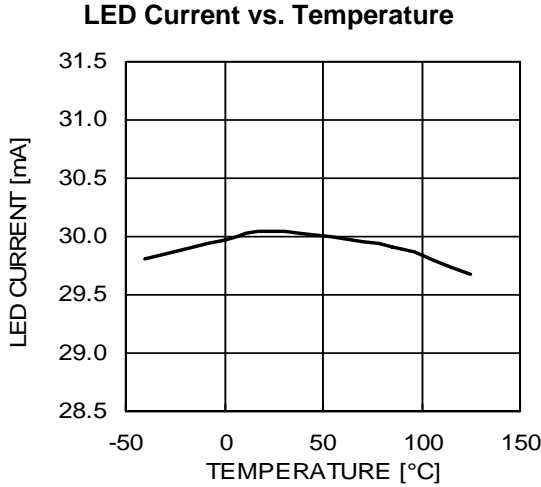
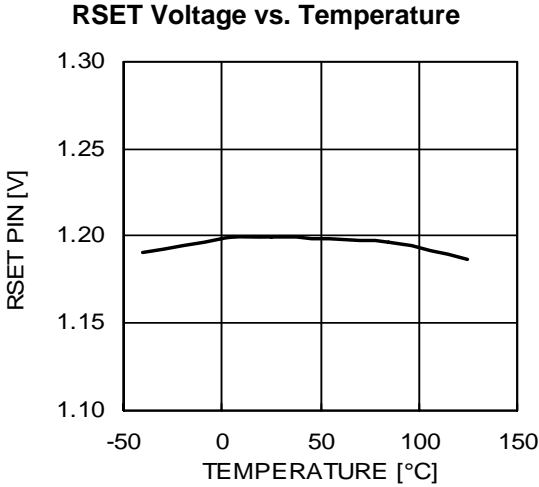


LED Current vs. RSET Resistor



TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 5.0V$, LED current 30mA, all LEDs On, $T_{AMB} = 25^{\circ}C$ unless otherwise specified.



PIN DESCRIPTION

Name	Function
GND	Ground
SIN	Serial data input pin
CLK	Serial clock input pin
LATCH	Latch serial data to output registers
LED1-LED8	LED channel 1 to 8 cathode terminals
BLANK	Enable / disable all channels
SOUT	Serial data output pin.
RSET	LED current set pin
VDD	Positive supply Voltage

PIN FUNCTION

GND is the ground reference pin for the device. This pin must be connected to the ground plane on the PCB.

SIN is the serial data input. Data is loaded into the internal register on each rising edge of CLK.

CLK is the serial clock input. On each rising CLK edge, data is transferred from SIN to the internal 8-bit serial shift register.

LATCH is the latch data input. On the rising edge of LATCH, data is loaded from the 8-bit serial shift register into the output register latch. On the falling edge, this data is latched in the output register and isolated from the state of the serial shift register.

LED1 – LED8 are the LED current sink channels. These pins are connected to the LED cathodes. The current sinks drive the LEDs with a current equal to about 51 times RSET pin current. For the LED sink to operate correctly, the voltage on the LED pin must be above 0.4V.

BLANK is the LED channel enable and disable input pin. When low, LEDs are enabled according to the output latch register content. When high, all LEDs are off, while preserving the data in the output latch register.

SOUT is the serial data output of the 8-bit serial shift register. This pin is used to cascade several devices on the serial bus. The SOUT pin is then connected to the SIN input of the next device on the serial bus to cascade.

RSET is the LED current setting pin. A resistor is connected between this pin and ground. Each LED channel current is set to about 51 times the current pulled out of the pin. The RSET pin voltage is regulated to 1.2V.

VDD is the positive supply pin voltage for the entire device. A small 1 μ F ceramic is recommended close to pin.

CURRENT SETTING RESISTOR

Table 1 lists standard resistor values for various LED current settings.

Table 1. LED Current and RSET resistor values

LED Current [mA]	R _{SET} [k Ω]
10	6.19
20	3.09
30	2.05
40	1.54
60	1.02
80	0.768

BLOCK DIAGRAM

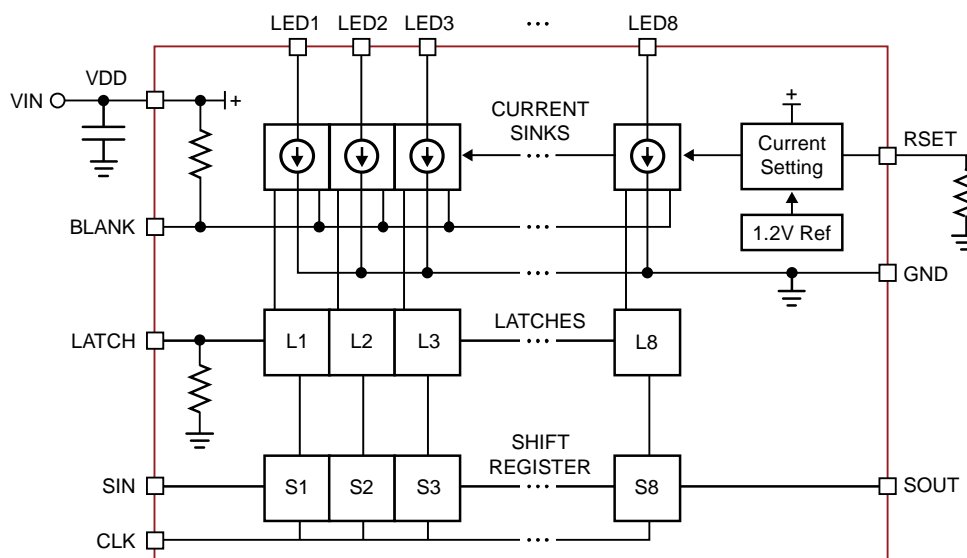


Figure 2. CAT4008 Functional Block Diagram

BASIC OPERATION

The CAT4008 uses 8 tightly matched current sinks to accurately regulate the LED current in each channel. The external resistor, R_{SET} , is used to set the LED

$$\text{LED current} \cong 51 \times \frac{1.2}{R_{SET}}$$

channel current to about 51 times the current in R_{SET} .

Tight current regulation for all channels is possible over a wide range of input and LED voltages due to independent current sensing circuitry on each channel. The LED channels have a maximum dropout of 0.4V for most current and supply voltage conditions. This helps improve the heat dissipation and efficiency of the LED driver.

Upon power-up, an under-voltage lockout circuit clears all latches and shift registers and sets all outputs to off. Once the under-voltage lockout threshold has been reached the device can be programmed.

The driver delays the activation of each consecutive LED output channel by 17ns (typical). Relative to LED1, LED2 is delayed by 17ns, LED3 by 34ns and LED8 by 120ns typical. The delay is introduced when LATCH is activated. The delay minimizes the inrush current on the LED supply by staggering the turn on and off current spikes over a period of time and therefore allowing usage of smaller bypass capacitors.

Pull-up and pull-down resistors are internally provided to set the state of the BLANK and LATCH pins to the off-state when not externally driven.

SERIAL INTERFACE

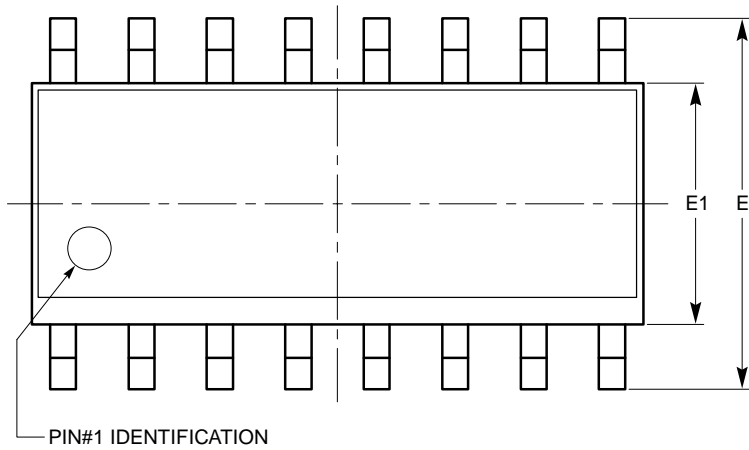
A high-speed serial 4-wire interface is provided to program the state of each LED on or off. The interface contains an 8-bit serial to parallel shift register (S1-S8) and an 8-bit latch (L1-L8). Programming the serial to parallel register is accomplished via SIN and CLK input pins. On each rising edge of the CLK signal, the data from SIN is moved through the shift register serially. Data is also moved out of SOUT which can be connected to a next device if programming more than one device on the same interface.

On the rising edge of LATCH, the data contents of the serial to parallel shift register is reflected in the latches. On the falling edge of LATCH, the state of the serial to parallel register at that particular time is saved in the latches and does not change irrespective of the contents of the serial to parallel register.

BLANK is used to disable all LEDs (turn off) simultaneously while maintaining the same data in the latch register. When low, the LED outputs reflect the data in the latches. When high, all outputs are high impedance (zero current).

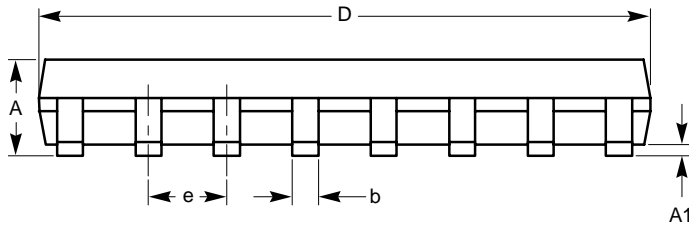
PACKAGE OUTLINE DRAWINGS

SOIC 16-Lead Narrow Body 150mils (W) ⁽¹⁾⁽²⁾

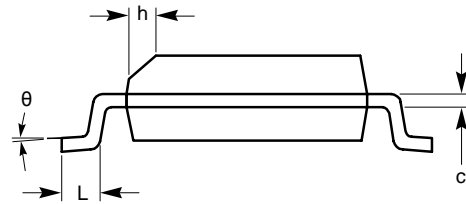


SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°

TOP VIEW



SIDE VIEW



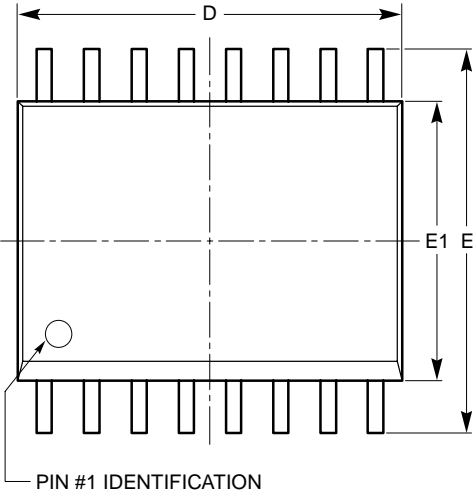
END VIEW

For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

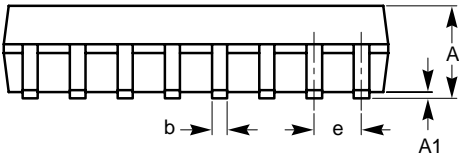
- (1) All dimensions in millimeters. Angle in degrees.
- (2) Complies with JEDEC MS-012

SOIC 16-Lead Wide Body 300mils (V) ⁽¹⁾⁽²⁾

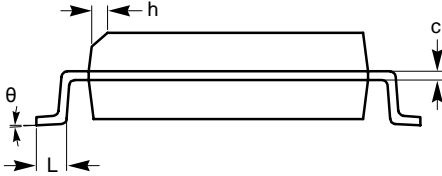


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
b	0.33	0.41	0.51
c	0.18	0.23	0.28
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC		
h	0.25		0.75
L	0.38	0.81	1.27
θ	0°		8°



SIDE VIEW



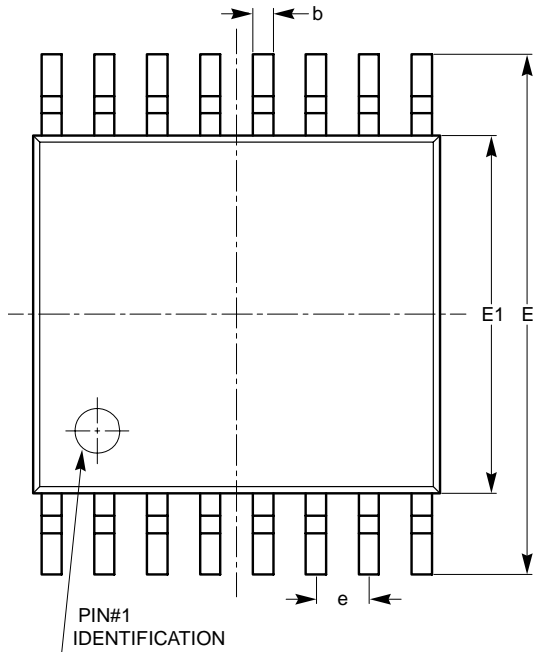
END VIEW

For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

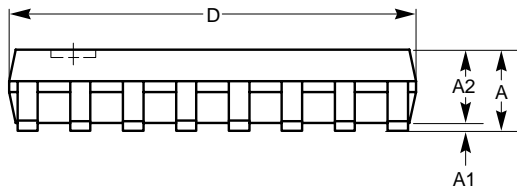
- (1) All dimensions in millimeters. Angle in degrees.
- (2) Complies with JEDEC MS-013.

TSSOP 16-Lead 4.4mm (Y)⁽¹⁾⁽²⁾

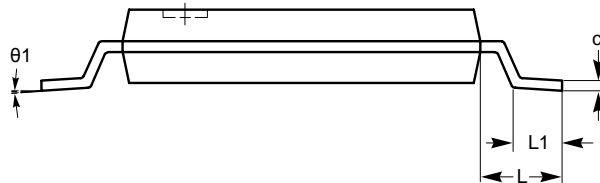


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
$\theta 1$	0°		8°



SIDE VIEW



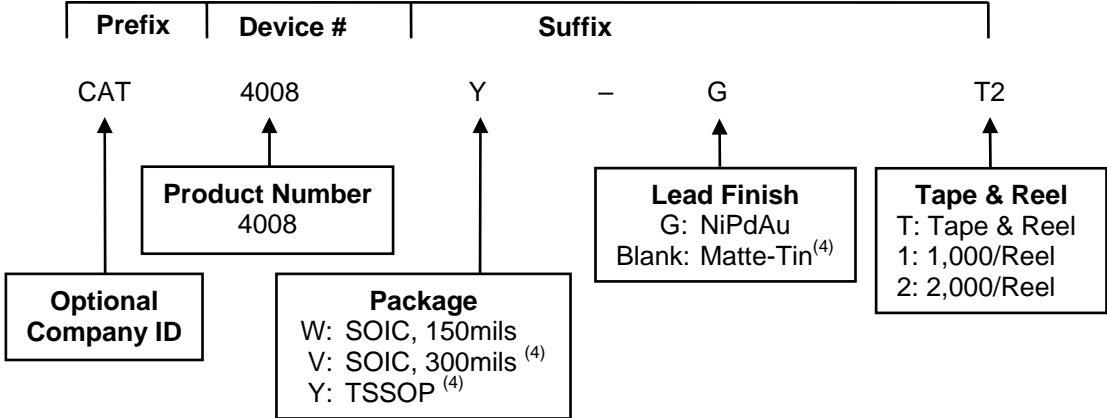
END VIEW

For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

- (1) All dimensions in millimeters. Angle in degrees.
- (2) Complies with JEDEC MO-153.

EXAMPLE OF ORDERING INFORMATION




Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is Matte-Tin.
- (3) The device used in the above example is a CAT4008W-T2 (TSSOP, NiPdAu, Tape & Reel, 2,000/Reel).
- (4) Contact factory for package availability.
- (5) For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

REVISION HISTORY

Date	Rev.	Reason
10-Jan-08	A	Initial Issue
17-Nov-08	B	Change logo and fine print to ON Semiconductor
03-Feb-09	C	Update Ordering Information with NiPdAu Plated Finish package

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center:
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative