

DESCRIPTION

This family is a 16M bit dynamic RAM organized 1,048,576 x 16-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode is a kind of page mode which is useful for the read operation. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60, 70 or 80ns) and refresh cycle(1K ref. or 4K ref.) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Fast Page mode operation
- Read-modify-write Capability
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- JEDEC standard pinout
- 42-pin Plastic SOJ (400mil)
44/50-pin plastic TSOP-II (400mil)
- Single power supply of 5.0V ± 10%
- Early write or output enable controlled write
- Max. Active power dissipation
- Fast access time and cycle time

| Speed | 1K refresh | 4K refresh |
|-------|------------|------------|
| 60 | 880mW | 550mW |
| 70 | 825mW | 495mW |
| 80 | 770mW | 440mW |

| Speed | tRAC | tCAC | tPC |
|-------|------|------|------|
| 60 | 60ns | 15ns | 40ns |
| 70 | 70ns | 20ns | 45ns |
| 80 | 80ns | 20ns | 50ns |

- Refresh cycle

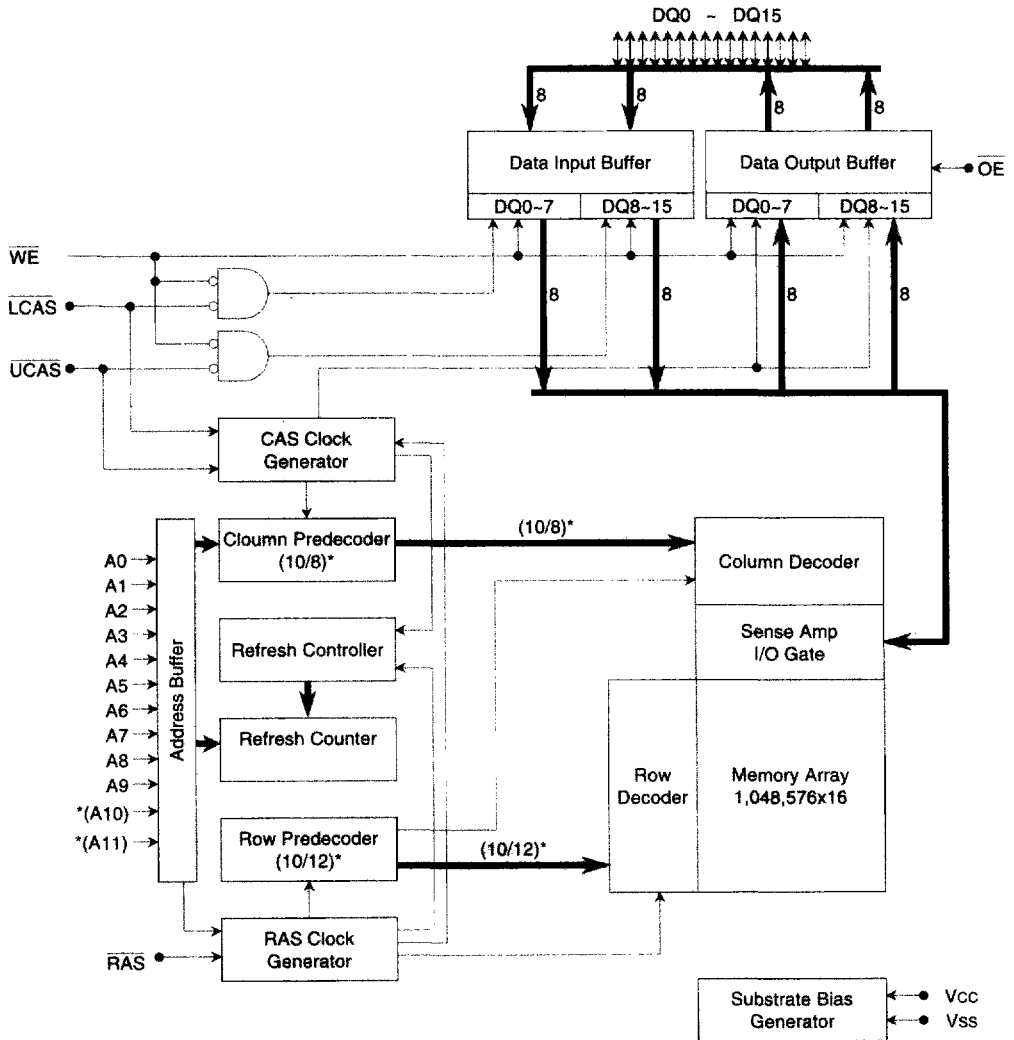
| Part number | Refresh | Normal | SL-part |
|-------------|---------|--------|---------|
| HY5118160B | 1K | 16ms | 256ms |
| HY5116160B | 4K | 64ms | |

ORDERING INFORMATION

| Part Name | Refresh | Power | Package |
|----------------|---------|---------|------------------|
| HY5118160BJC | 1K | | 42Pin SOJ |
| HY5118160BSLJC | 1K | SL-part | 42Pin SOJ |
| HY5118160BTC | 1K | | 44/50Pin TSOP-II |
| HY5118160BSLTC | 1K | SL-part | 44/50Pin TSOP-II |
| HY5116160BJC | 4K | | 42Pin SOJ |
| HY5116160BSLJC | 4K | SL-part | 42Pin SOJ |
| HY5116160BTC | 4K | | 44/50Pin TSOP-II |
| HY5116160BSLTC | 4K | SL-part | 44/50Pin TSOP-II |

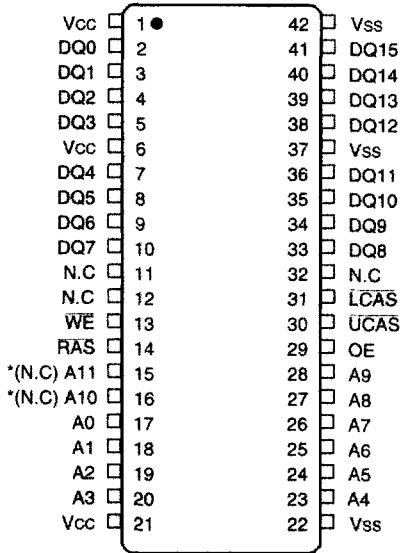
*SL : Low power with self refresh

FUNCTIONAL BLOCK DIAGRAM

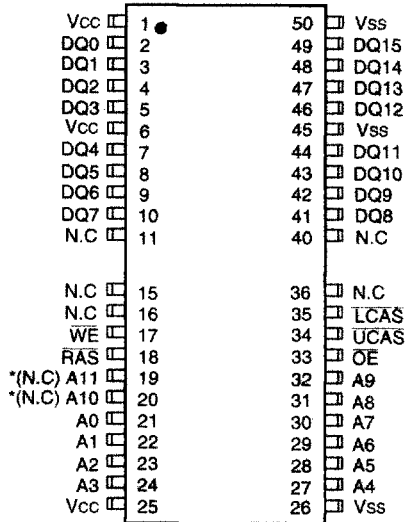


*(A10) and *(A11) for 4K refresh part
(1K Refresh / 4K Refresh)*

PIN CONFIGURATION (Marking Side)



42Pin Plastic SOJ (400mil)



44/50Pin Plastic TSOP-II (400mil)

*(N.C) : For 1K refresh product

PIN DESCRIPTION

| Pin Name | Parameter |
|----------|------------------------------------|
| /RAS | Row Address Strobe |
| /CAS | Column Address Strobe |
| /WE | Write Enable |
| /OE | Output Enable |
| A0-A11 | Address Input (4K Refresh Product) |
| A0-A9 | Address Input (1K Refresh Product) |
| DQ0-DQ15 | Data In/Out |
| Vcc | Power (5.0V) |
| Vss | Ground |
| NC | No Connection |

ABSOLUTE MAXIMUM RATING

| Symbol | Parameter | Rating | Unit |
|------------------------------------|--|-------------|----------|
| TA | Ambient Temperature | 0 to 70 | °C |
| TSTG | Storage Temperature | -55 to 150 | °C |
| V _{IN} , V _{OUT} | Voltage on Any Pin relative to V _{SS} | -1.0 to 7.0 | V |
| V _{CC} | Voltage on V _{CC} relative to V _{SS} | -1.0 to 7.0 | V |
| I _{OS} | Short Circuit Output Current | 50 | mA |
| P _D | Power Dissipation | 1 | W |
| T _{SOLDER} | Soldering Temperature · Time | 260 · 10 | °C · sec |

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

| Symbol | Parameter | Min | Typ | Max | UNIT |
|-----------------|----------------------|------|-----|----------------------|------|
| V _{CC} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.4 | - | V _{CC} +1.0 | V |
| V _{IL} | Input Low Voltage | -1.0 | - | 0.8 | V |

Note : All voltages are referenced to V_{SS}.

DC OPERATING CHARACTERISTIC

| Symbol | Parameter | Test condition | Min | Max | Unit |
|-----------------|---------------------------------------|--|-----|-----|------|
| I _{LI} | Input Leakage Current (Any input) | V _{SS} ≤ V _{IN} ≤ V _{CC} + 1.0 All other pins not under test = V _{SS} | -10 | 10 | μA |
| I _{LO} | Output Leakage Current (Any input) | V _{SS} ≤ V _{OUT} ≤ V _{CC} /RAS & /CAS at V _{IH} | -10 | 10 | μA |
| V _{OL} | Output Low Voltage | I _{OL} = 4.2mA | - | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -5.0mA | 2.4 | - | V |

DC CHARACTERISTICS

(TA = 0°C to 70°C, Vcc = 5.0V ± 10%, Vss = 0V, unless otherwise noted.)

| Symbol | Parameter | Test condition | Speed | Max. Current | | Unit |
|--------|-----------------------------------|---|--------------|--------------|----------|----------|
| | | | | 1K Ref | 4K Ref | |
| Icc1 | Operating Current | /RAS, /CAS Cycling tRC = tRC(min.) | 60 | 160 | 100 | mA |
| | | | 70 | 150 | 90 | |
| | | | 80 | 140 | 80 | |
| Icc2 | TTL Standby Current | /RAS, /CAS ≥ VIH Other inputs ≥ Vss | SL-part | 2 1 | 2 1 | mA |
| Icc3 | /RAS-only Refresh Current | /RAS Cycling, /CAS = VIH tRC = tRC(min.) | 60 | 160 | 100 | mA |
| | | | 70 | 150 | 90 | |
| | | | 80 | 140 | 80 | |
| Icc4 | Fast Page Mode Current | /CAS Cycling, /RAS = VIL tPC = tPC(min.) | 60 | 110 | 90 | mA |
| | | | 70 | 100 | 80 | |
| | | | 80 | 90 | 70 | |
| Icc5 | CMOS Standby Current | /RAS = /CAS ≥ Vcc - 0.2V | SL-part | 1 300 | 1 300 | mA μA |
| Icc6 | /CAS-before-/RAS Refresh Current | /RAS & /CAS = 0.2V tRC = tRC(min.) | 60 | 160 | 100 | mA |
| | | | 70 | 150 | 90 | |
| | | | 80 | 140 | 80 | |
| Icc7 | Battery Back-up Current (SL-part) | tRC=250μs (1K Ref), 62.5μs (4K Ref) /CAS = CBR cycling or 0.2V /OE & /WE = Vcc - 0.2V Address = Vcc-0.2V or 0.2V DQ0-DQ15 = Vcc-0.2, 0.2V or Open | tRAS ≤ 300ns | 350 | 350 | μA |
| | | | tRAS ≤ 1μs | 450 | 450 | |
| Icc8 | Self Refresh Current (SL-part) | /RAS & /CAS = 0.2V Other pins are same as Icc7 | | 350 | 350 | μA |

Note

- Icc1, Icc3, Icc4 and Icc6 depend on output loading and cycle rates(tRC and tPC).
- Specified values are obtained with output unloaded.
- Icc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=VIH within one Fast Page mode cycle time tPC.

AC CHARACTERISTICS

(TA = 0 °C to 70 °C, Vcc = 5.0V ± 10%, Vss = 0V, unless otherwise noted.)

| Symbol | Parameter | 60ns | | 70ns | | 80ns | | Unit | Note |
|--------|---|------|------|------|------|------|------|------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| tRC | Random read or write cycle time | 110 | - | 130 | - | 150 | - | ns | |
| tRWC | Read-modify-write cycle time | 155 | - | 170 | - | 200 | - | ns | |
| tPC | Fast Page mode cycle time | 40 | - | 45 | - | 50 | - | ns | |
| tPRWC | Fast Page mode read-modify-write cycle time | 80 | - | 95 | - | 105 | - | ns | |
| tRAC | Access time from /RAS | - | 60 | - | 70 | - | 80 | ns | 4,5,6 |
| tCAC | Access time from /CAS | - | 15 | - | 20 | - | 20 | ns | 4,5 |
| tAA | Access time from column address | - | 30 | - | 35 | - | 40 | ns | 4,6 |
| tCPA | Access time from column precharge | - | 35 | - | 40 | - | 45 | ns | 4 |
| tCLZ | /CAS to output low impedance | 0 | - | 0 | - | 0 | - | ns | 4 |
| tOFF | Output buffer turn-off delay from /CAS | 0 | 15 | 0 | 15 | 0 | 15 | ns | 7 |
| tT | Transition time(rise and fall) | 3 | 50 | 3 | 50 | 3 | 50 | ns | 2 |
| tRP | /RAS precharge time | 40 | - | 50 | - | 50 | - | ns | |
| tRAS | /RAS pulse width | 60 | 10K | 70 | 10K | 70 | 10K | ns | |
| tRASP | /RAS pulse width(Fast Page mode) | 60 | 100K | 70 | 100K | 70 | 100K | ns | |
| tRSH | /RAS hold time | 15 | - | 20 | - | 20 | - | ns | |
| tCSH | /CAS hold time | 60 | - | 70 | - | 80 | - | ns | |
| tCAS | /CAS pulse width | 15 | 10K | 15 | 10K | 20 | 10K | ns | |
| tRCD | /RAS to /CAS delay time | 20 | 45 | 20 | 50 | 20 | 60 | ns | 5 |
| tRAD | /RAS to column address delay time | 15 | 30 | 15 | 35 | 15 | 40 | ns | 6 |
| tCRP | /CAS to /RAS precharge time | 5 | - | 5 | - | 5 | - | ns | |
| tCP | /CAS precharge time | 10 | - | 10 | - | 10 | - | ns | |
| tASR | Row address set-up time | 0 | - | 0 | - | 0 | - | ns | |
| tRAH | Row address hold time | 10 | - | 10 | - | 10 | - | ns | |
| tASC | Column address set-up time | 0 | - | 0 | - | 0 | - | ns | |
| tCAH | Column address hold time | 10 | - | 15 | - | 15 | - | ns | |
| tRAL | Column address to /RAS lead time | 30 | - | 35 | - | 40 | - | ns | |
| tRCS | Read command set-up time | 0 | - | 0 | - | 0 | - | ns | |
| tRCH | Read command hold time referenced to /CAS | 0 | - | 0 | - | 0 | - | ns | 8 |
| tRRH | Read command hold time referenced to /RAS | 0 | - | 0 | - | 0 | - | ns | 8 |
| tWCH | Write command hold time | 15 | - | 15 | - | 15 | - | ns | |
| tWP | Write command pulse width | 10 | - | 10 | - | 10 | - | ns | |
| tRWL | Write command to /RAS lead time | 20 | - | 20 | - | 20 | - | ns | |
| tCWL | Write command to /CAS lead time | 20 | - | 20 | - | 20 | - | ns | 14 |

AC CHARACTERISTICS

Continued

| Symbol | Parameter | 60ns | | 70ns | | 80ns | | Unit | Note |
|--------|--|------|-----|------|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| tDS | Data-in set-up time | 0 | - | 0 | - | 0 | - | ns | 9 |
| tDH | Data-in hold time | 15 | - | 15 | - | 15 | - | ns | 9 |
| tREF | Refresh period(1024 cycles) | - | 16 | - | 16 | - | 16 | ms | |
| | Refresh period(4096 cycles) | - | 64 | - | 64 | - | 64 | ms | |
| | Refresh period(SL-part) | - | 256 | - | 256 | - | 256 | ms | |
| twCS | Write command set-up time | 0 | - | 0 | - | 0 | - | ns | 10 |
| tcWD | /CAS to /WE delay time | 45 | - | 50 | - | 50 | - | ns | 10,13 |
| trWD | /RAS to /WE delay time | 85 | - | 95 | - | 105 | - | ns | 10 |
| tAWD | Column address to /WE delay time | 55 | - | 60 | - | 65 | - | ns | 10 |
| tCSR | /CAS set-up time(CBR cycle) | 5 | - | 5 | - | 5 | - | ns | 15 |
| tCHR | /CAS hold time(CBR cycle) | 10 | - | 10 | - | 10 | - | ns | 16 |
| trPC | /RAS to /CAS precharge time | 5 | - | 5 | - | 5 | - | ns | |
| tcPT | /CAS precharge time(CBR counter test) | 30 | - | 35 | - | 40 | - | ns | 12 |
| trOH | /RAS hold time referenced to /OE | 10 | - | 10 | - | 10 | - | ns | |
| toEA | /OE access time | - | 15 | - | 20 | - | 20 | ns | |
| toED | /OE to data delay time | 15 | - | 20 | - | 20 | - | ns | |
| toEZ | Output buffer turn-off delay time from /OE | 0 | 15 | 0 | 15 | 0 | 15 | ns | 7 |
| toEH | /OE command hold time | 15 | - | 20 | - | 20 | - | ns | |
| tcPWD | /WE delay time from /CAS precharge | 55 | - | 65 | - | 75 | - | ns | 10 |
| trHCP | /RAS hold time from /CAS precharge | 40 | - | 40 | - | 50 | - | ns | |
| tWRP | /WE to /RAS precharge time(CBR cycle) | 10 | - | 10 | - | 10 | - | ns | |
| tWRH | /WE to /RAS hold time(CBR cycle) | 10 | - | 10 | - | 10 | - | ns | |
| trASS | /RAS pulse width(self refresh) | 100K | - | 100K | - | 100K | - | ns | |
| trPS | /RAS Precharge Time (Self refresh) | 110 | - | 130 | - | 150 | - | ns | |
| tCHS | /CAS Hold Time (Self refresh) | -50 | - | -50 | - | -50 | - | ns | |

NOTE

1. An initial pause of 200 μ s is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
3. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA=0 to 70°C) is assured.
4. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 2TTL loads and 100pF.
5. Operation within the tRCD(max.) limit ensures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
6. Operation within the tRAD(max.) limit ensures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
7. tOFF and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to /LCAS or /UCAS leading edge in early write cycles and to /WE leading edge in read-modify-write cycles.
10. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS \geq tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD \geq tRWD(min.), tCWD \geq tCWD(min.), tAWD \geq tAWD(min.), and tCPWD \geq tCPWD(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. tASC, tCAH are referenced to the earlier /CAS falling edge.
12. tCP and tCPT are measured when both /LCAS and /UCAS are high state.
13. tCWD is referenced to the later /CAS falling edge at word read-modify-write cycle.
14. tCWL must be satisfied by both /LCAS and /UCAS for 16-bit access cycles.
15. tCSR is referenced to the earlier /CAS falling before /RAS transition low.
16. tCHR is referenced to the later /CAS rising high after /RAS transition low.
17. tDS, tDH is independently specified for lower byte DQ(0-7), upper byte DQ(8-15).

CAPACITANCE

(TA = 25°C, VCC = 5.0V \pm 10%, VSS = 0V and f=1MHz, unless otherwise noted.)

| Symbol | Parameter | Typ. | Max | Unit |
|--------|--|------|-----|------|
| CIN1 | Input Capacitance (A0-A11) | - | 5 | pF |
| CIN2 | Input Capacitance (/RAS, /LCAS, /UCAS, /WE, /OE) | - | 7 | pF |
| CDQ | Data Input / Output Capacitance (DQ0-DQ15) | - | 7 | pF |