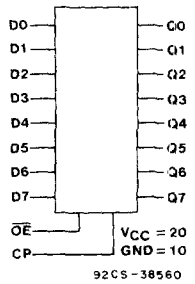
CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574

File Number **1663**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop, 3-State Positive-Edge Triggered

Type Features:

- *Common 3-State Output Enable Control*
- *Buffered Inputs*
- *3-State Outputs*
- *Bus Line Driving Capability*
- *Typical Propagation Delay (Clock to Q) = 15 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA CD54/74HC374/574 and CD54/74HCT374/574 are Octal D-Type Flip-Flops with 3-State Outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When Output Enable ($\overline{OE}$) is HIGH the outputs will be in the high impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

The CD54HC/HCT374/574 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD54HC/HCT374/574 are supplied in a 20-lead plastic dual-in-line plastic package (E suffix) and in 20-lead plastic dual-in-line surface mount plastic packages (M suffix). The CD54HC/HCT374/574 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

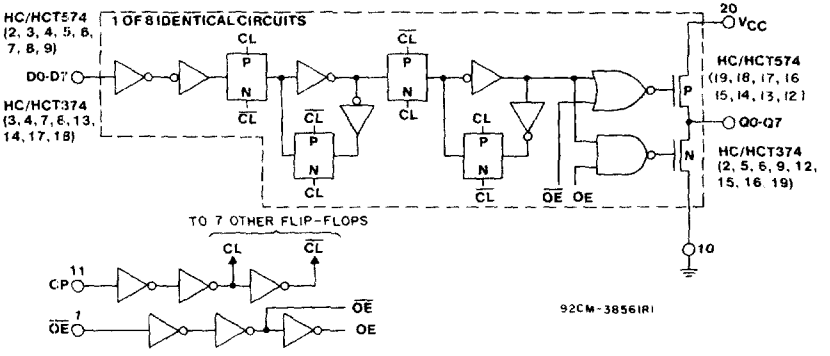


Fig. 1 - Logic diagram.

CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\text{ V} < V_o < V_{CC} + 0.5$V) ..... ±35mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}) ..... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... **400 mW**
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... **Derate Linearly at 6 mW/° C to 70 mW**
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE			
INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	↗	H	H
L	↗	L	L
L	L	X	Q0
H	X	X	Z

HC/HCT374,574

H = high level (steady state)
L = low level (steady state)
X = don't care
↗ = transition from low to high level
Q0 = the level of Q before the indicated steady-state input conditions were established.
Z = high impedance

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC374/CD54HC374 CD74HC574/CD54HC574										CD74HCT374/CD54HCT374 CD74HCT574/CD54HCT574									UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*	
	HCT374	HCT574
D0-D7	0.3	0.4
CP	0.9	0.75
$\overline{OE}$	1.3	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay Clock to Q	t_{PLH} t_{PHL}	15	15	15	ns
Propagation Delay Output Disable to Q	t_{PLZ} t_{PHZ}	15	11	11	ns
Propagation Delay Output Enable to Q	t_{PZL} t_{PZH}	15	12	12	ns
Max Clock Frequency	f_{max}	15	60	60	MHz
Power Dissipation Capacitance	C_{PD}*	—	39	47	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_o C_L$ where
f_i = input frequency,
f_o = output frequency,
C_L = output load capacitance
V_{CC} = supply voltage

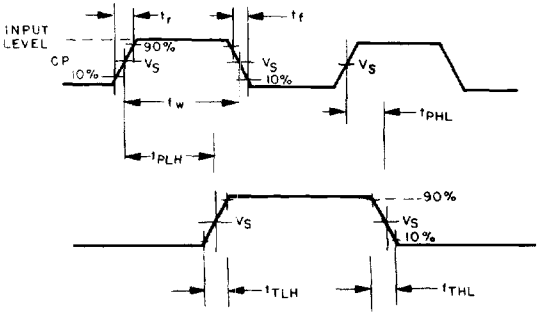
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	30	—	25	—	25	—	20	—	20	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Clock Pulse Width Fig. 2	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time Data to Clock Fig. 3	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data to Clock Fig. 3	t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	

CD54/74HC374, CD54/74HCT374
CD54/74HC574, CD54/74HCT574

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
		V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	165	—	—	—	205	—	—	—	250	—	—	
Clock to Output	t_{PHL}	4.5	—	33	—	33	—	41	—	41	—	50	—	50	ns
Fig. 2		6	—	28	—	—	—	35	—	—	—	43	—	—	
Propagation Delay	t_{PLZ}	2	—	135	—	—	—	170	—	—	—	205	—	—	
Output Disable to Q	t_{PHZ}	4.5	—	27	—	28	—	34	—	35	—	41	—	42	ns
Fig. 4		6	—	23	—	—	—	29	—	—	—	35	—	—	
Propagation Delay	t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Output Enable to Q	t_{PZH}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
Fig. 4		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
Fig. 2		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

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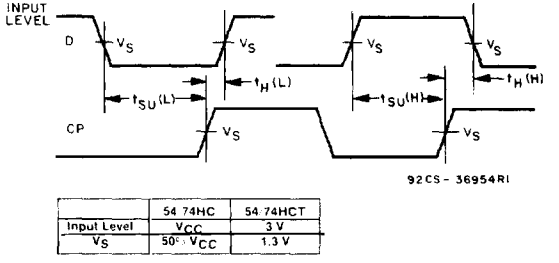
Fig. 2 — Clock to output delays and clock pulse width.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

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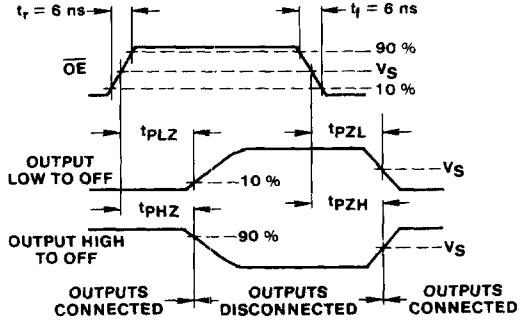
Fig. 3 — Data set-up and hold times.



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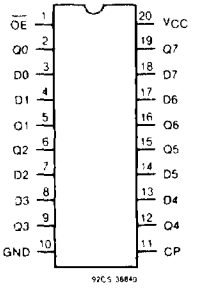
	54/74HC	54/74HCT
Input Level	**V_{CC}**	**3 V**
Switching Voltage, V_S	**50% V_{CC}**	**1.3 V**

Fig. 4 — Transition times and propagation delay times.



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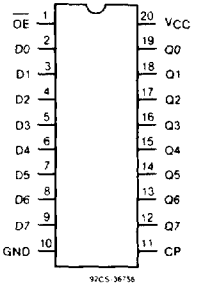
CD54/74HC, HCT374 Types
TERMINAL ASSIGNMENT



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CD54/74HC, HCT574 Types
TERMINAL ASSIGNMENT