SRAM

256K x 4 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 17, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 7 and 8ns
- Complies to JEDEC low-voltage TTL standards

OPTIONS

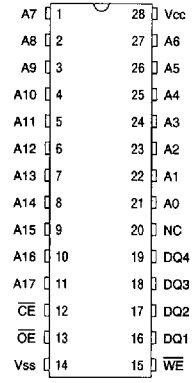
	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
• 2V data retention (optional)	L
• 2V data retention, low power (optional)	LP
• Temperature	
Commercial (0°C to +70°C)	None

- Part Number Example: MT5LC1005DJ-15 LP

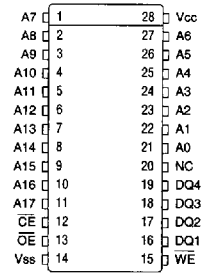
NOTE. Not all combinations of speed, data retention and low power are necessarily available Please contact the factory for availability of specific part number combinations

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-5)



28-Pin SOJ (SD-3)



GENERAL DESCRIPTION

The MT5LC1005 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

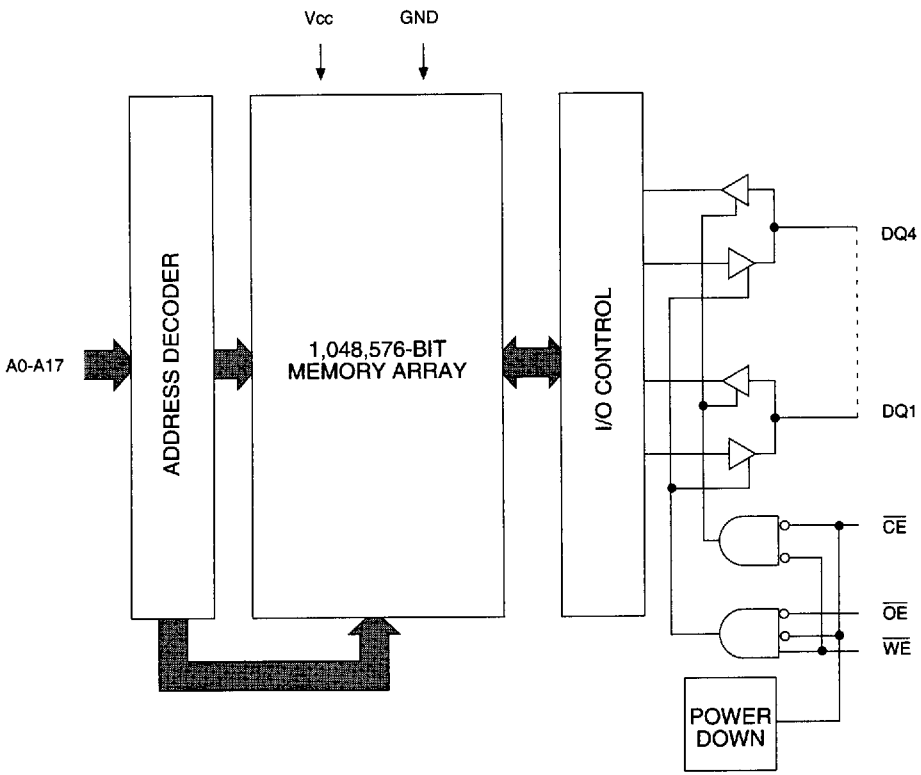
Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ are LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

3.3V ASYNCHRONOUS SRAM

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-15	-17	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{CC}	ALL	70	155	145	135	125	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{SB1}	STD, L	20	45	40	35	30	mA	13
			LP	1.5	3	3	3	3	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	STD, L	1.0	3	3	3	3	mA	13
			LP	0.7	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 3.3V	C_I	6	pF	4
Output Capacitance		C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION	SYM	-15		-17		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	^tRC	15		17		20		25		ns	
Address access time	^tAA		15		17		20		25	ns	
Chip Enable access time	^tACE		15		17		20		25	ns	
Output hold from address change	^tOH	3		3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		17		20		25	ns	
Output Enable access time	^tAOE		6		6		7		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		7		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	15		17		20		25		ns	
Chip Enable to end of write	^tCW	10		12		12		15		ns	
Address valid to end of write	^tAW	10		12		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		12		15		ns	
WRITE pulse width	$^tWP2$	12		8		15		15		ns	
Data setup time	^tDS	7		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

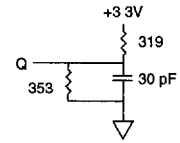


Fig. 1 OUTPUT LOAD EQUIVALENT

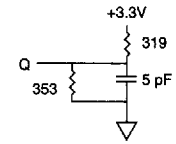


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq Vcc -0.2V$ Other inputs: $V_{IN} \geq Vcc -0.2V$ or $V_{IN} \leq Vss+0.2V$ $Vcc = 2V$	I_{CCDR}		145	260	µA	14
Data Retention Current LP version	$\overline{CE} \geq Vcc -0.2V$ $Vcc = 2V$	I_{CCDR}		145	260	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

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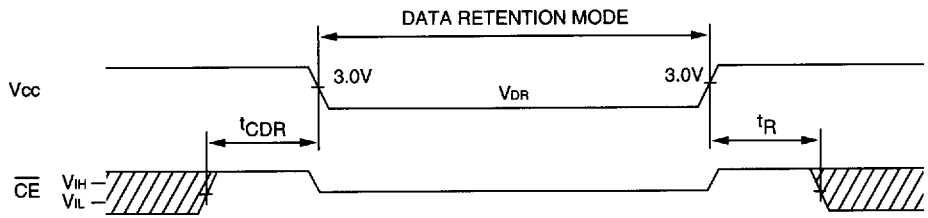
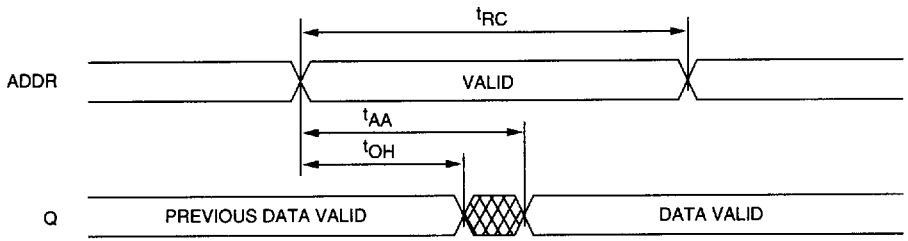
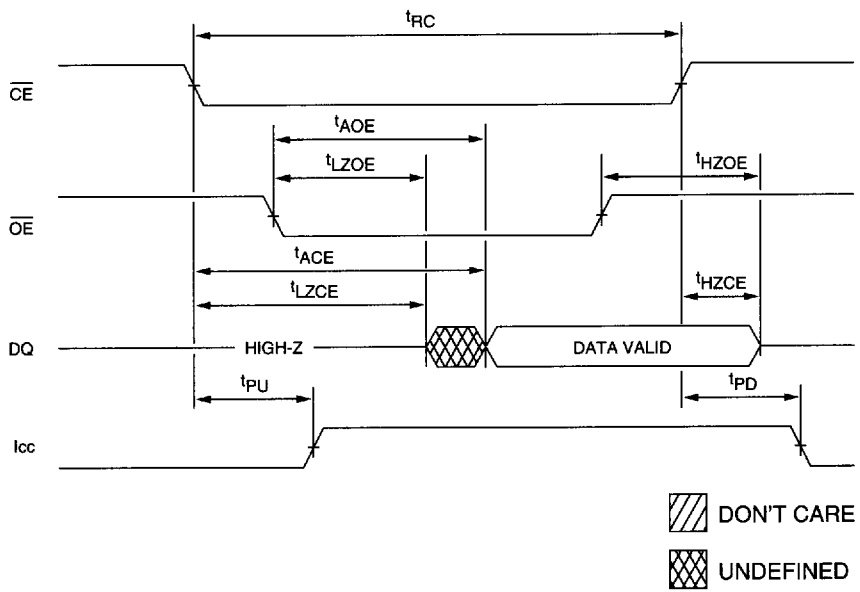
LOW Vcc DATA RETENTION WAVEFORM



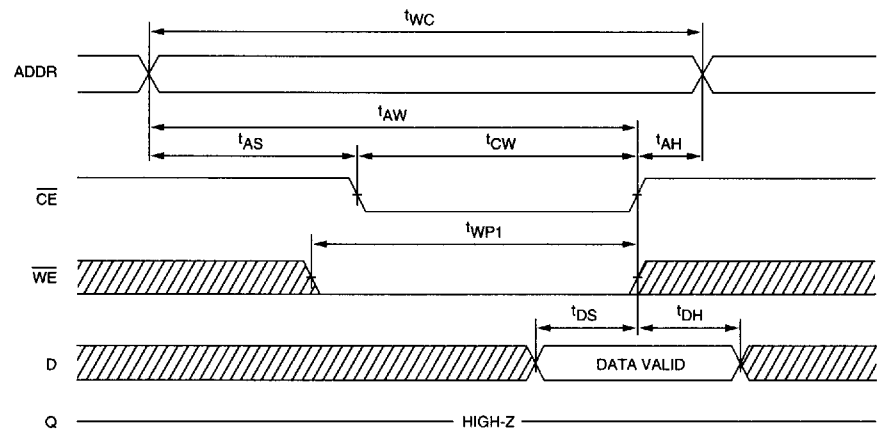
READ CYCLE NO. 1 [8, 9]



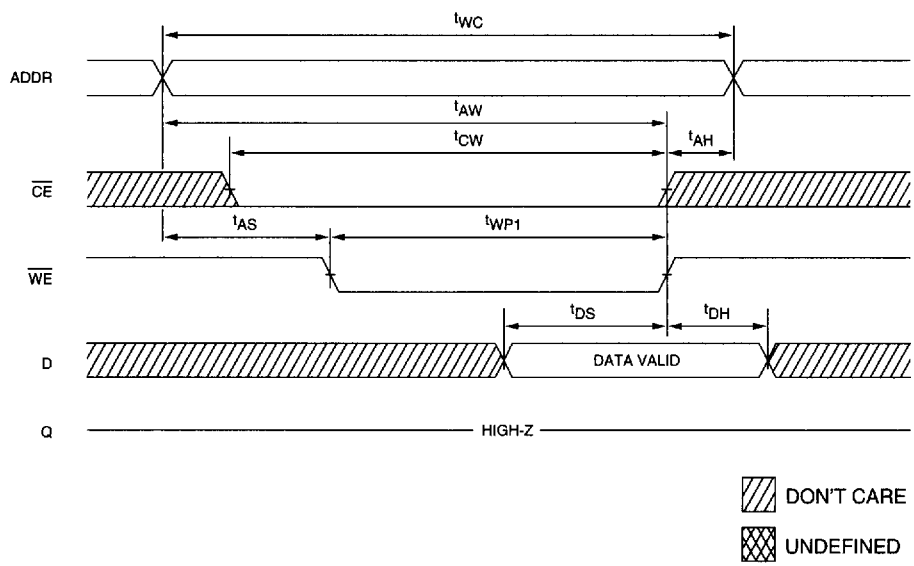
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

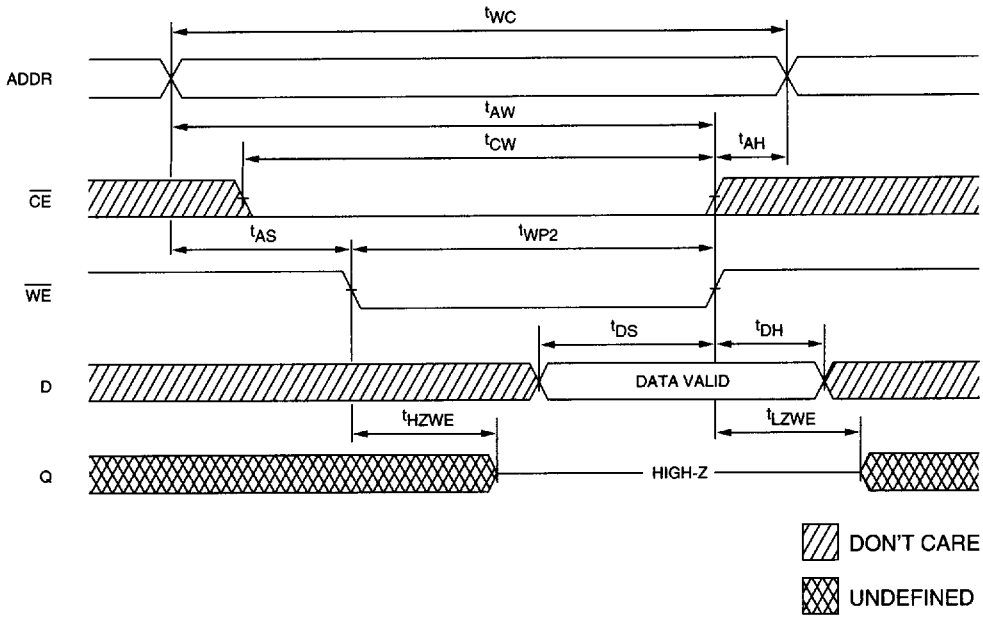


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).