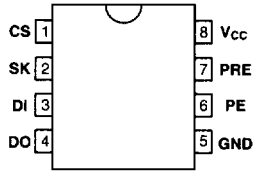
1,024-Bit Serial Electrically Erasable PROM with 2V Read Capability

FEATURES

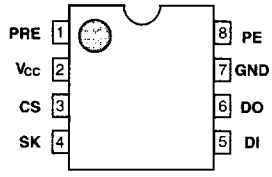
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V and 3V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— Pin-enabled writes to memory and Protect Register**
  - **— Temporary or permanent protection of selected registers**
- **Low Power Consumption**
  - **— 1mA active**
  - **— 1μA standby**
- **Low Voltage Read Operations**
  - **— Read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 100-year data retention after 100K write cycles**
  - **— Minimum of 100,000 erase/write cycles**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS

Plastic Dual-in-line
Type "P" Package



EIAJ Small Outline
"J" Package



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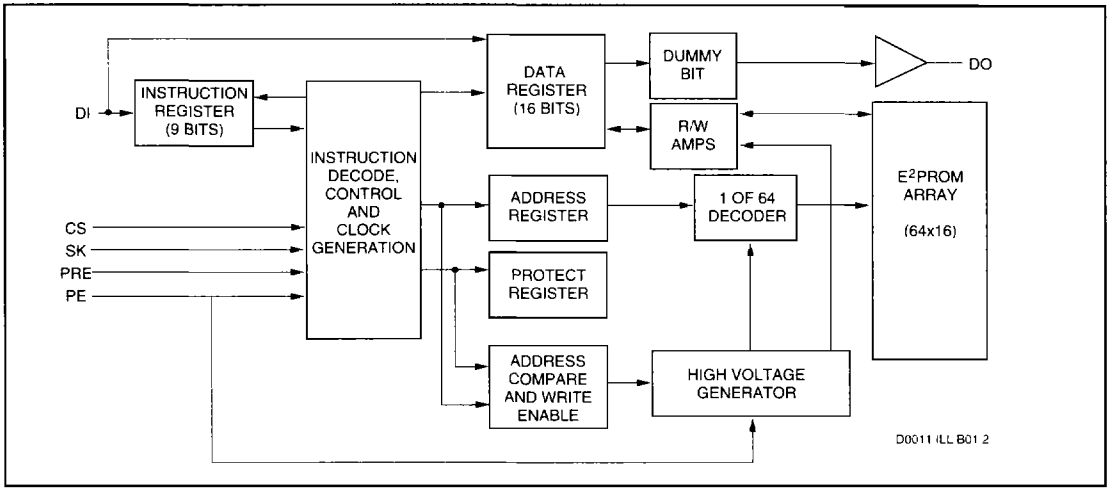
PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
Vcc	Power Supply

OVERVIEW

The XL93CS46 is a low cost 1,024-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93CS46 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Any number of the registers can be protected against data modification by programming the on-chip Protect Register. This register holds the address of the lowest memory register to be protected. The value in the Protect Register can be frozen, ensuring that the selected range of registers can never be altered. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

BLOCK DIAGRAM



The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. To protect against inadvertent writes, the WRITE instruction is accepted only while Program Enable (PE) is held HIGH, and only functions if the selected address is less than the address in the Protect Register. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

APPLICATIONS

The XL93CS46 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93CS46 is designed for applications requiring up to 100,000 erase/write cycles. It provides 100 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93CS46 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93CS46 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XLS93CS46 has been designed to ensure that data read operations are reliable in low voltage environments. The XLS93CS46 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V.

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93CS46 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)
The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle. While the WRITE instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. The WRALL instruction functions only when the Protect Register has been cleared by a PRCLEAR instruction. While the WRALL instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write-disabled state.) To protect data, a

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INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data	PRE Pin	PE Pin
READ	1	10	(A_5-A_0)		0	X
WEN (Write Enable)	1	00	11XXXX		0	1
WRITE	1	01	(A_5-A_0)	D_{15}-D_0	0	1
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0	0	1
WDS (Write Disable)	1	00	00XXXX		0	X
PRREAD (Protect Register Read)	1	10	XXXXXX		1	X
PREN (Protect Register Enable)	1	00	11XXXX		1	1
PRCLEAR (Protect Register Clear)	1	11	111111		1	1
PRWRITE (Protect Register Write)	1	01	(A_5-A_0)		1	1
PRDS (Protect Register Disable)	1	00	000000		1	1
ERASE REGISTER	1	11	(A_5-A_0)		0	1
ERAL (Erase All Registers)	1	00	10XXXX		0	1

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WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{BUSY}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. Registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands cannot be erased. (See Figure 8)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." The erase all (ERAL) command will not erase registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands. (See Figure 9.)

PROTECTION REGISTER LOGIC

Protect Register Read (PRREAD)
The protect register read (PRREAD) instruction causes the address stored in the Protect Register to be output on the DO pin. Data is transferred from the Protect Register into a serial-out shift register. A dummy bit (logical "0") precedes the actual output string. The data on the DO pin changes with the LOW to HIGH transition of the SK clock. While the PRREAD instruction is being loaded, the PRE pin must be held HIGH; then it becomes a DON'T-CARE. (See Figure 10.)

After a PRCLEAR instruction is executed, a PRREAD instruction will return all 1's, even though the highest register is NOT protected.

Protect Register Enable (PREN)
The protect register enable (PREN) instruction enables execution of the PRCLEAR, PRWRITE and PRDS instructions. It must be executed immediately before each of these instructions. (The PREN instruction functions only if the part has been write enabled; see the WEN instruction). Both the PRE and PE pins must be held HIGH while the PREN instruction is being loaded; then they become DON'T-CAREs. (See Figure 11.)

Protect Register Clear (PRCLEAR)
The protect register clear (PRCLEAR) instruction clears the address stored in the Protect Register, making all registers accessible to the WRITE and WRALL instructions. If a PRDS instruction has been executed, the PRCLEAR instruction will not function. A PREN instruction must be executed immediately before a PRCLEAR instruction. While the PRCLEAR instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure12.)

Protect Register Write (PRWRITE)
The protect register write (PRWRITE) instruction is used to load the Protect Register with the address of the lowest register to be protected. After the PRWRITE instruction is executed, only registers with addresses less than the address in the Protect Register can be written by the WRITE instruction. The Protect Register must have been cleared (see the PRCLEAR instruction) before executing a PRWRITE instruction. A PREN instruction must be executed immediately before the PRWRITE instruction. While the PRWRITE instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 13.)

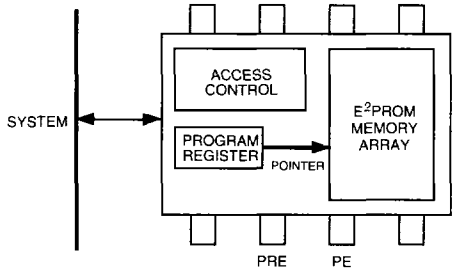
Protect Register Disable (PRDS)
The protect register disable (PRDS) instruction is effective exactly once per part. After this instruction has been executed, the Protect Register will accept no further modifications. All registers with addresses greater than or equal to the address in the Protect Register are permanently protected from the WRITE and WRALL operations. A PREN instruction must be executed immediately before the PRDS instruction. While the PRDS instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 14.)

Figure A shows the status of the memory array regions as defined by the pointer address and the state of the program enable (PE) pin. In the first case, programming operations are enabled through the application of a logic "1" to the PE control pin. All memory locations beneath that of the pointer address are available for data changes. All memory locations at or above the pointer address are protected against data alteration and serve as read only memory.

In the second case, the PE pin is held in a logic "0" state. While this condition is present, the XL93CS46 is protected against any data changes.

The conceptual block diagram, Figure B above, shows the simplicity with which the security features of the XL93CS46 may be managed.



Program register may be permanently set or changed upon command.

FIGURE B

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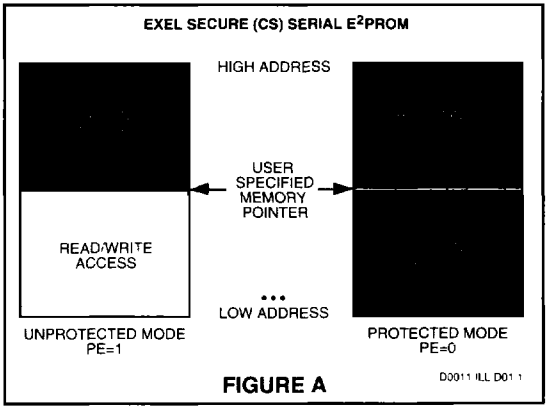

FIGURE A

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The program register is accessed for read or write operations whenever the program register enable (PRE) pin is in a logic "1" state. Normal write operations to the program register establish the E^2 memory array address defining the region to be protected.

When PRE is in a logic "0" state, all read and write operations directed to the XL93CS46 affect the E^2PROM memory array locations.

Setting the address in the program register to the top of the XL93CS46 memory array renders the entire array to be writable. Setting the address to the bottom of the array renders the entire array to be a read only memory.

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ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93CS46 ..... 0°C to +70°C
XLE93CS46 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93CS46
T_A = -40°C to +85°C for the XLE93CS46

Symbol	Parameter	Conditions	XLS93CS46 XLE93CS46 Vcc = 5V + 10%		XLS93CS46-3 XLE93CS46-3 Vcc = 3V + 10%		XLS93CS46 XLS93CS46-3 Vcc = 2V Read		Units
			Min	Max	Min	Max	Min	Max	
I_{CC1}	Operating Current **CMOS** Input Levels	CS = V_{CC}, SK = 1MHz @ 5V		2		n/a		n/a	mA
I_{CC2}	Operating Current **TTL** Input Levels	CS = V_{IH}, SK = 1MHz @ 5V		5		n/a		n/a	mA
I_{CC3}	Operating Current **CMOS** Input Levels	CS = V_{CC}, SK = 250KHz @ 3V		n/a		2		n/a	mA
I_{CC3}	Operating Current **CMOS** Input Levels	CS = V_{CC}, SK = 250KHz @2V **Read** Only		n/a		n/a		2	mA
I_{SB1}	Standby Current	CS = DI = SK=0V		2					µA
I_{LI}	Input Leakage	V_{IN} = 0V to V_{CC}, PE and PRE		20		20		20	µA
I_{LI}	Input Leakage	V_{IN} = 0V to V_{CC}, CS, SK, DI		1		1		1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to V_{CC}, CS = 0V		1		1		1	µA
V_{IL}	Input Low Voltage			0.8	-0.1	0.15V_{CC}	-0.1	0.1V_{CC}	V
V_{IH}	Input High Voltage			V_{CC}	0.8 V_{CC}	V_{CC}	0.9 V_{CC}	$V_{CC}^{+0.2}$	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1µA (TTL)		0.4					V
V_{OH1}	Output High Voltage	I_{OH} = -400µA (TTL)	2.4		n/a		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA (CMOS)		0.2		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA (CMOS)	$V_{CC}^{-0.2}$		$V_{CC}^{-0.2}$		$V_{CC}^{-0.2}$		V

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AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93CS46
or -40°C to +85°C for the XLE93CS46

Symbol	Parameter	Conditions	XLS93CS46 XLE93CS46		XLS93CS46-3 XLE93CS46-3		XLS93CS46 XLS93CS46-3		Units
			V_{CC} = 5V+10%		V_{CC} = 3V+10%		V_{CC} = 2V Read		
			Min	Max	Min	Max	Min	Max	
f_{SK}	SK Clock Frequency			1000		250		250	KHz
t_{SKH}	SK High Time		400		1000		2000		ns
t_{SKL}	SK Low Time		250		1000		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		200		ns
t_{PRES}	PRE Setup Time	Relative to SK ⌐	50		200				ns
t_{PES}	PE Setup Time	Relative to SK ⌐	50		200				ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		400		ns
t_{CSH}	CS Hold Time	Relative to SK ⌐	0		0		0		ns
t_{PEH}	PE Hold Time	Relative to CS ⌐	50		200				ns
t_{PREH}	PRE Hold Time	Relative to CS ⌐	50		200				ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		400		ns
t_{PDI}	Output Delay to "1"	AC Test		500		2000		2000	ns
t_{PDO}	Output Delay to "0"	AC Test		500		2000		2000	ns
t_{SV}	CS to Status Valid	AC Test CL= 100pF		500		2000		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		25		n/a	ms

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CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

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Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

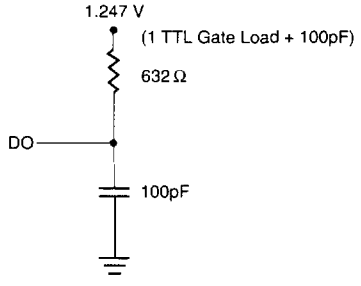

FIGURE 1. AC TEST CONDITIONS

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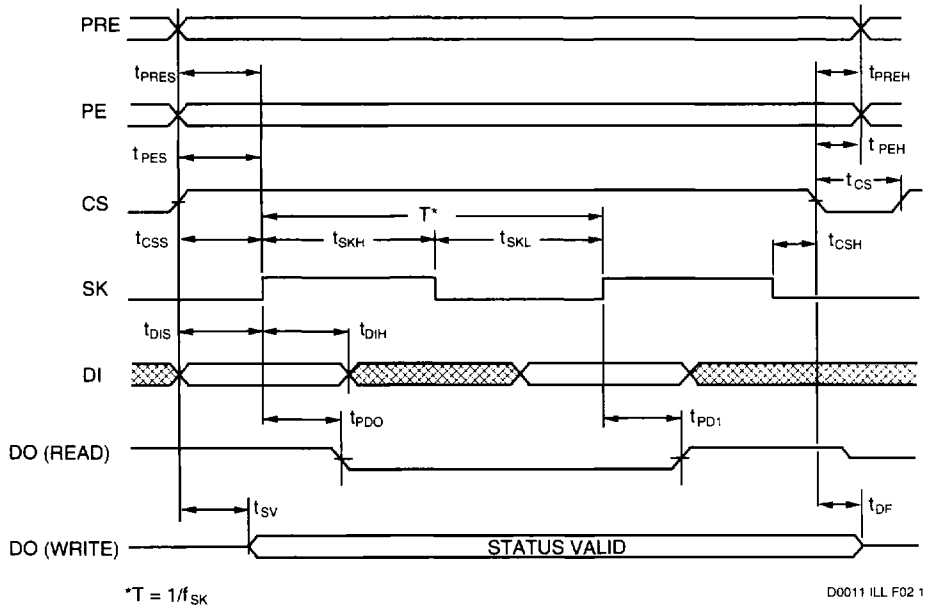

FIGURE 2. SYNCHRONOUS DATA TIMING

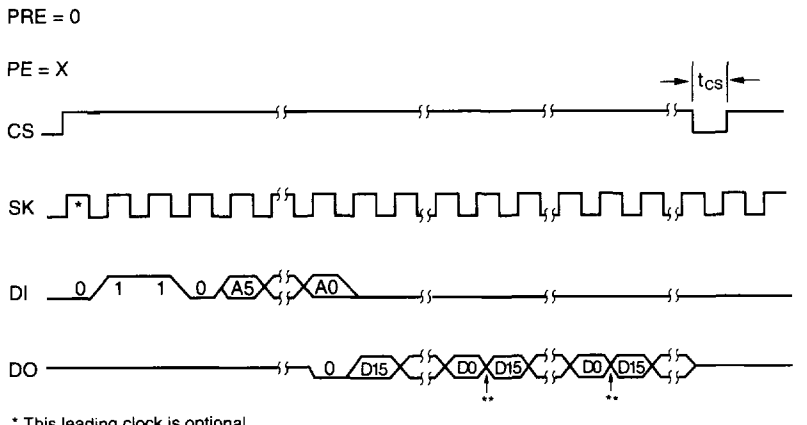

FIGURE 3. READ CYCLE TIMING

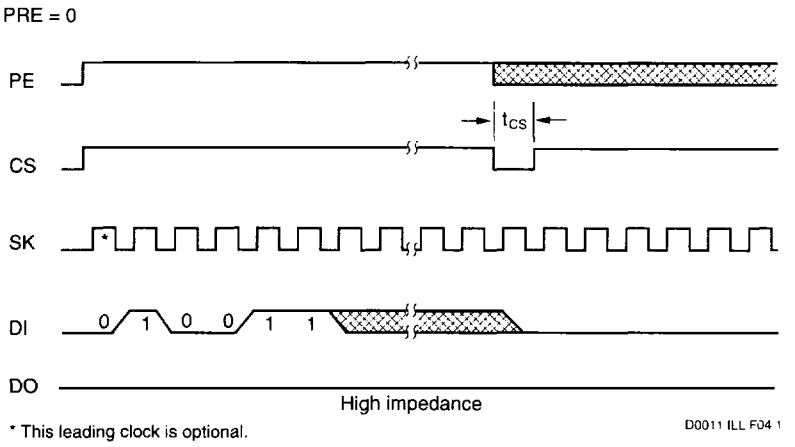

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

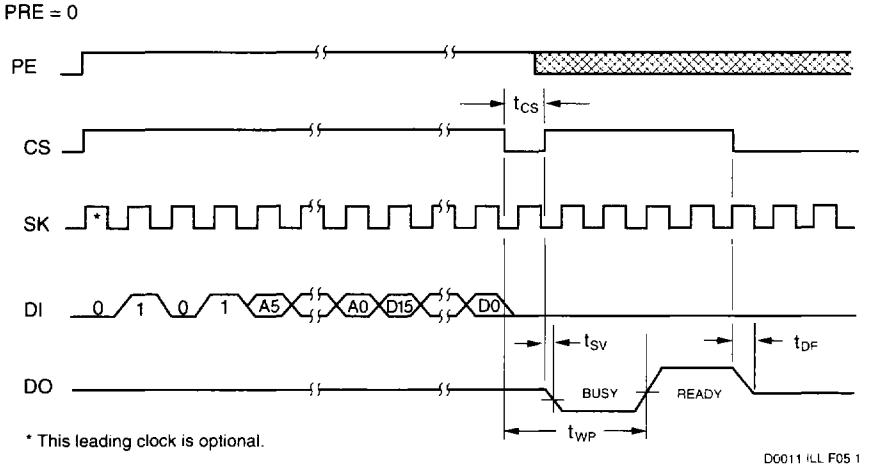

FIGURE 5. WRITE CYCLE TIMING

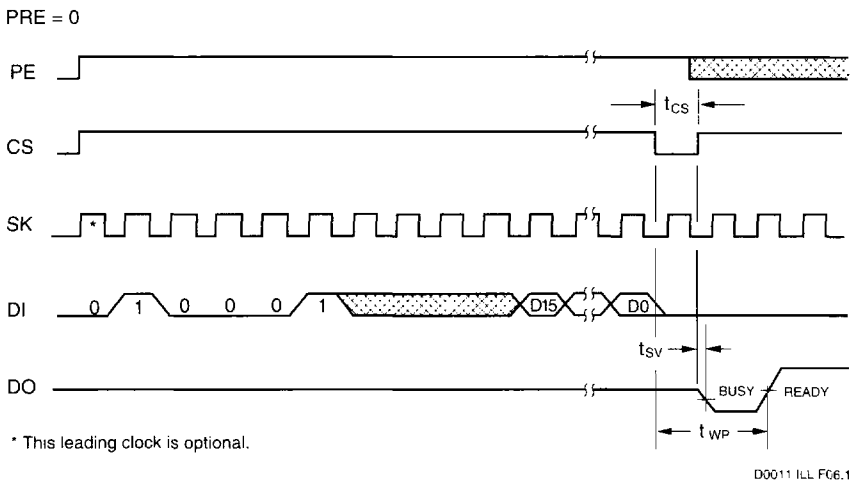

FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

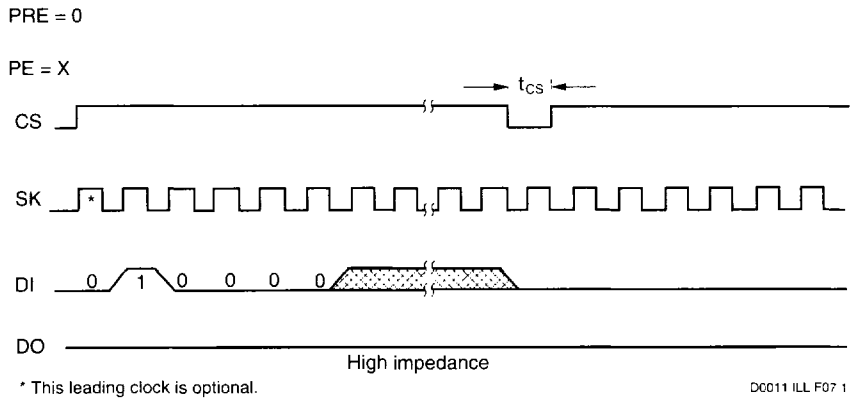

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

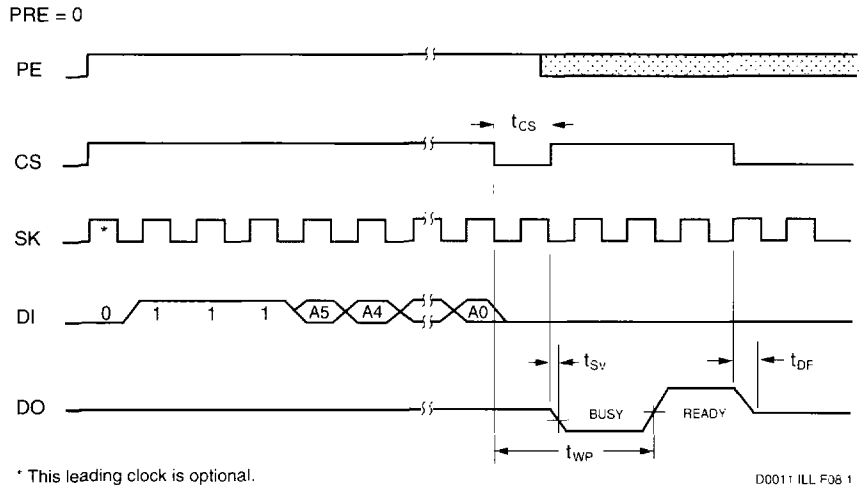

FIGURE 8. ERASE (REGISTER) CYCLE TIMING

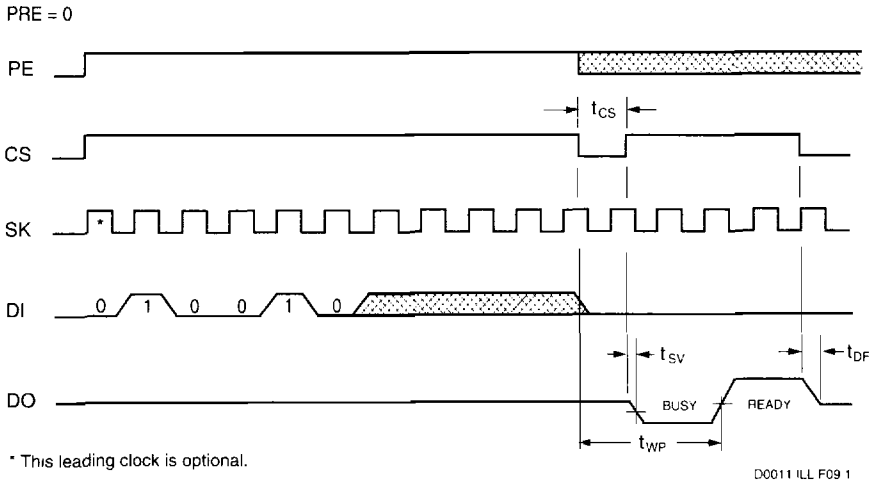

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

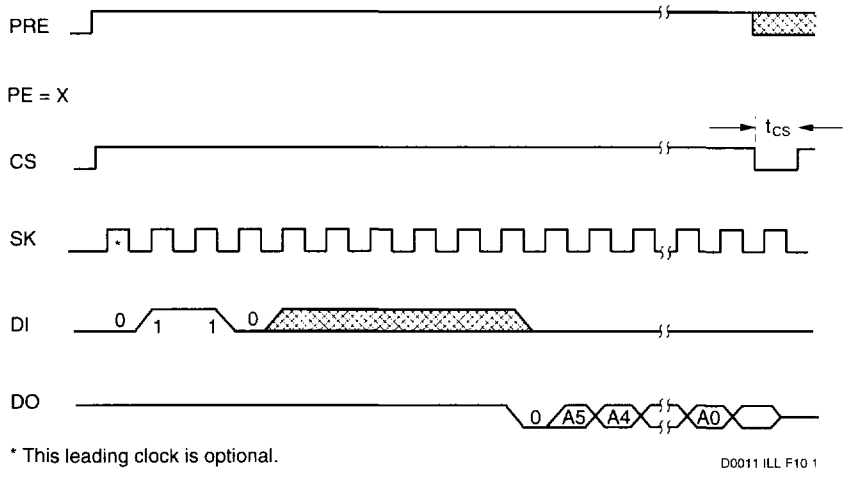

FIGURE 10. PROTECT REGISTER READ (PRREAD) CYCLE TIMING

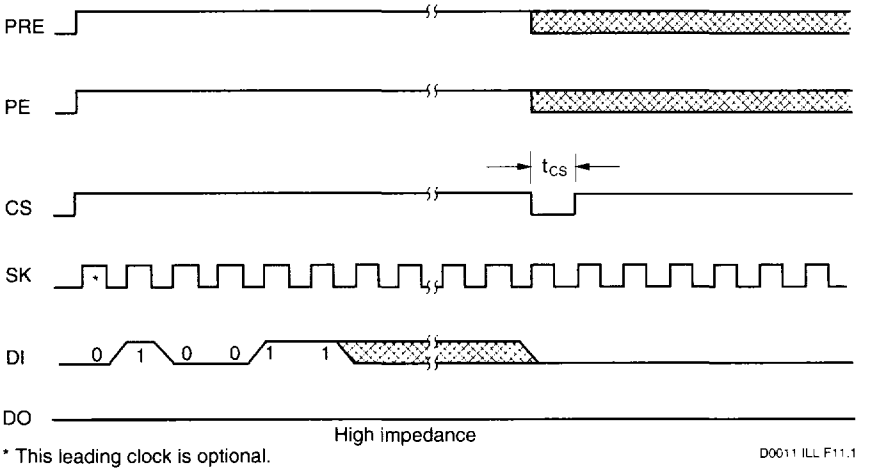

FIGURE 11. PROTECT REGISTER ENABLE (PREN) CYCLE TIMING

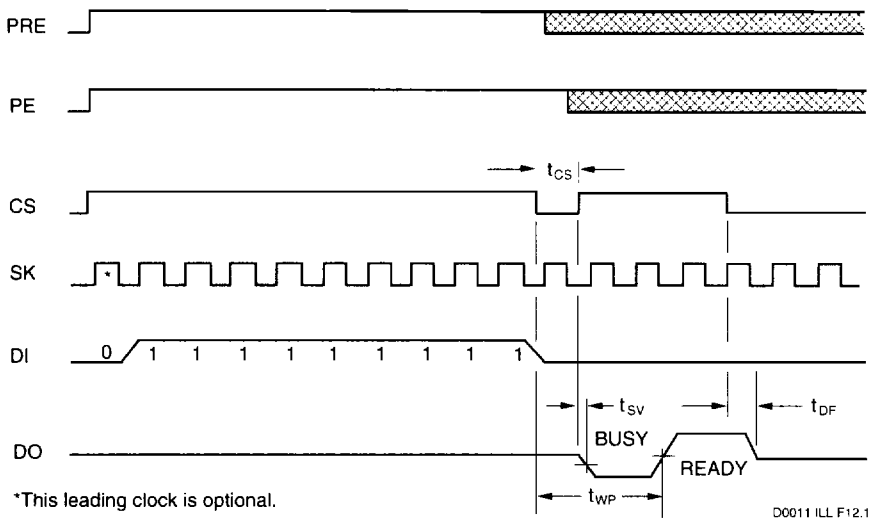

FIGURE 12. PROTECT REGISTER CLEAR (PRCLEAR) CYCLE TIMING

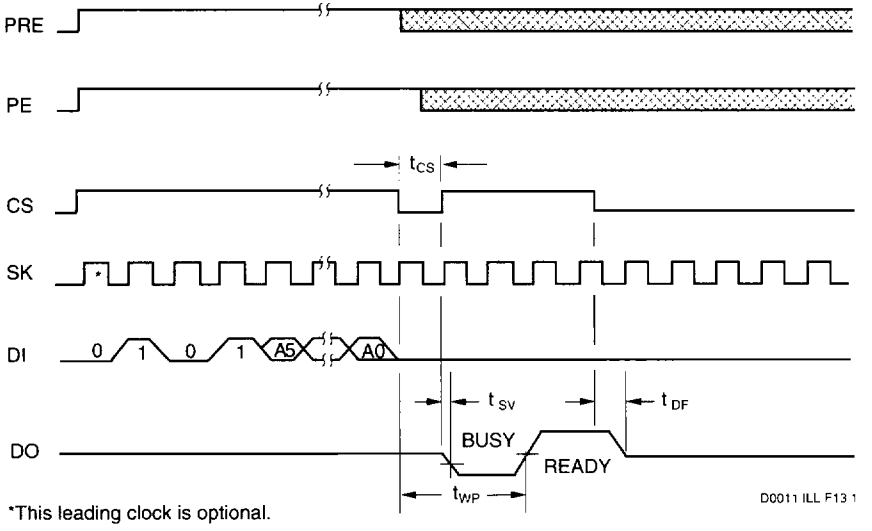

FIGURE 13. PROTECT REGISTER WRITE (PRWRITE) CYCLE TIMING

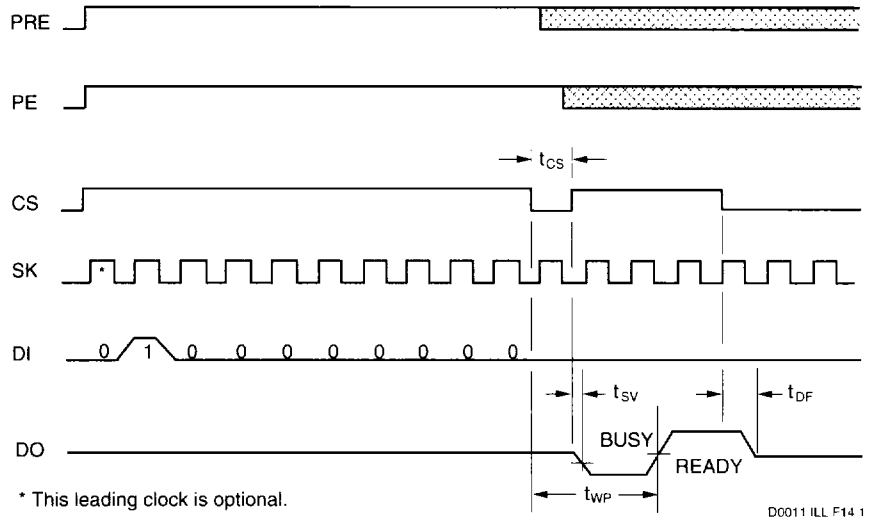

FIGURE 14. PROTECT REGISTER DISABLE (PRDS) CYCLE TIMING