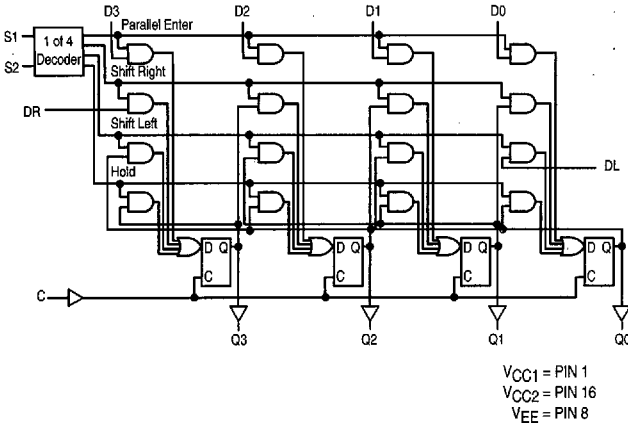


Four Bit Universal Shift Register

The MC10141 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

$P_D = 425 \text{ mW typ/pkg (No Load)}$
 $f_{\text{Shift}} = 200 \text{ MHz typ}$
 $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$

LOGIC DIAGRAM



$V_{CC1} = \text{PIN 1}$
 $V_{CC2} = \text{PIN 16}$
 $V_{EE} = \text{PIN 8}$

TRUTH TABLE

SELECT		OPERATING MODE	OUTPUTS			
S1	S2		Q_{0n+1}	Q_{1n+1}	Q_{2n+1}	Q_{3n+1}
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	Q_{1n}	Q_{2n}	Q_{3n}	DR
H	L	Shift Left*	DL	Q_{0n}	Q_{1n}	Q_{2n}
H	H	Stop Shift	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}

*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).

MC10141



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

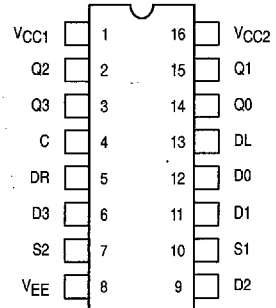


P SUFFIX
PLASTIC PACKAGE
CASE 648-08



FN SUFFIX
PLCC
CASE 775-02

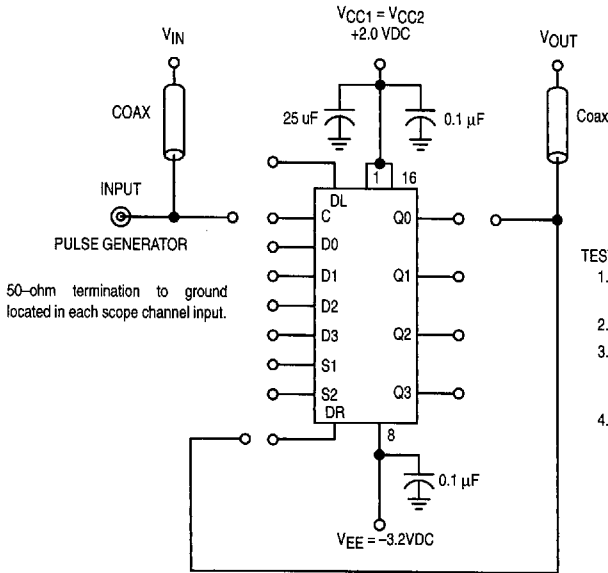
DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6-11.




SHIFT FREQUENCY TEST CIRCUIT



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

TEST PROCEDURES:

1. SET D1, D2, D3 = +0.31 VDC (LOGIC L)
D0 = +1.11 VDC (LOGIC H)
2. APPLY CLOCK PULSE  TO SET Q0 HIGH.
3. MAINTAIN CLOCK LOW.
SET S1 = +0.31 VDC (LOGIC L)
S2 = +1.11 VDC (LOGIC H)
4. TEST SHIFT FREQUENCY

3

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit	
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min		Max
Power Supply Drain Current	I_E	8		112		82	102		112	mAdc
Input Current	i_{inH}	5		350			220		220	μ Adc
		6		350			220		220	
		7		390			245		245	
		4		425			265		265	
	i_{inL}	12	0.5		0.5			0.3		μ Adc
Output Voltage Logic 1	V_{OH}	3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
Output Voltage Logic 0	V_{OL}	3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
Threshold Voltage Logic 1	V_{OHA} (Note 1.)	3	-1.080		-0.980			-0.910		Vdc
		3	-1.080		-0.980			-0.910		
		3	-1.080		-0.980			-0.910		
		3	-1.080		-0.980			-0.910		
Threshold Voltage Logic 0	V_{OLA} (Note 1.)	3		-1.655			-1.630		-1.595	Vdc
		3		-1.655			-1.630		-1.595	
		3		-1.655			-1.630		-1.595	
		3		-1.655			-1.630		-1.595	
Switching Times (50Ω Load)									ns	
Propagation Delay	t_{4+3+}	3	1.7	3.9	1.8	2.9	3.8	2.0	4.2	
Setup Time (t_{setup})	t_{12+4+}	14	2.5		2.5			2.5		
	t_{10+4+}	14	5.5		5.0			5.5		
Hold Time (t_{hold})	t_{4+12+}	14	1.5		1.5			1.5		
	Rise Time (20 to 80%)	t_{3+}	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6
Fall Time (20 to 80%)	t_{3-}	3	1.0	3.4	1.1	2.0	3.3	1.1	3.6	
Shift Frequency	f_{shift}		150		150	200		150		MHz

3

1. These tests to be performed in sequence as shown.

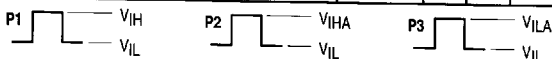


- 2. See shift frequency test circuit for test procedures.
- 3. Reset to zero before performing test.
- 4. Reset to one before performing test.

ELECTRICAL CHARACTERISTICS (continued)

© Test Temperature			TEST VOLTAGE VALUES (Volts)					P1	P2	P3	(V _{CC}) Gnd									
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmx}	V _{EE}													
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2													
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2													
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2													
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					P1	P2	P3	(V _{CC}) Gnd									
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmx}	V _{EE}													
Power Supply Drain Current	I _E	8					8				1, 16									
Input Current	I _{inH}	5	5				8				1, 16									
		6	6				8				1, 16									
		7	7				8				1, 16									
		4	4				8				1, 16									
	I _{inL}	12	4,5,6,7,9, 10,11,13	12			8				1, 16									
Output Voltage	Logic 1	V _{OH}	3	6			8	4			1, 16									
Output Voltage	Logic 0	V _{OL}	3				8	4			1, 16									
Threshold Voltage	Logic 1	V _{OHA} (Note 1.)	3			6	8	4				1, 16								
			3	6	Note 3.	7	8	4				1, 16								
			3	6	Note 3.		8		4			1, 16								
			3				8			4		1, 16								
Threshold Voltage	Logic 0	V _{OLA} (Note 1.)	3				8	4				1, 16								
			3		Note 4.	6	8	4				1, 16								
			3		Note 4.	7	8		4			1, 16								
			3	6			8			4		1, 16								
Switching Times (50Ω Load)							-3.2 V				+2.0 V									
							Propagation Delay				t ₄₊₃₊	3				8				1, 16
							Setup Time (t _{setup})				t ₁₂₊₄₊	14				8				1, 16
											t ₁₀₊₄₊	14				8				1, 16
							Hold Time (t _{hold})				t ₁₀₊₄₊	14				8				1, 16
											t ₄₊₁₂₊	14				8				1, 16
							Rise Time (20 to 80%)				t ₃₊	3				8				1, 16
Fall Time (20 to 80%)	t ₃₋	3				8				1, 16										
Shift Frequency	f _{shift}		Note 2.			8				1, 16										

1. These tests to be performed in sequence as shown.



2. See shift frequency test circuit for test procedures.

3. Reset to zero before performing test.

4. Reset to one before performing test.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.