MOTOROLA

MC74AC374
MC74ACT374

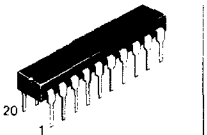
Product Preview

Octal D-Type Flip-Flop with 3-State Outputs

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The MC74AC374/74ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

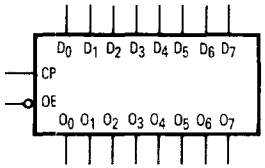
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- See MC74AC273 for Reset Version
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC574 for Broadside Pinout Version
- See MC74AC564 for Broadside Pinout Version with Inverted Outputs
- 'ACT374 Has TTL Compatible Inputs

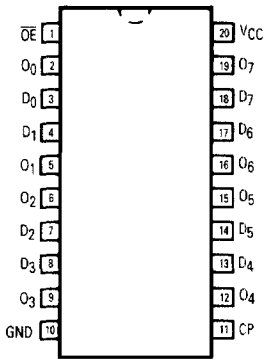


N SUFFIX
CASE 738-03
PLASTIC

DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
O_0–O_7	3-State Outputs

TRUTH TABLE

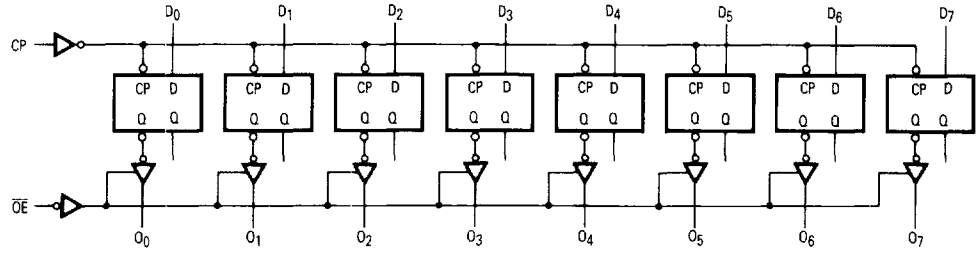
Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⎍	L	H
L	⎍	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⎍ = LOW-to-HIGH Transition

FUNCTIONAL DESCRIPTION

The MC74AC374/74ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT374)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	60 100	110 155		60 100		MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0	1.0 1.0	11 8.0	13.5 9.5	1.0 1.0	15.5 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	1.0 1.0	10 7.0	12.5 9.0	1.0 1.0	14 10	ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	9.5 7.0	11.5 8.5	1.0 1.0	13 9.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	9.0 6.5	11.5 8.5	1.0 1.0	13 9.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	10.5 8.0	12.5 1[illegible]	1.0 1.0	14.5 12.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0	5.5 4.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 0	1.0 1.5	1.0 1.5	ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 2.5	5.5 4.0	6.0 4.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	100	160		90		MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	8.5	10	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	8.0	9.5	1.0	11	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	8.0	9.5	1.0	10.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	8.0	9.0	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	8.5	11.5	1.0	12.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.0	8.5	1.0	10	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	7.0	8.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5	1.5	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	7.0	8.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	80	pF	V_{CC} = 5.0 V

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