

SN54LS266, SN74LS266 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

SDLS151 - DECEMBER 1972 - REVISED MARCH 1988

- Can Be Used as a 4-Bit Digital Comparator
- Input Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level

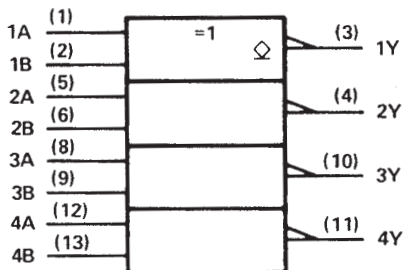
description

The 'LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

logic symbol (each gate)



logic symbol†



positive logic: $Y = \overline{A \oplus B} = AB + \overline{AB}$

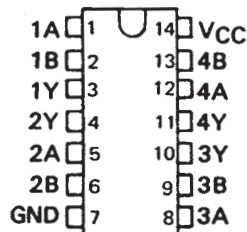
† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS266 . . . J OR W PACKAGE

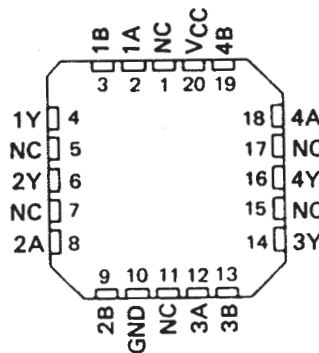
SN74LS266 . . . D OR N PACKAGE

(TOP VIEW)



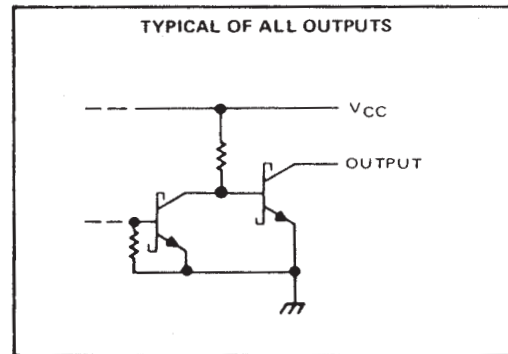
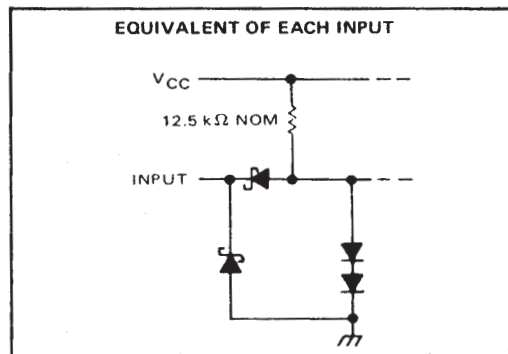
SN54LS266 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

schematic of inputs and outputs



SN54LS266, SN74LS266 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS266	-55°C to 125°C
SN74LS266	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS266			SN74LS266			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	5.5			5.5			V
Low-level output current, I_{OL}	4			8			mA
Operating free-air temperature, T_A	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS266			SN74LS266			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage					0.8			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.5			V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$	100			100			μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$	0.25 0.4			0.25 0.4			V
	$I_{OL} = 8 \text{ mA}$				0.35 0.5			
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	0.2			0.2			mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	40			40			μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.8			-0.8			mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	8 13			8 13			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER§	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 3}$	18	30	ns	
t_{PHL}							
t_{PLH}	A or B	Other input high		18	30	ns	
t_{PHL}							

§ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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SN74LS266, Quad 2-input exclusive-NOR gates with open collector outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS266	SN74LS266
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		- /8
No. of Gates	4	4
Static Current		13
tpd max (ns)		30

FEATURES

[▲Back to Top](#)

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DESCRIPTION

[▲Back to Top](#)

The 'LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

TECHNICAL DOCUMENTS

[▲Back to Top](#)

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DATASHEET

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Full datasheet in Acrobat PDF: [sn74ls266.pdf](#) (99 KB) (Updated: 03/01/1983)

APPLICATION NOTES

[▲Back to Top](#)

View Application Notes for [Digital Logic](#)

- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Designing with the SN54/74LS123 \(Rev. A\)](#) (SDLA006A - Updated: 03/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits \(SZZA026](#) - Updated: 06/20/2001)

- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS

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- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

[▲Back to Top](#)

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS266D	ACTIVE	SOP (D) 14	0 TO 70	View Contents	1KU 0.31	50	N/A*	1300 03 Oct	4 WKS			
								>10k 07 Oct				
								>10k 14 Oct				
								>10k 21 Oct				
SN74LS266DR	ACTIVE	SOP (D) 14	0 TO 70	View Contents	1KU 0.34	2500	N/A*	>10k 04 Oct	4 WKS			
								>10k 11 Oct				
								>10k 18 Oct				
SN74LS266N	ACTIVE	PDIP (N) 14	0 TO 70	View Contents	1KU 0.28	25	1000	2525 19 Sep	4 WKS	Avnet AMERICA	> 1k	BUY NOW
								19 25 Sep		DigiKey AMERICA	> 1k	BUY NOW
								>10k 30 Sep				
								>10k 04 Oct				
								>10k 07 Oct				
SN74LS266N3	OBSOLETE	PDIP (N) 14	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74LS266NSR	ACTIVE	SOP (NS) 14		View Contents	1KU 0.28	2000	N/A*	>10k 04 Oct	4 WKS			
								>10k 11 Oct				

Table Data Updated on: 9/26/2002

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