



High Speed CMOS 8 Input Multiplexers

QS54/74FCT151T
QS54/74FCT251T

QS54/74FCT2151T
QS54/74FCT2251T

FEATURES/BENEFITS

- Pin and function compatible to the 74F151/251 74FCT151/251 and 74FCT151T/251T
- CMOS power levels: <7.5 mW static
- Available in DIP, ZIP, SOIC, QSOP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 151T, 251T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, and C speed grades with 4.5 ns t_{PD} for C
- $I_{OL} = 48$ mA Com., 32 mA Mil.

FCT-T 2151T, 2251T

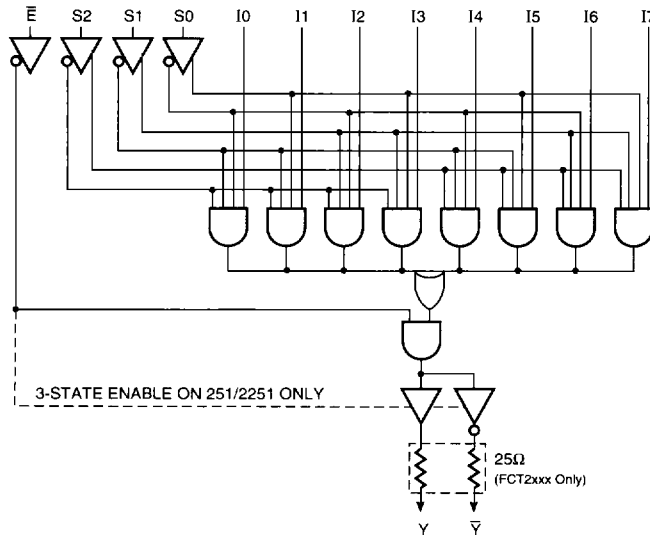
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std, A and C speed grades with 4.5 ns t_{PD} for C
- $I_{OL} = 12$ mA Com.

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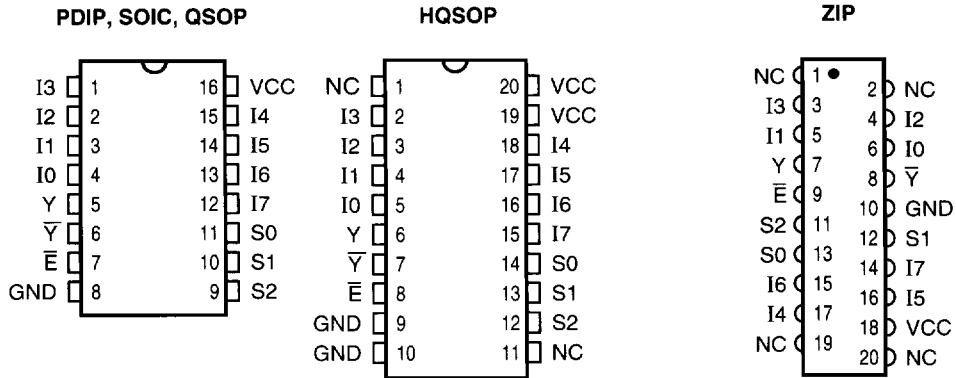
DESCRIPTION

The QSFCT151T and QSFCT251T are high-speed CMOS TTL-compatible 8-input multiplexers. The 151 has TTL outputs; the 251 has 3-state outputs. The QSFCT2151T and QSFCT2251T are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001). Outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (All Pins Top View)



Note:
Available in both 150 mil wide SOIC (package code S1)
and 300 mil SOIC (package code S0).

PIN DESCRIPTION

Name	I/O	Description
I7-I0	I	Data In
S2-S0	I	Select
E-bar	I	Enable
Y, Y-bar	O	Data Out

FUNCTION TABLE

E-bar	Select			151, 2151		251, 2251		Function
	S2	S1	S0	Y	Y-bar	Y	Y-bar	
H	X	X	X	L	H	HI-Z	HI-Z	Disable
L	L	L	L	I0	I0-bar	I0	I0-bar	S2-0 = 0
L	L	L	H	I1	I1-bar	I1	I1-bar	S2-0 = 1
L	L	H	L	I2	I2-bar	I2	I2-bar	S2-0 = 2
L	L	H	H	I3	I3-bar	I3	I3-bar	S2-0 = 3
L	H	L	L	I4	I4-bar	I4	I4-bar	S2-0 = 4
L	H	L	H	I5	I5-bar	I5	I5-bar	S2-0 = 5
L	H	H	L	I6	I6-bar	I6	I6-bar	S2-0 = 6
L	H	H	H	I7	I7-bar	I7	I7-bar	S2-0 = 7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_{OUT}	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20 mA
DC Output Diode Current with $V_{OUT} < 0$	-50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1$ MHz, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-3, 10, 11, 13-15	4	4	5	7	pF
-	6	6	7	9	pF
4-7, 9, 12	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, $\text{freq} = 0$ ⁽²⁾	—	2.0	mA
Q_{CCd}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$, Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC} ^(3,4)	—	0.25	mA/ MHz

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$).
- For flip-flops, Q_{CCd} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_C can be computed using the above parameters as explained in the Technical Overview section.

QSFCT151T, 251T, 2151T, 2251T

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
I_{IH} I_{IL}	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	μA
I_{OZ}	Off-State Output Current (Hi-Z)(251, 2251)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	μA
I_{OS}	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
I_{OR}	Current Drive (FCT2XXX)	$V_{CC} = \text{Max.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}, I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX- 25 Ω)	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX- 25 Ω)	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— 20	25 28	— 40	Ω

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

QSFCT151T, 251T, 2151T, 2251T

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Military T_A = -55°C to 125°C, V_{CC} = 5.0V ± 10%

C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description ⁽¹⁾		151 251 2151 2251		151A 251A 2151A 2251A		151C 251C 2151C 2251C		Unit
			Min	Max	Min	Max	Min	Max	
t _{1Y}	Propagation Delay In to Y or \bar{Y} , 151/251	Com	1.5	7	1.5	5.2	1.5	4.5	ns
		Mil	1.5	8	1.5	5.8	1.5	5.2	
t _{1Y}	Propagation Delay In to Y or \bar{Y} , 2151/2251	Com	1.5	7	1.5	5.2	1.5	4.5	ns
		Mil	1.5	8	1.5	5.8	1.5	5.2	
t _{SY}	Propagation Delay S _n to Y or \bar{Y} , 151/251	Com	1.5	9	1.5	6.6	1.5	5.9	ns
		Mil	1.5	9.5	1.5	7.4	1.5	6.5	
t _{SY}	Propagation Delay In to Y or \bar{Y} , 2151/2251	Com	1.5	9	1.5	6.6	1.5	5.9	ns
		Mil	1.5	9.5	1.5	7.4	1.5	6.5	
t _{OE\bar{H}} t _{OEL}	Output Enable Time \bar{E} to Y _i , 151	Com	1.5	7	1.5	5.2	1.5	4.5	ns
		Mil	1.5	8	1.5	5.8	1.5	5.2	
t _{OE\bar{H}} t _{OEL}	Output Enable Time \bar{E} to Y _i , 2151	Com	1.5	7	1.5	5.2	1.5	4.5	ns
		Mil	1.5	8	1.5	5.8	1.5	5.2	
t _{PZH} t _{PZL}	Output Enable Time \bar{E} to Y _i , 251	Com	1.5	9	1.5	6.0	1.5	5.0	ns
		Mil	1.5	10	1.5	6.4	1.5	5.5	
t _{PZH} t _{PZL}	Output Enable Time \bar{E} to Y _i , 2251	Com	1.5	9	1.5	6.0	1.5	5.0	ns
		Mil	1.5	10	1.5	6.4	1.5	5.5	
t _{PHZ} t _{PLZ}	Output Disable Time ⁽²⁾ \bar{E} to Y _i , 251/2251	Com	1.5	7	1.5	6	1.5	5.0	ns
		Mil	1.5	7	1.5	6.3	1.5	5.5	

Notes:

1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

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