MOTOROLA

Military 54F151

8-Input Data Selector/Multiplexer

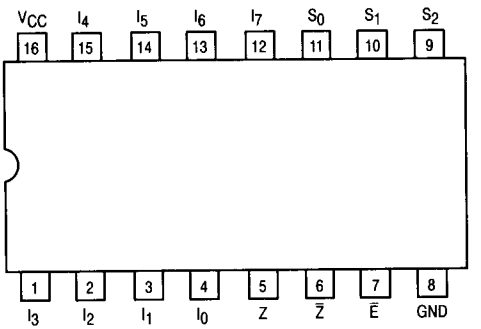
ELECTRICALLY TESTED PER:
MIL-M-38510/33901

The 54F151 is a high-speed 8-input digital multiplexer. It provides in one package, the ability to select one line of data from up to eight sources. The 'F151 can be used as a universal function generator to generate any logic function of four variables. Both asserted and negated outputs are provided.

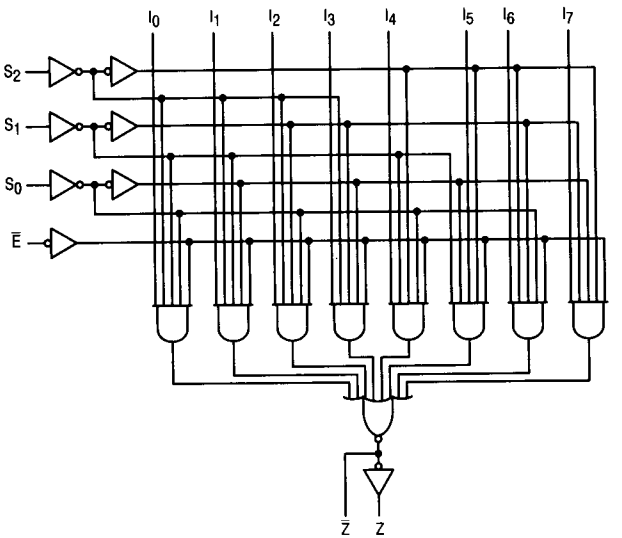
The 'F151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of the three Select inputs, S_0, S_1, S_2. The Enable input ($\overline{E}$) is active LOW. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

CONNECTION DIAGRAM



LOGIC DIAGRAM



AVAILABLE AS:

1) JAN: JM38510/33901BXA
2) SMD: N/A
3) 883: 54F151/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
I_3	1	1	2	V_{CC}
I_2	2	2	3	V_{CC}
I_1	3	3	4	V_{CC}
I_0	4	4	5	V_{CC}
Z	5	5	7	OPEN
$\overline{Z}$	6	6	8	OPEN
$\overline{E}$	7	7	9	V_{CC}
GND	8	8	10	GND
S_2	9	9	12	V_{CC}
S_1	10	10	13	V_{CC}
S_0	11	11	14	V_{CC}
I_7	12	12	15	V_{CC}
I_6	13	13	17	V_{CC}
I_5	14	14	18	V_{CC}
I_4	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

Table 1

Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

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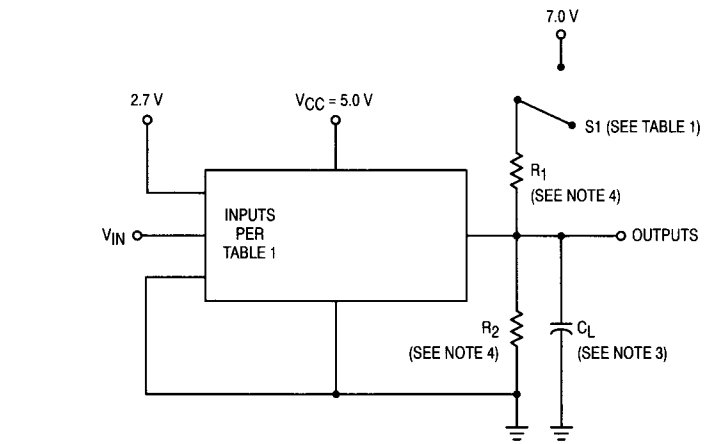
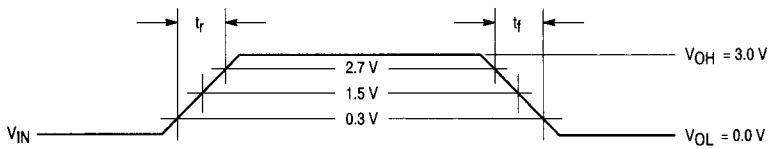
TRUTH TABLE					
Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

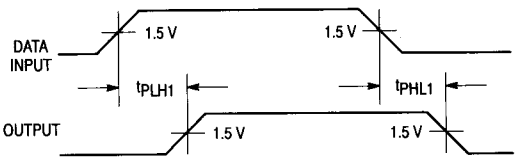
AC TEST CIRCUIT

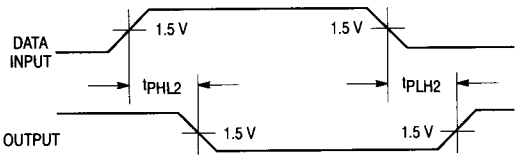


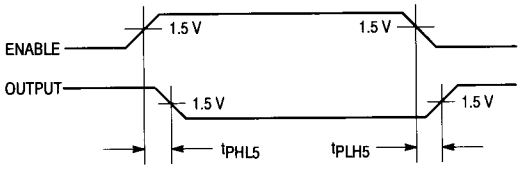


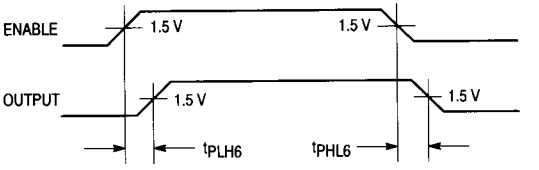
REFERENCE NOTES ON PAGE 4-58

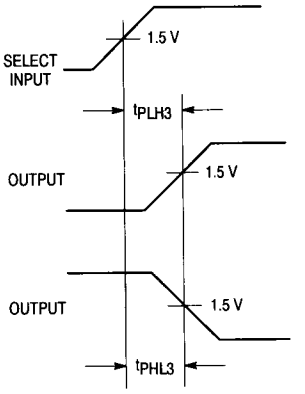
WAVEFORMS

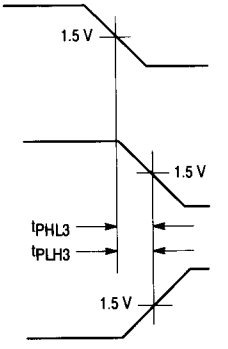


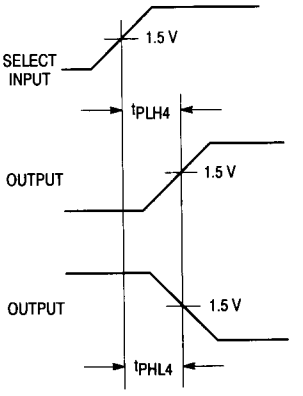


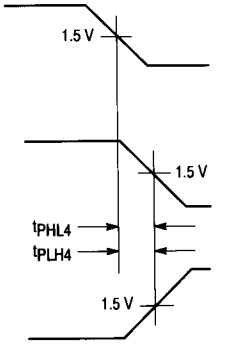












NOTES:

1. Input pulse and has the following characteristics: PRR ≤ 1.0 MHz, $t_r = t_f \leq 2.5$ ns, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. $R_1 = R_2 = 499\ \Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IL} = 0.8 V, S = 0.8 V or 2.0 V, $\overline{E}$ = 2.0 V or 0.8 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IH} = 2.0 V, S = 0.8 V or 2.0 V, $\overline{E}$ = 0.8 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{E}$ = 4.5 V or (2.7 V), S = 0 V, 4.5 V or (2.7 V).
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open, $\overline{E}$ = 4.5 V or (7.0 V), S = 0 V, 4.5 V or (7.0 V).
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open, $\overline{E}$ = 0 V or (0.5 V), S = 4.5 V, 0 V or (0.5 V).
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, other inputs are open, S = 0 V, V_{IN} = 5.5 V, V_{OUT} = 2.5 V, $\overline{E}$ = 5.5 V or 0 V.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, all other inputs are open, V_{OUT} = 0 V, S = 0 V, $\overline{E}$ = 0 V.
I_{CC}	Power Supply Current		21		21		21	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (all inputs)
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**) V_{CC} = 5.5 V, V_{IL} = 0.5 V, and V_{IH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output I_n to Z	3.7	7.0	3.5	9.0	3.5	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output I_n to Z	3.0	6.5	2.5	8.5	2.5	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output I_n to $\overline{Z}$	1.5	4.0	1.5	6.0	1.5	6.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output I_n to $\overline{Z}$	3.0	6.5	2.5	7.5	2.5	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output S_n to Z	4.0	9.0	4.0	9.5	4.0	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output S_n to Z	4.5	13	4.5	13.5	4.5	13.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output S_n to $\overline{Z}$	3.2	7.5	3.0	8.0	3.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output S_n to $\overline{Z}$	4.0	9.0	3.5	11.5	3.5	11.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL5}	Propagation Delay /Data-Output $\overline{E}$ to Z	3.5	7.0	3.0	8.0	3.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH5}	Propagation Delay /Data-Output $\overline{E}$ to Z	5.0	9.5	4.0	12	4.0	12	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL6}	Propagation Delay /Data-Output $\overline{E}$ to $\overline{Z}$	3.0	6.0	2.5	6.5	2.5	6.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH6}	Propagation Delay /Data-Output $\overline{E}$ to $\overline{Z}$	3.0	6.1	3.0	7.5	3.0	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.