



3.3V CMOS DUAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

**IDT74ALVC74
ADVANCE
INFORMATION**

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP and 0.65mm pitch TSSOP packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ± 0.2V
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVC74:

- High Output Drivers: ±24mA
- Suitable for heavy loads

DESCRIPTION:

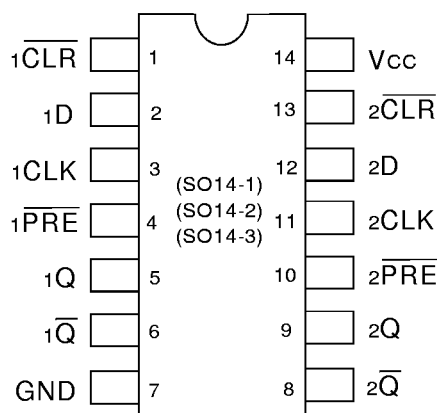
This dual positive-edge-triggered D-type flip-flop is built using advanced dual metal CMOS technology. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The ALVC74 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

PIN CONFIGURATION

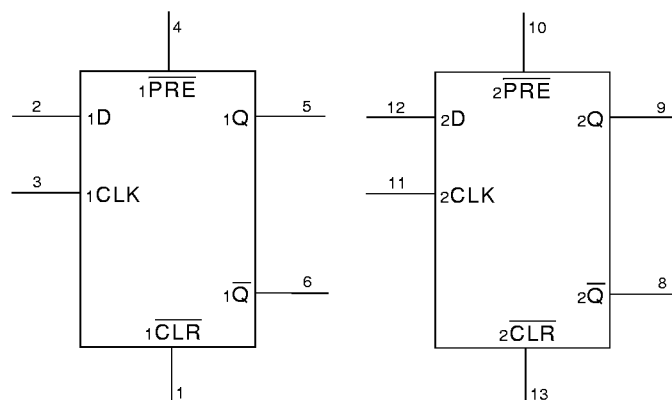


SOIC/SSOP/TSSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xCLK	Clock Inputs
xCLR	Clear Inputs
xPRE	Preset Inputs
xD	Data Inputs
xQ, xQ [̄]	Data Outputs

LOGIC SYMBOLS



EXTENDED COMMERCIAL TEMPERATURE RANGE

MARCH 1999

FUNCTION TABLE (1)

Inputs				Outputs	
\overline{xPRE}	\overline{xCLR}	$xCLK$	xD	xQ	\overline{xQ}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽²⁾	H ⁽²⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀ ⁽³⁾	$\overline{Q_0}$ ⁽⁴⁾

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- This configuration is unstable; that is, it does not persist when \overline{PRE} or \overline{CLR} returns to its inactive (HIGH) level.
- Q₀ = Level of Q before the indicated steady-state input conditions were established.
- $\overline{Q_0}$ = Complement of Q₀ or level of $\overline{Q_0}$ before the indicated steady-state input conditions were established.

ABSOLUTE MAXIMUM RATING⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	± 100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

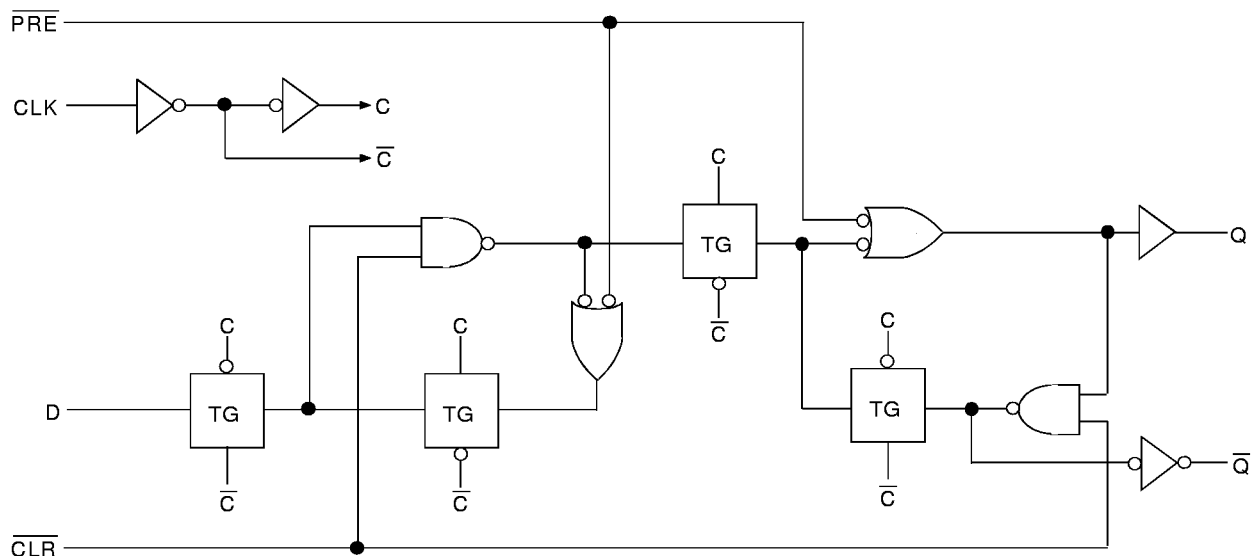
Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTIONAL BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	± 5	
IoZH	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA
IoZL			V _O = GND	—	—	± 10	
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = 3.6V		—	0.1	10	μA
I _{CC} H		V _{IN} = GND or V _{CC}					
I _{CC} Z							
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

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NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = -24mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Vcc = 2.5V ± 0.2V	Vcc = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per flip-flop	CL = 0pF, f = 10Mhz			pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fMAX								MHz
tPLH tPHL	Propagation Delay xCLK to xQ or x \bar{Q}		6		5		3.8	ns
tPLH tPHL	Propagation Delay xPRE or xCLR to xQ or x \bar{Q}		6.2		5.2		4	ns
tw	Pulse Duration, xPRE or xCLR LOW	3.3		3.3		3.3		ns
tw	Pulse Duration, xCLK HIGH or LOW	3.3		3.3		3.3		ns
tsu	Setup Time, data before xCLK \uparrow	3		3		3		ns
tsu	Setup Time, xPRE or xCLR inactive	2		2		2		ns
tH	Hold Time, data after xCLK \uparrow	1		1		0		ns

NOTE:

1. See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

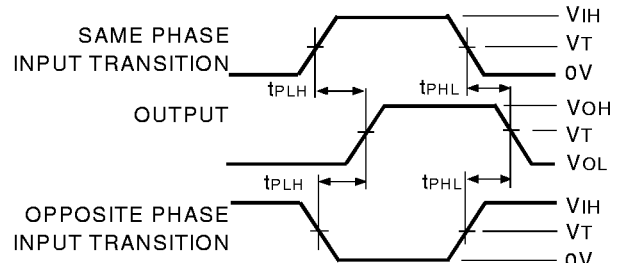
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V ± 0.3V	V _{CC} (1) = 2.7V	V _{CC} (2)= 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

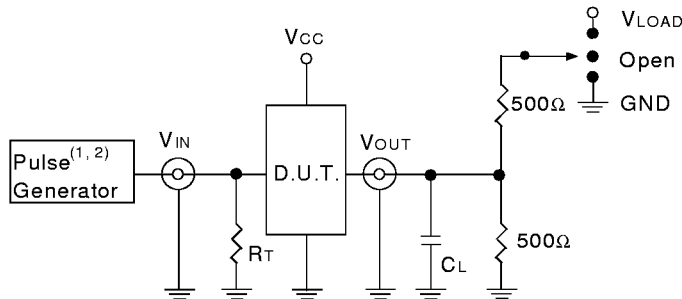
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PROPAGATION DELAY



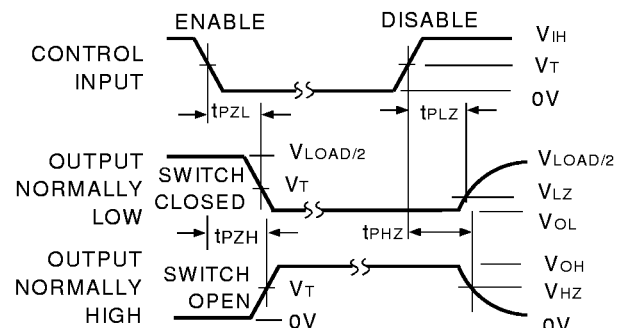
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TEST CIRCUITS FOR ALL OUTPUTS



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ENABLE AND DISABLE TIMES



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NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
 R_T= Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

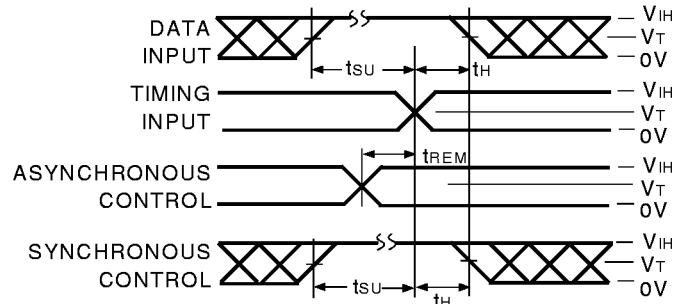
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain	V _{LOAD}
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

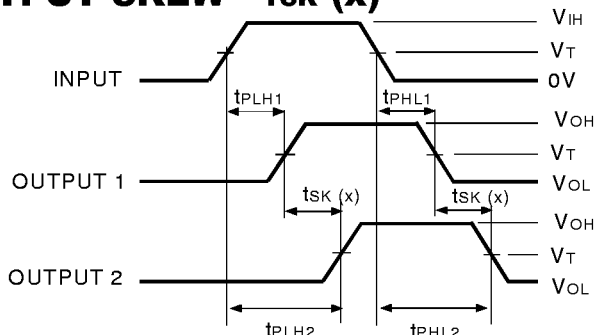
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SET-UP, HOLD, AND RELEASE TIMES



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OUTPUT SKEW - t_{SK} (x)



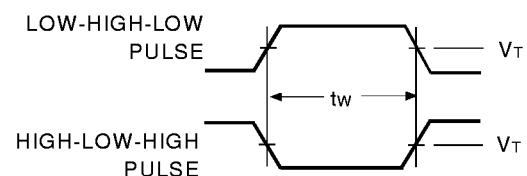
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

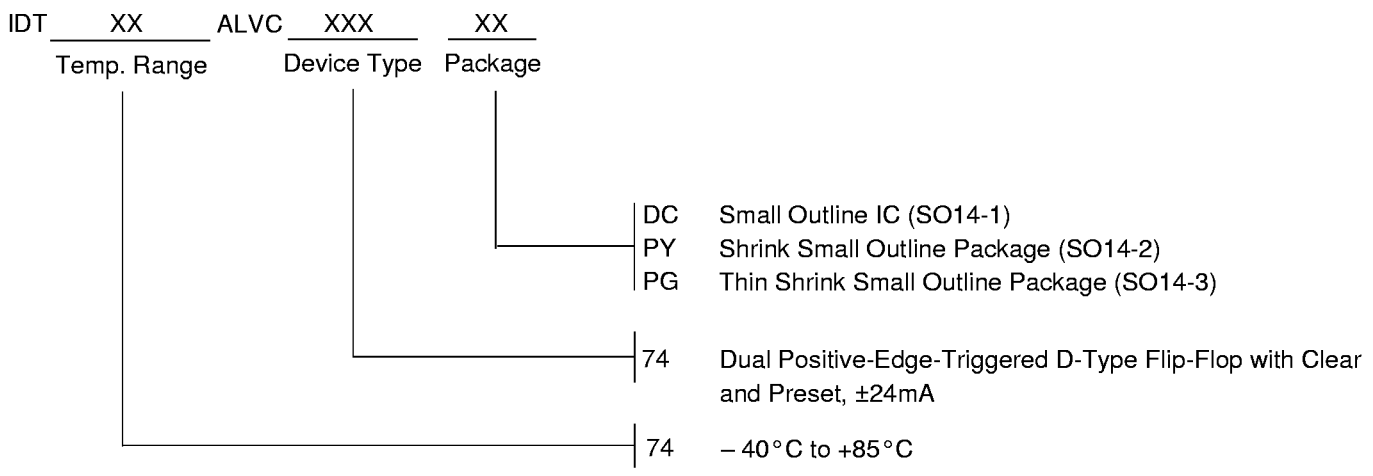
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PULSE WIDTH



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ORDERING INFORMATION



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