

M5M51008AP,FP,VP,RV-70L,-85L,-10L,-12L,-70LL,-85LL,-10LL,-12LL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008AP,FP,VP,RV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51008AVP,RV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD). Two types of devices are available. M5M51008AVP (normal lead vend type package),M5M51008ARV (reverse lead vend type package). Using both types of devices,it becomes very easy to design a printed circuit board.

FEATURES

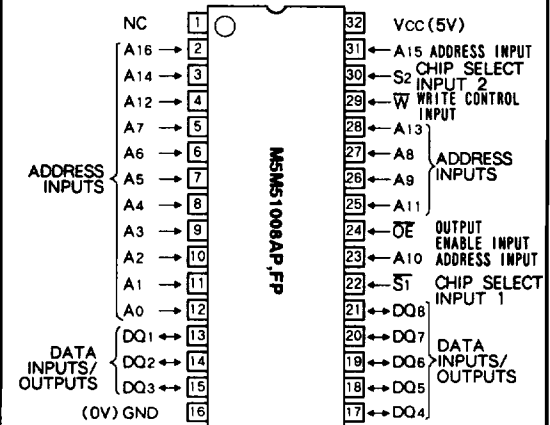
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51008AP, FP, VP, RV-70L	70ns	15mA (1MHz)	100 μ A (V _{CC} = 5.5V)
M5M51008AP, FP, VP, RV-85L	85ns		
M5M51008AP, FP, VP, RV-10L	100ns		
M5M51008AP, FP, VP, RV-12L	120ns		
M5M51008AP, FP, VP, RV-70LL	70ns	20 μ A (V _{CC} = 5.5V)	0.3 μ A (V _{CC} = 3.0V, typ)
M5M51008AP, FP, VP, RV-85LL	85ns		
M5M51008AP, FP, VP, RV-10LL	100ns		
M5M51008AP, FP, VP, RV-12LL	120ns		

- Single +5V power supply
- Low stand-by current 0.3 μ A (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S1}, \overline{S2}$
- Data hold on +2v power supply
- Three-state outputs : OR-tie capability
- \overline{OE} prevents data contention in the I/O bus
- Common data I/O
- Package M5M51008AP 32 pin 600mil DIP
M5M51008AFP 32 pin 525 mil SOP
M5M51008AVP, RV 32pin 8 x 20mm² TSOP

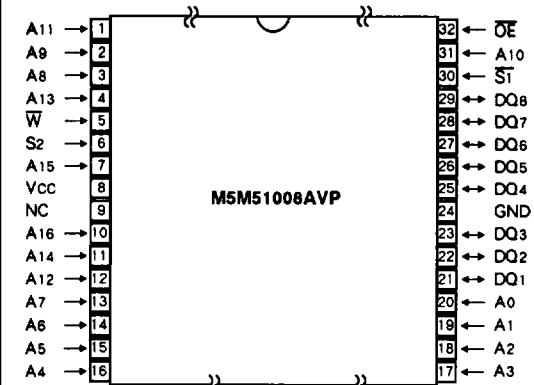
APPLICATION

Small capacity memory units

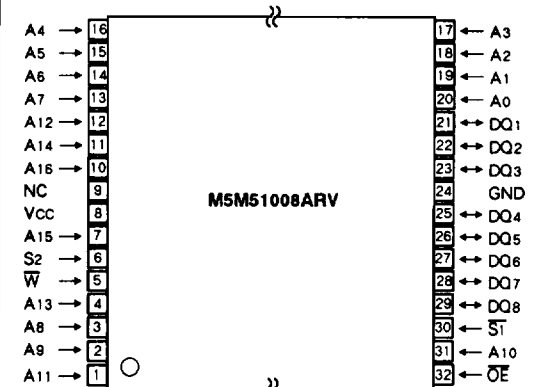
PIN CONFIGURATION (TOP VIEW)



Outline 32P4 (P)
32P2M-A (FP)



Outline 32P3H-E



Outline 32P3H-F

NC : NO CONNECTION

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FUNCTION

The operation mode of the M5M51008AP,FP,VP,RV are determined by a combination of the device control inputs $\overline{S1}$, $S2$, \overline{W} and \overline{OE} . Each mode is summarized in the function table.

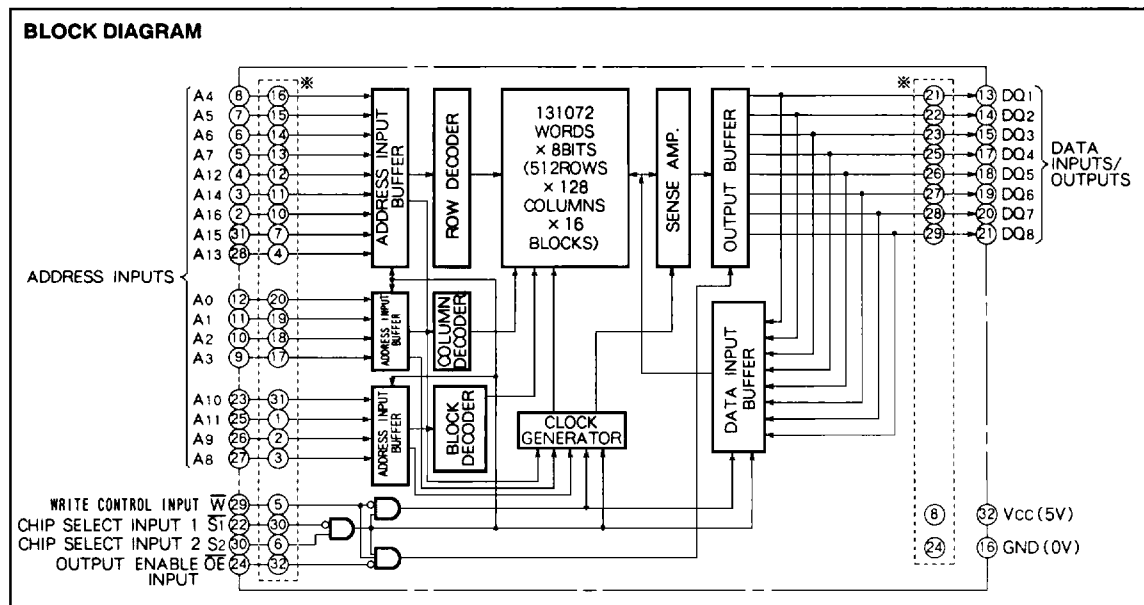
A write cycle is executed whenever the low level \overline{W} overlaps with the low level $\overline{S1}$ and the high level $S2$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , $\overline{S1}$ or $S2$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{S1}$ and $S2$ are in an active state ($\overline{S1} = L, S2 = H$).

When setting $\overline{S1}$ at a high level or $S2$ at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output state is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S1}$ and $S2$. The power supply current is reduced as low as the stand-by current which is specified as I_{cc3} or I_{cc4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	$S2$	\overline{W}	\overline{OE}	Mode	DQ	I_{cc}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	D_{in}	Active
L	H	H	L	Read	D_{out}	Active
L	H	H	H		High-impedance	Active



* Pin numbers inside dotted line show those of TSOP.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	- 0.3~7	V
V _i	Input voltage		- 0.3*~V _{cc} + 0.3	V
V _o	Output voltage		0~V _{cc}	V
P _d	Power dissipation	T _a = 25°C	700	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		- 65~150	°C

* - 3.0V in case of AC (Pulse width ≤ 50ns)

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{cc} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{cc} +0.3	V
V _{IL}	Low-level input voltage		- 0.3*		0.8	V
V _{OH}	High-level output voltage	I _{OH} = - 1mA	2.4			V
		I _{OH} = - 0.1mA	V _{cc} -0.5			
V _{OL}	Low-level output voltage	I _{OL} = 2mA			0.4	V
I _i	Input leakage current	V _i = 0~V _{cc}			± 1	μA
I _o	Output leakage current	S ₁ = V _{IH} or S ₂ = V _{IL} or OE = V _{IH} , V _{i/o} = 0~V _{cc}			± 1	μA
I _{cc1}	Active supply current (AC, MOS level)	S ₁ ≤ 0.2V, S ₂ ≥ V _{cc} - 0.2V Other inputs ≤ 0.2V or ≥ V _{cc} - 0.2V Output-open (duty 100%)	Min cycle	38	70	mA
			1MHz	5	15	
I _{cc2}	Active supply current (AC, TTL level)	S ₁ = V _{IL} , S ₂ = V _{IH} , Other inputs = V _{IH} or V _{IL} Output-open (duty 100%)	Min cycle	40	70	mA
			1MHz	7	15	
I _{cc3}	Stand-by current	1) S ₂ ≤ 0.2V, other inputs = 0~V _{cc} 2) S ₁ ≥ V _{cc} - 0.2V, S ₂ ≥ V _{cc} - 0.2V, Other inputs = 0~V _{cc}	-L		100	μA
			-LL	1.0	20	
I _{cc4}	Stand-by current	S ₁ = V _{IH} or S ₂ = V _{IL} Other inputs = 0~V _{cc}			3	mA

* - 3.0V in case of AC(Pulse width ≤ 50ns)

CAPACITANCE (T_a = 0~70°C, V_{cc} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _i	Input capacitance	V _i = GND, V _i = 25mV _{rms} , f = 1MHz			6	pF
C _o	Output capacitance	V _o = GND, V _o = 25mV _{rms} , f = 1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark)
2: Typical value is V_{cc} = 5V, T_a = 25°C

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AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level..... VIH = 2.4V, VIL = 0.6V
 Input rise and fall time.....5ns
 Reference level..... VOH = VOL = 1.5V
 Transition is measured ± 500mV from steady state voltage.(for ten, tdis)
 Output loads.....Fig. 1, CL = 100pF (P, FP, VP, RV-85L, -10L, -12L, -85LL, -10LL, -12LL)
 CL = 30pF (P, FP, VP, RV-70L, -70LL)
 CL = 5pF (for ten, tdis)

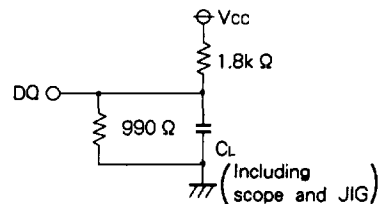


Fig. 1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits								Unit
		M5M51008AP, FP, VP, RV-70L, -70LL		M5M51008AP, FP, VP, RV-85L, -85LL		M5M51008AP, FP, VP, RV-10L, -10LL		M5M51008AP, FP, VP, RV-12L, -12LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCR	Read cycle time	70		85		100		120		ns
ta(A)	Address access time		70		85		100		120	ns
ta(S1)	Chip select 1 access time		70		85		100		120	ns
ta(S2)	Chip select 2 access time		70		85		100		120	ns
ta(OE)	Output enable access time		35		45		50		60	ns
tdis(S1)	Output disable time after S1 high		25		30		35		40	ns
tdis(S2)	Output disable time after S2 low		25		30		35		40	ns
tdis(OE)	Output disable time after OE high		25		30		35		40	ns
ten(S1)	Output enable time after S1 low	10		10		10		10		ns
ten(S2)	Output enable time after S2 high	10		10		10		10		ns
ten(OE)	Output enable time after OE low	5		5		5		5		ns
tv(A)	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

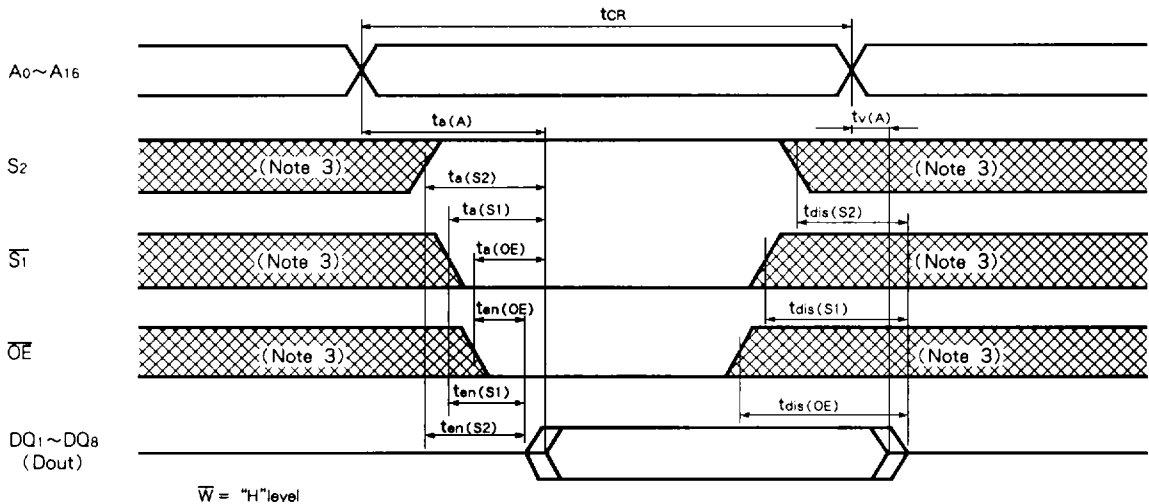
Symbol	Parameter	Limits								Unit
		M5M51008AP, FP, VP, RV-70L, -70LL		M5M51008AP, FP, VP, RV-85L, -85LL		M5M51008AP, FP, VP, RV-10L, -10LL		M5M51008AP, FP, VP, RV-12L, -12LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
tcw	Write cycle time	70		85		100		120		ns
tw(W)	Write pulse width	55		65		75		85		ns
tsu(A)	Address set up time	0		0		0		0		ns
tsu(A-WH)	Address set up time with respect to W high	65		75		85		100		ns
tsu(S1)	Chip select 1 set up time	65		75		85		100		ns
tsu(S2)	Chip select 2 set up time	65		75		85		100		ns
tsu(D)	Data set up time	30		35		40		45		ns
th(D)	Data hold time	0		0		0		0		ns
trec(W)	Write recovery time	0		0		0		0		ns
tdis(W)	Output disable time from W low		25		30		35		40	ns
tdis(OE)	Output disable time from OE high		25		30		35		40	ns
ten(W)	Output enable time from W high	5		5		5		5		ns
ten(OE)	Output enable time from OE low	5		5		5		5		ns

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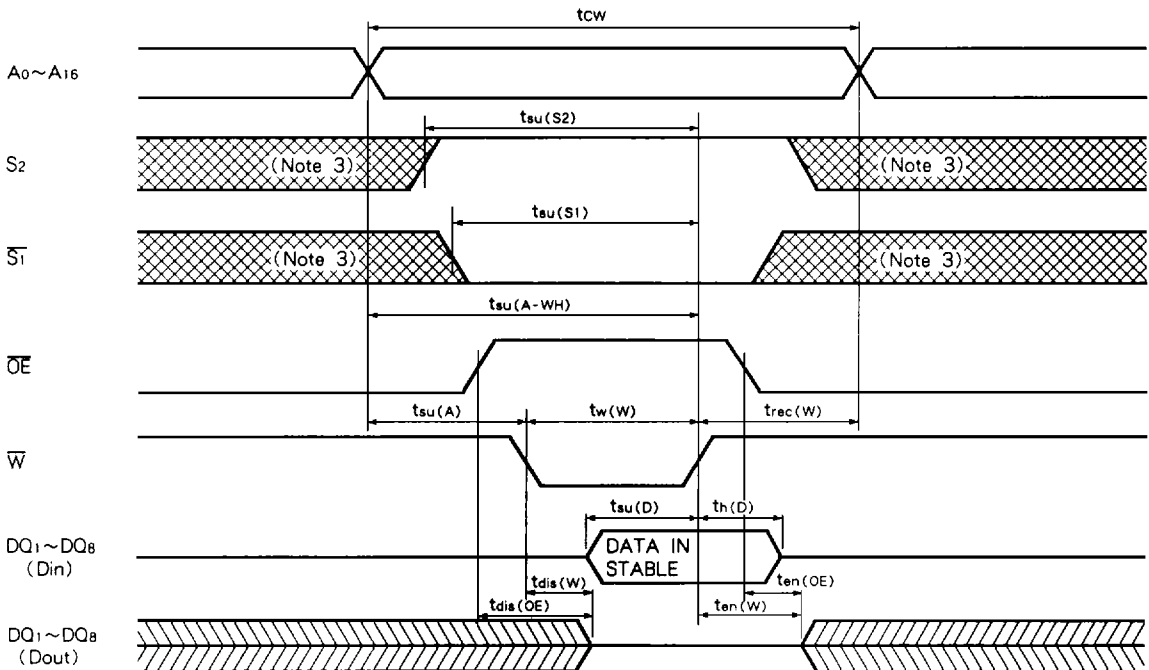
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(4) TIMING DIAGRAMS

Read cycle



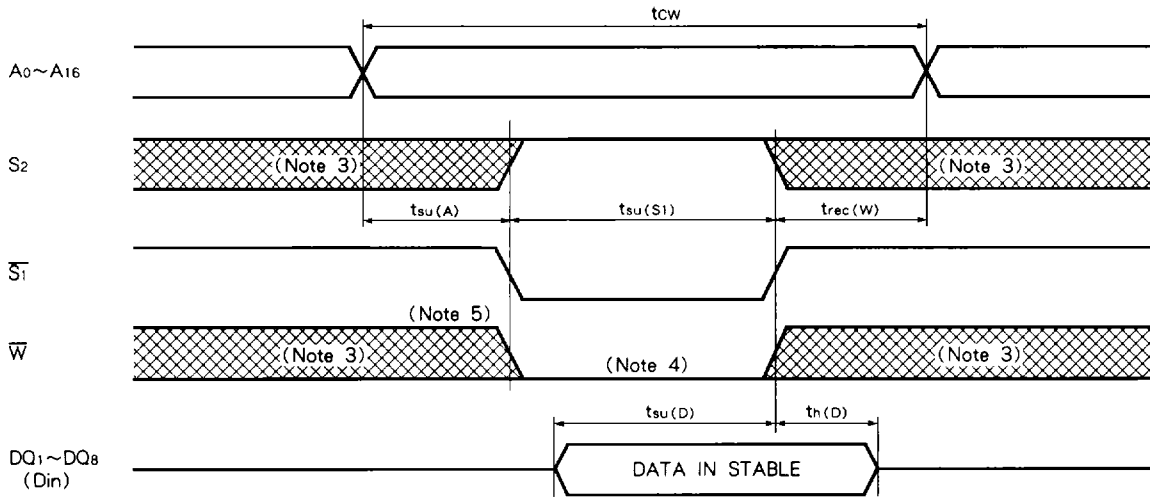
Write cycle (\overline{W} control mode)



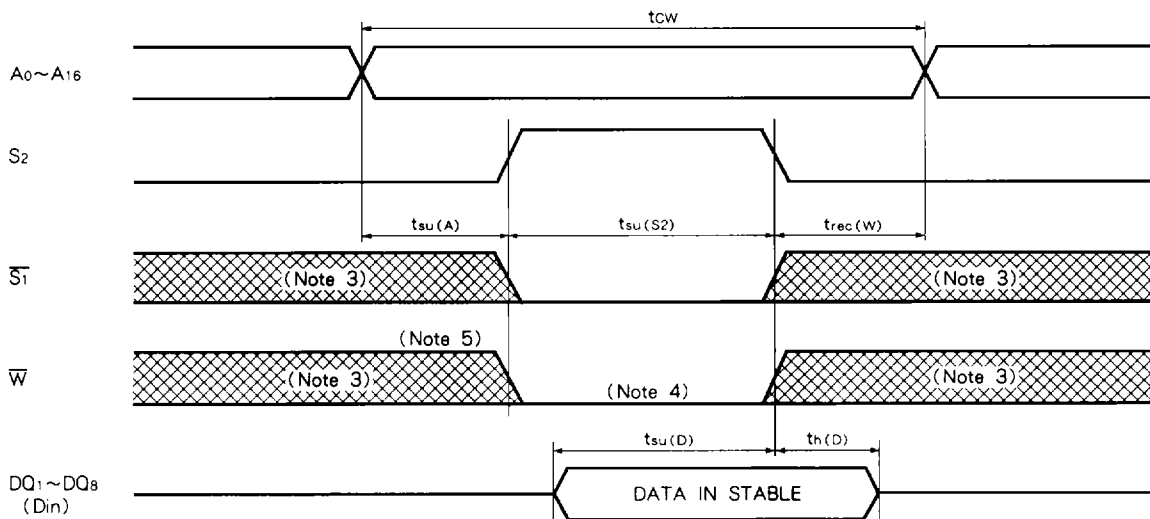
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Write cycle ($\overline{S1}$ control mode)



Write cycle (S_2 control mode)



Note 3: Hatching indicates the state is "don't care".

4: Writing is executed while S_2 high overlaps $\overline{S1}$ and \overline{W} low.

5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of S_2 , the outputs are maintained in the high impedance state.

6: Don't apply inverted phase signal externally when DQ pin is output mode.

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POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V _{CC(PD)}	Power down supply voltage		2			V	
V _{I(S1)}	Chip select input $\overline{S1}$	2.2V ≤ V _{CC(PD)}	2.2			V	
		2V ≤ V _{CC(PD)} ≤ 2.2V		V _{CC(PD)}			
V _{I(S2)}	Chip select input S ₂	4.5V ≤ V _{CC(PD)}			0.8	V	
		V _{CC(PD)} < 4.5V			0.2		
I _{CC(PD)}	Power down supply current	V _{CC} = 3V 1) S ₂ ≤ 0.2V, other inputs = 0~3V 2) $\overline{S1} \geq V_{CC} - 0.2V$, S ₂ ≥ V _{CC} - 0.2V, other inputs = 0~3V	-L			50	μA
			-LL		0.3	10 (note 7)	

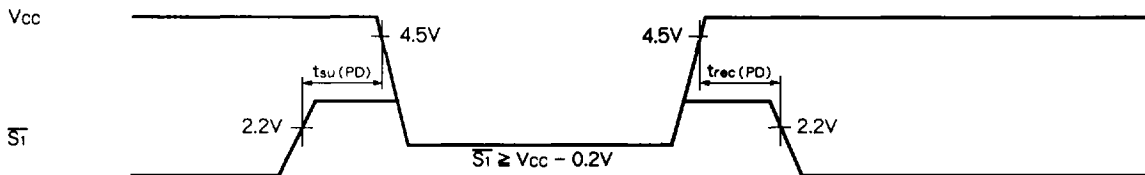
Note 7 : I_{CC(PD)} = 1 μA in case of Ta = 25°C

TIMING REQUIREMENTS (Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su(PD)}	Power down set up time		0			ns
t _{rec(PD)}	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS

$\overline{S1}$ control mode



S2 control mode

