To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

HD151TS201AT

Mother Board Clock Generator for Intel P4 Chipset Banias and Dothan processor / ODEM and MONTARA–GM chip set

REJ03D0085–0100Z
Preliminary
Rev.1.00
Oct.21.2003

Description

The HD151TS201AT is Intel CK408 type high-performance, low-skew, low-jitter, PC motherboard Clock generator. It is specifically designed for Intel Pentium®4 chipset.
Banias and Dothan processor / ODEM and MONTARA–GM chip set

Features

- 3 differential pairs of current mode control CPU clock
- 7 PCI clocks and 3 PCIF clocks @3.3V, 33.3MHz typ.
- 1 copy of 48MHz for USB @3.3V
- 1 copy of 48MHz for DOT @3.3V
- 6 copies of 3V66 clock @3.3V,66.6MHz
- 1 copy of VCH@3.3V, 48MHz
- Power save and clock stop function.
- I^2C^{TM} serial port programming
- Programmable Clock Control (Spread Spectrum Percentage, Clock Output Skew, Slew Rate)
- 56pin TSSOP (244 mils)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD151TS201ATEL	TSSOP-56 pin	—	AT	EL (1,000 pcs / Reel)

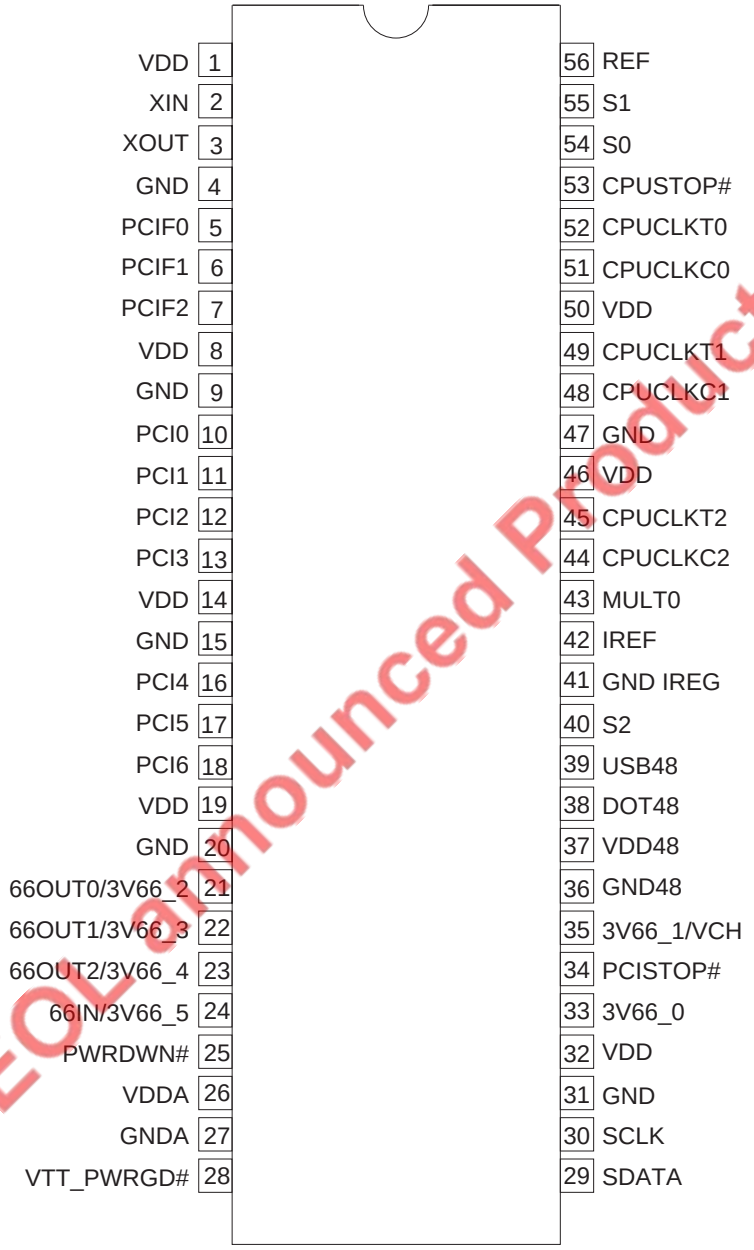
Note: Please consult the sales office for the above package availability.

Note: I^2C is a trademark of Philips Corporation.
Pentium is registered trademark of Intel Corporation

Key Specifications

- Supply Voltages: VDD = 3.0 V to 3.475 V
- CPU Clock cycle to cycle jitter = |150 ps|
- CPU clock group Skew = 100 ps
- 3V66 clock group Skew = 250 ps max
- PCI clock group Skew = 500 ps max

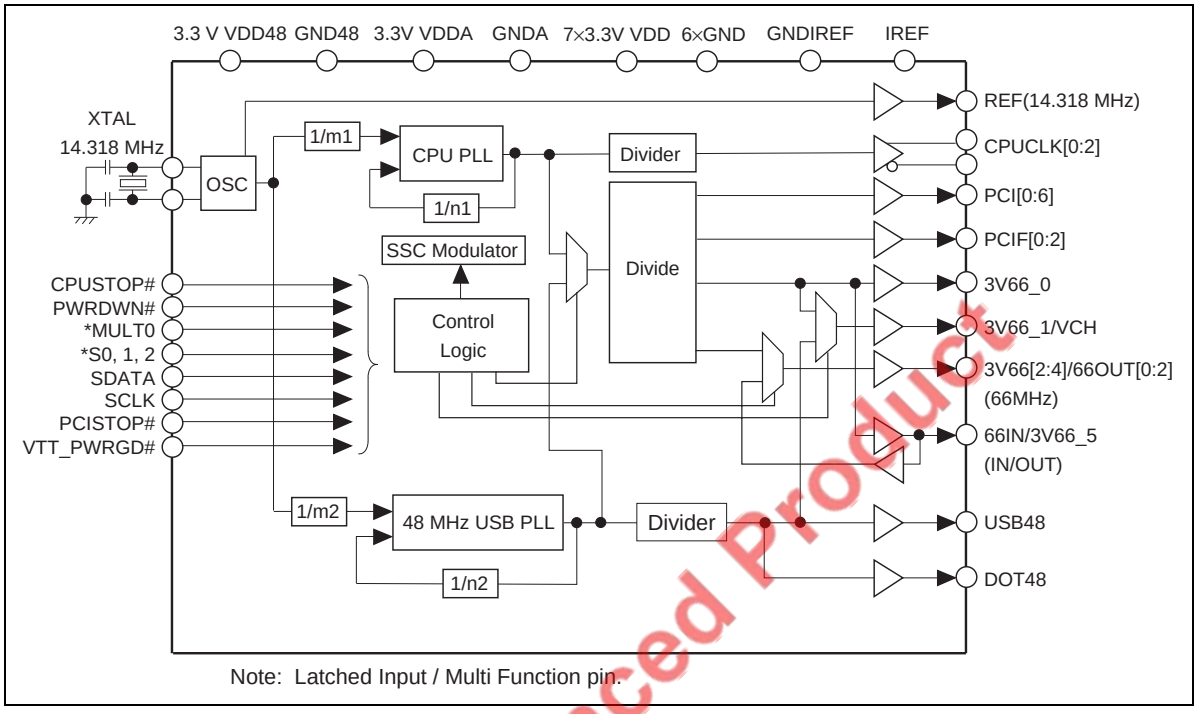
Pin Arrangement



(Top view)

PCISTOP#, MULT0, PWRDWN#, CPUSTOP# = 150KΩ Internal Pull-up

Block Diagram



Note: Latched Input / Multi Function pin.

Table1 Clock Frequency Function Table & I^2C

Byte8 (bit1, 2, 3, 4, 5)

	Bit5	Bit4	Bit3	Bit2	Bit1	CPU	3V66	PCI
0	0	0	0	0	0	66.67	66.67	33.33
1	0	0	0	0	1	100	66.67	33.33
2	0	0	0	1	0	200	66.67	33.33
3	0	0	0	1	1	133.33	66.67	33.33
4	0	0	1	0	0	150	50	25
5	0	0	1	0	1	166.67	55.56	27.78
6	0	0	1	1	0	150	66.67	33.33
7	0	0	1	1	1	166.67	66.67	33.33

Table2 Hardware Clock Frequency Table (MHz)

S2	S1	S0	CPU	3V66	66OUT[2:0] 3V66[4:0]	66IN 3V66_5	PCI	Note
0	0	0	66.67	66.67	66.67	66.67	33.33	Un-Buff Mode
0	0	1	100	66.67	66.67	66.67	33.33	Un-Buff Mode
0	1	0	200	66.67	66.67	66.67	33.33	Un-Buff Mode
0	1	1	133.33	66.67	66.67	66.67	33.33	Un-Buff Mode
1	0	0	66.67	66.67	66IN	66IN	66MHzIN/2	Buff Mode
1	0	1	100	66.67	66IN	66IN	66MHzIN/2	Buff Mode
1	1	0	200	66.67	66IN	66IN	66MHzIN/2	Buff Mode
1	1	1	133.33	66.67	66IN	66IN	66MHzIN/2	Buff Mode
Mid	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Tristate Mode
Mid	0	1	TCLK/2	TCLK/4	TCLK/4	TCLK/4	TCLK/8	Test Mode
Mid	1	0	150	50	50	50	25	
Mid	1	1	166.67	55.5	55.5	55.5	27.7	

Note: TCLK is a test clock over driven on the XIN during test mode.

Table3 CPUCLK Outputs Specification

MULT0 (pin43)	Board Target Trace/Term Z	Reference R, Iref = VDD/(3Rr)	Output Current Ioh	Voh @Z
0	50 Ω	Rr=221 1% I_REF=5.00mA	4 x Iref	1.0V @50 Ω
1	50 Ω	Rr=475 1% I_REF=2.32mA	6 x Iref	0.7V @50 Ω

Table4 Clock Power Management Truth Table

Byte0/bit6	Byte1/bit6	PWRDWN#	CPUSTOP#	*CPU Stoppable	*CPU Free Running
0	0	1	1	Run	Run
0	0	1	0	Iref*6	Run
0	0	0	1	Iref*2	Iref*2
0	0	0	0	Iref*2	Iref*2
0	1	1	1	Run	Run
0	1	1	0	Hi-Z	Run
0	1	0	1	Hi-Z	Iref*2
0	1	0	0	Hi-Z	Iref*2
1	0	1	1	Run	Run
1	0	1	0	Iref*6	Run
1	0	0	1	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Hi-Z
1	1	1	1	Run	Run
1	1	1	0	Hi-Z	Run
1	1	0	1	Hi-Z	Hi-Z
1	1	0	0	Hi-Z	Hi-Z

Note: CPUT&C State are controlled by Byte1 (bit3,4,5)

Table5 PCISTOP# I^2C control Truth Table

PCISTOP# (pin34)	Byte0/bit3 Write bit	Byte0/bit3 Read bit (Internal status)
0	0	0
0	1	0
1	0	0
1	1	1

Table6 S2 pin Three Level Input

Logic Level	Min Voltage	Max Voltage
0 (Low)	—	0.8 V
Mid	1.0 V	1.8 V
1 (High)	2.0 V	—

I²C Controlled Register Bit Map

Byte0 Control Register

Bit	Description	Contents	Default
7	Spread spectrum Enable	"1" = SSC ON "0" = SSC OFF	0
6	CPUCLK Power down mode setting. See Table4.	See Table4	0
5	VCH (pin35) Select 66 MHZ or 48 MHz	"1" = 48 MHz "0" = 66 MHz	0
4	CPUSTOP# status register	CPUSTOP# Reflects the current value of external CPUSTOP# (pin53). This bit is read only.	1
3	PCISTOP# Selection. See Table5	Reflects the current value of the internal PCISTOP# function when read. Internally PCISTOP# is a logical AND function of the internal SM Bus registers bit and the external PCISTOP# (pin34).	1
2	Reflects the value of the S2 (pin40)	Frequency selects bit2, reflects the value of S2 (pin40). This bit is read only.	X
1	Reflects the value of the S1 (pin55)	Frequency selects bit1, reflects the value of S1 (pin55). This bit is read only.	X
0	Reflects the value of the S0(pin54)	Frequency selects bit0, reflects the value of S0 (pin54). This bit is read only.	X

Byte1 Control Register

Bit	Description	Contents	Default
7	MULT0 (pin43) Value	MULT0 value. This bit is read only.	X
6	CPUCLK Power down mode setting. See Table4.	See Table4	0
5	Control of CPU2 with CPUSTOP#	"1" = Free running "0" = Not free running. When this bit is "0", CPUT/C outputs are affected by CPUSTOP# pin.	0
4	Control of CPU1 with CPUSTOP#		0
3	Control of CPU0 with CPUSTOP#		0
2	CPUT2/C2 Enable register	"1" = Enabled "0" = Disabled (CPUT stops "High" & CPUC stops "Low")	1
1	CPUT1/C1 Enable register		1
0	CPUT0/C0 Enable register		1

I²C Controlled Register Bit Map (cont.)

Byte2 PCI clock enable Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	PCI6 Enable register	"1" = Enabled	1
5	PCI5 Enable register	"0" = Disabled	1
4	PCI4 Enable register	(Each PCI clock stops "Low")	1
3	PCI3 Enable register		1
2	PCI2 Enable register		1
1	PCI1 Enable register		1
0	PCI0 Enable register		1

Byte3 PCIF & USB, DOT enable Register

Bit	Description	Contents	Default
7	DOT output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
6	USB output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
5	Control of PCIF2 with PCISTOP#	"1" = Not Free running.	0
4	Control of PCIF1 with PCISTOP#	When this bit is "1", PCIF outputs are stopped by PCISTOP# pin.	0
3	Control of PCIF0 with PCISTOP#	"0" = Free running.	0
2	PCIF2 output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
1	PCIF1 output enable	1 = Enable, 0 = Disable (DC Low fixed)	1
0	PCIF0 output enable	1 = Enable, 0 = Disable (DC Low fixed)	1

Byte4 66OUT, 3V66 Enable Register

Bit	Description	Contents	Default
7	Reserved		0
6	Reserved		0
5	3V66_0 Enable	1 = Enable, 0 = Disable (DC Low fixed)	1
4	3V66_1/VCH Enable	1 = Enable, 0 = Disable (DC Low fixed)	1
3	3V66_5 Enable	1 = Enable, 0 = Disable (DC Low fixed)	1
2	66OUT2/3V66_4 Enable	1 = Enable, 0 = Disable (DC Low fixed)	1
1	66OUT1/3V66_3 Enable	1 = Enable, 0 = Disable (DC Low fixed)	1
0	66OUT0/3V66_2 Enable	1 = Enable, 0 = Disable (DC Low fixed)	1

I²C Controlled Register Bit Map (cont.)

Byte5 Control Register

Bit	Description	Contents	Default
7	Reserved		0
6	Reserved		0
5	66IN to 66OUT [2:0] delay bit1		0
4	66IN to 66OUT[2:0] delay bit0		0
3	DOT Slew Rate Control bit1	00 = Default 01 = Fast1 10 = Fast2 11 = Slow1	0
2	DOT Slew Rate Control bit0		0
1	USB Slew Rate Control bit1	00 = Default 01 = Fast1 10 = Fast2 11 = Slow1	0
0	USB Slew Rate Control bit0		0

Byte6 Vendor ID Register

Bit	Description	Contents	Default
7	Revision Code		0
6			0
5			0
4			1
3	Vendor ID Register	Renesas = “1111”	1
2			1
1			1
0			1

Note: This register is read only register. Don’t write any data.

Byte7 Byte Count Read Back Register

Bit	Description	Contents	Default
7	Byte Count setting bit7	Writing to this register will configure byte.	0
6	Byte Count setting bit6	Count and how many bytes will be read back.	0
5	Byte Count setting bit5	Default is 17hex = 23 bytes.	0
4	Byte Count setting bit4		1
3	Byte Count setting bit3		0
2	Byte Count setting bit2		1
1	Byte Count setting bit1		1
0	Byte Count setting bit0		1

I²C Controlled Register Bit Map (cont.)

Byte8 Clock Frequency Control Register

Bit	Description	Contents	Default
7	Reserved		X
6	Reserved		X
5	Reserved		0
4	Reserved		0
3	Clock Freq. Control bit2	See Table1	0
2	Clock Freq. Control bit1		0
1	Clock Freq. Control bit0		0
0	Freq. Select Mode bit	0 = Freq. is selected by latched input S2:0 1 = Freq. is selected by I²C Byte8 bit5:1	0

Byte9 Control Register

Bit	Description	Contents	Default
7	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Spread Spectrum Control bit	0 = –0.5% (Default) 1 = –1.0%	0
2	3V66 & PCI Clock PLL select bit	“0” = CPU PLL “1” = USB PLL When this bit set to “1”, 3V66 & PCI clocks will be supply from USB PLL. Not depended on CPU PLL.	0
1	PLL N Divider Control bit9	PLL N Divider Control bit9	0
0	PLL N Divider Control bit8	PLL N Divider Control bit8	0

Note: Byte9 [1:0], Byte10 and Byte11must be written together (at writing Byte11) in every case.

I²C Controlled Register Bit Map (cont.)

Byte10 PLL N Divide Ratio Control Register

Bit	Description	Contents	Default
7	PLL N Divider Control bit7	PLL N Divider Control bit7	X
6	PLL N Divider Control bit6	PLL N Divider Control bit6	X
5	PLL N Divider Control bit5	PLL N Divider Control bit5	X
4	PLL N Divider Control bit4	PLL N Divider Control bit4	X
3	PLL N Divider Control bit3	PLL N Divider Control bit3	X
2	PLL N Divider Control bit2	PLL N Divider Control bit2	X
1	PLL N Divider Control bit1	PLL N Divider Control bit1	X
0	PLL N Divider Control bit0	PLL N Divider Control bit0	X

Note: The default N value will be reflected in S [2:0] or Byte8 bit[5:1] frequency setting value.
Byte9 [1:0], Byte10 and Byte11must be written together (at writing Byte11) in every case.

Byte11 PLL M Divide Ratio Control Register

Bit	Description	Contents	Default
7	N & M divider enable bit	0: N & M value will be determined by S [2:0] or Byte8 bit[5:1]. 1: N & M value will be determined by Byte9,10,11.	0
6	PLL M Divider Control bit6	PLL M Divider Control bit6	X
5	PLL M Divider Control bit5	PLL M Divider Control bit5	X
4	PLL M Divider Control bit4	PLL M Divider Control bit4	X
3	PLL M Divider Control bit3	PLL M Divider Control bit3	X
2	PLL M Divider Control bit2	PLL M Divider Control bit2	X
1	PLL M Divider Control bit1	PLL M Divider Control bit1	X
0	PLL M Divider Control bit0	PLL M Divider Control bit0	X

Note: The default M value will be reflected in S [2:0] or Byte8 bit[5:1] frequency setting value.
Byte9 [1:0], Byte10 and Byte11must be written together (at writing Byte11) in every case.

I²C Controlled Register Bit Map (cont.)

Byte12 Clock Outputs Divider Control Register

Bit	Description	Contents	Default
7	Reserved		0
6	Reserved		0
5	Reserved		0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0	Reserved		0

Byte13 Clock Outputs Divider Control Register

Bit	Description	Contents	Default
7	PCISTOP# pin Enable	0 = Enable, 1 = Disable	0
6	CPUSTOP# pin Enable	0 = Enable, 1 = Disable	0
5	PWRDWN# pin Enable	0 = Enable, 1 = Disable	0
4	Reserved		0
3	Reserved		0
2	Reserved		0
1	Reserved		0
0	Reserved		0

Note: Byte 12 & 13 must be written together in every case.

I²C Controlled Register Bit Map (cont.)

Byte14 Control Register

Bit	Description	Contents	Default
7	Reserved		0
6	DOT Clock Invert	0=Normal, 1=Inverted	0
5	USB clock Invert	0=Normal, 1=Inverted	0
4	VCH clock Invert	0=Normal, 1=Inverted	0
3	PCI clock Invert	0=Normal, 1=Inverted	0
2	66OUT clock Invert	0=Normal, 1=Inverted	0
1	3V66 clock Invert	0=Normal, 1=Inverted	0
0	CPU clock Invert	0=Normal, 1=Inverted	0

Byte15 Control Register

Bit	Description	Contents	Default
7	REF clock enable	0 = Enable, 1 = Disable	0
6	Control of PCI6 with PCISTOP#	"0" = Not Free running When this bit is "0", PCI outputs are stopped by PCISTOP# pin. "1" = Free running.	0
5	Control of PCI5 with PCISTOP#		0
4	Control of PCI4 with PCISTOP#		0
3	Control of PCI3 with PCISTOP#		0
2	Control of PCI2 with PCISTOP#		0
1	Control of PCI1 with PCISTOP#		0
0	Control of PCI0 with PCISTOP#		0

Byte16 CPU Skew Control Register

Bit	Description	Contents		Default
7	(Reserved)			0
6	(Reserved)			0
5	CPU clock skew controlbit5	00 : Delay 0ps 01 : Delay 250ps	10 : Ahead 500ps 11 : Ahead 250ps	0
4	CPU clock skew controlbit4			0
3	CPU clock skew controlbit3	0100 : Delay 0ps 0101 : Delay 500ps 0110 : Delay 1000ps 0111 : Delay 1500ps 1000 : Delay 2000ps Don't set 1001 to 1111	0011 : Ahead 500ps 0010 : Ahead 1000ps 0001 : Ahead 1500ps 0000 : Ahead 2000ps	0
2	CPU clock skew controlbit2			1
1	CPU clock skew controlbit1			0
0	CPU clock skew controlbit0			0

I²C Controlled Register Bit Map (cont.)

Byte17 3V66 Skew Control Register

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	3V66 clock skew controlbit5	00 : Delay 0ps 11 : Ahead 500ps	0
4	3V66 clock skew controlbit4	01 : Delay 250ps 11 : Ahead 250ps	0
3	3V66 clock skew controlbit3	0100 : Delay 0ps	0
2	3V66 clock skew controlbit2	0101 : Delay 500ps 0011 : Ahead 500ps	0
1	3V66 clock skew controlbit1	0110 : Delay 1000ps 0010 : Ahead 1000ps 0111 : Delay 1500ps 0001 : Ahead 1500ps	1
0	3V66 clock skew controlbit0	1000 : Delay 2000ps 0000 : Ahead 2000ps Don't set 1001 to 1111	0

Byte18 PCI Skew Control Register 1

Bit	Description	Contents	Default
7	(Reserved)		0
6	(Reserved)		0
5	PCI clock skew controlbit5	00 : Delay 0ps 10 : Ahead 500ps	0
4	PCI clock skew controlbit4	01 : Delay 250ps 11 : Ahead 250ps	0
3	PCI clock skew controlbit3	0100 : Delay 0ps	0
2	PCI clock skew controlbit2	0101 : Delay 500ps 0011 : Ahead 500ps	1
1	PCI clock skew controlbit1	0110 : Delay 1000ps 0010 : Ahead 1000ps 0111 : Delay 1500ps 0001 : Ahead 1500ps	1
0	PCI clock skew controlbit0	1000 : Delay 2000ps 0000 : Ahead 2000ps Don't set 1001 to 1111	0

Byte19 PCI Skew Control Register 2

Bit	Description	Contents	Default
7	(Reserved)		0
6	PCI_F2 skew Early or Late	"0" = Early	0
5	PCI_F1 skew Early or Late	"1" = Late	0
4	PCI_F0 skew Early or Late		0
3	PCI clock skew controlbit3	0100 : Delay 0ps	0
2	PCI clock skew controlbit2	0101 : Delay 500ps 0011 : Ahead 500ps	1
1	PCI clock skew controlbit1	0110 : Delay 1000ps 0010 : Ahead 1000ps 0111 : Delay 1500ps 0001 : Ahead 1500ps	0
0	PCI clock skew controlbit0	1000 : Delay 2000ps 0000 : Ahead 2000ps Don't set 1001 to 1111	0

I²C Controlled Register Bit Map (cont.)

Byte20 PCI Skew Control Register 3

Bit	Description	Contents	Default
7	(Reserved)		0
6	PCI6 skew Early or Late	"0" = Early "1" = Late	0
5	PCI5 skew Early or Late		0
4	PCI4 skew Early or Late		0
3	PCI3 skew Early or Late		0
2	PCI2 skew Early or Late		0
1	PCI1 skew Early or Late		0
0	PCI0 skew Early or Late		0

Byte21 Slew Rate Control Register

Bit	Description	Contents	Default
7	PCI clock slew rate controlbit1	00 : Normal 10 : ++ 01 : + 11 : –	0
6	PCI clock slew rate controlbit0		0
5	PCIF clock slew rate controlbit1	00 : Normal 10 : ++ 01 : + 11 : –	0
4	PCIF clock slew rate controlbit0		0
3	66OUT clock slew rate controlbit1	00 : Normal 10 : ++ 01 : + 11 : –	0
2	66OUT clock slew rate controlbit0		0
1	3V66 clock slew rate controlbit1	00 : Normal 10 : ++ 01 : + 11 : –	0
0	3V66 clock slew rate controlbit0		0

Byte22 Slew Rate Control Register

Bit	Description	Contents	Default
7	Reserved		1
6	Reserved		0
5	Reserved		1
4	Reserved		1
3	REF clock slew rate controlbit1	00 : Normal 10 : ++ 01 : + 11 : –	0
2	REF clock slew rate controlbit0		0
1	VCH clock slew rate controlbit1	00 : Normal 10 : ++ 01 : + 11 : –	0
0	VCH clock slew rate controlbit0		0

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	VDD	–0.5 to 4.6	V	
Input voltage	V_I	–0.5 to 4.6	V	
Output voltage *[1]	V_O	–0.5 to VDD +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	V_O = 0 to VDD
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	Tstg	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	VDD	3.00	3.3	3.465	V	
Supply voltage	VDDA	3.00	3.3	3.465	V	
DC input signal voltage		–0.3	—	VDD+0.3	V	
High level input voltage	V_{IH}	2.0	—	VDD+0.3	V	
Low level input voltage	V_{IL}	–0.3	—	0.8	V	
Operating temperature	Ta	0	—	85	°C	

Pin Descriptions

Pin name	No.	Type	Description
GND	4,9,15,20 31,36,41,47	Ground	GND pins
VDD	1,8,14,19 32,37,46,50	Power	Power supplies pins. Nominal 3.3 V.
VDDA	26	Power	Power supply for PLL core.
GNDA	27	Power	Power supply for PLL core.
CPUT[2:0]	45,49,52	OUTPUT	"True" clocks of differential pair CPUCLK. These pins are HCSL output.
CPUC[2:0]	44,48,51	OUTPUT	"Complementary" clocks of differential pair CPUCLK. These pins are HCSL output.
CPUSTOP#	53	INPUT	CPUCLK STOP pin. Active low input. When asserted low, CPUT [2:0] clocks are synchronously disabled in high state and CPUC [2:0] clocks are synchronously disabled in a low state. CPUSTOP# pin is 150 kΩ internal pulled-up.
PCIF[2:0]	7,6,5	OUTPUT	Free running PCI clock 3.3 V output. 33 MHz clocks divided from 3V66.
PCI[6:0]	18,17,16,13 12,11,10	OUTPUT	3.3 V PCI clock outputs. 33 MHz clocks divided from 3V66.
PCISTOP#	34	INPUT	PCICLK STOP pin. Active low input. When asserted low, PCI [6:0] clocks are synchronously disabled in low state. This pin does not effect PCIF [2:0] clocks outputs if they are programmed to be PCIF clocks via the device's SM Bus interface. PCISTOP# pin is 150 kΩ internal pulled-up.
S1, S0	55,54	INPUT	Frequency selects input. See frequency table2 in page5.
S2	40	INPUT	Frequency selects input. See frequency table2 in page5. This pin is 3 level input.
VTT_PWRGD#	28	INPUT	Qualifying input that latches S [2:0] and MULT0. When this input is at a logic low, the S[2:0] and MULT0 are latched.

Pin Descriptions (cont.)

Pin name	No.	Type	Description
REF	56	OUTPUT	14.318MHz reference clock.
MULT0	43	INPUT	CPUCLK's output current setting. This pin is 150kΩ internal pull-up.
PWRDWN#	25	INPUT	Power down pin. All circuits will be powered down. (Output state of each output is shown in page Table.) Asynchronous active low input pin used to power down the device into low power state. The internal clocks are disabled and VCO and the crystal are stopped.
USB48	39	OUTPUT	3.3V 48 MHz USB clock output.
DOT48	38	OUTPUT	3.3V 48MHz DOT clock output.
XIN	2	INPUT	XTAL input.
XOUT	3	OUTPUT	XTAL output. Don't connect when an external clock is applied to XIN.
SDATA	29	INPUT/ OUTPUT	Data input/output for I^2C logic. This pin is internal pull-up to VDD by 150KΩ resistor.
SCLK	30	INPUT	Clock input for I^2C logic. This pin is internal pull-up to VDD by 150KΩ resistor.
IREF	42	IN	A precision resistor is attached to this pin which is connected to internal current reference. A resistor is connected between this pin and GNDIREF.
3V66_0	33	OUTPUT	3.3 V 66 MHz clock.
3V66_1/VCH	35	OUTPUT	3.3V clock output selectable with SM Bus byte0, bit5. When Byte0 bit5 is at logic"1", this pin is 48 MHz clock output. When Byte0 bit5 is at logic"0", this pin is 66 MHz clock output. Default is 66 MHz output.
66IN/3V66_5	24	IN/OUT	If S2 = 1, Input connection for 66OUT [2:0]. If S2 = 0, outputs fixed 66 MHz clock.
66OUT[2:0]/ 3V66[4:2]	23,22,21	OUTPUT	If S2 = 1, Buffered copies of 66IN. If S2=0, outputs fixed 66MHz clock.

DC Electrical Characteristics / Serial Input Port

Ta = 0°C to 85°C, VDD = 3.3 V

Item	Symbol	Min	typ*[1]	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	—	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	—	V	
Input Current	I_I	–50	—	+50	µA	V_I = 0 V or 3.465 V, VDD = 3.465 V
Input capacitance	C_I	—	10	—	pF	SDATA & SCLK*[2]

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.
2. Target of design, not 100% tested in production.

AC Electrical Characteristics / Serial Input port

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
SCLK Frequency	F_{SCLK}	—	—	100	kHz	Normal Mode
Start Hold Time	t_{STHD}	4.0	—	—	µs	
SCLK Low Time	t_{LOW}	4.7	—	—	µs	
SCLK High Time	t_{HIGH}	4.0	—	—	µs	
Data Setup Time	t_{DSU}	250	—	—	ns	
Data Hold Time	t_{DHD}	300	—	—	ns	
Stop Setup Time	t_{STSU}	4.0	—	—	µs	
BUS Free Time between Stop & Start Condition	t_{SPF}	4.7	—	—	µs	

Note: Target of design, not 100% tested in production.

DC Electrical Characteristics CPUT/C Clock

Ta = 0°C to 85°C

Item	Symbol	Min	Typ *[1]	Max	Unit	Test Conditions
Output voltage	V_O	—	0.695	1.2	V	Rp = 49.9, VDD = 3.3 V
Output Current	I_O	—	I(nom)	—	mA	VDD = 3.3 V *[2]
Output resistance		3000	—	—	Ω	V_O = 1.2 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions

2 I(nom) is output current(Ioh) shown in Page5 Table3.

AC Electrical Characteristics CPUT/C Clock (CPU at 0.7V Timing)

Ta = 0°C to 85°C, VDD = 3.3 V, C_L = 2 pF, Rs = 33.2 Ω, Rp = 49.9 Ω

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Cycle to cycle jitter*[1]	t_{CCS}	—	|150|	—	ps	
CPU Group Skew (CPU clock out to CPU clock out)	t_{skS}	—	|100|	—	ps	
Rise time	t_r	175	—	700	ps	V_O = 0.175 V to 0.525 V
Fall time	t_f	175	—	700	ps	V_O = 0.175 V to 0.525 V
Clock Duty Cycle		45	50	55	%	
CPU clock period (66)		—	15.075	—	ns	
CPU clock period (100)		—	10.25	—	ns	
CPU clock period (133)		—	7.5	—	ns	
CPU clock period (200)		—	4.975	—	ns	

Note: 1.Difference of cycle time between two adjoining cycles.

DC Electrical Characteristics / 3V66 Clock (CK408 Type5 Buffer)

Ta = 0°C to 85°C, VDD = 3.3 V

Item	Symbol	Min	Typ *1	Max	Unit	Test Conditions
Output Voltage	V_{OH}	3.1	—	—	V	I_{OH} = –1 mA, VDD = 3.3 V
	V_{OL}	—	—	50	mV	I_{OL} = 1 mA, VDD = 3.3 V
Output Current	I_{OH}	—	—	–33	mA	V_{OH} = 1.0 V
	I_{OL}	30	—	—	mA	V_{OL} = 1.95 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / 3V66 Clock

Ta = 0°C to 85°C, VDD = 3.3 V, C_L = 30 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t_{CCS}	—	|250|	—	ps	Fig1	*1
3V66 Group Skew	t_{skS}	—	0	250	ps	Rising edge @1.5 V to 1.5 V Fig.2	
Slew rate	t_{SL}	1.0	—	4.0	V/ns		0.4V to 2.4V
Clock Duty Cycle		45	50	55	%		
3V66[5:0] leads 33 MHz PCI		1.5	—	3.5	ns	Un-Buffer Mode	

Note: 1. Difference of cycle time between two adjoining cycles.

DC Electrical Characteristics / PCI & PCIF Clock (CK408 Type5 Buffer)

Ta = 0°C to 85°C, VDD = 3.3 V

Item	Symbol	Min	Typ *1	Max	Unit	Test Conditions
Output Voltage	V_{OH}	3.1	—	—	V	I_{OH} = –1 mA, VDD = 3.3 V
	V_{OL}	—	—	50	mV	I_{OL} = 1 mA, VDD = 3.3 V
Output Current	I_{OH}	—	—	–33	mA	V_{OH} = 1.0 V
	I_{OL}	30	—	—	mA	V_{OL} = 1.95 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / PCI & PCIF Clock

Ta = 0°C to 85°C, VDD = 3.3 V, C_L = 30 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t_{CCS}	—	|250|	—	ps	Fig1	*1
PCI Group Skew	t_{skS}	—	0	500	ps	Rising edge @1.5V to 1.5V Fig.2	
Clock Period		—	20.8316	—	ns		
Slew rate	t_{SL}	1.0	—	4.0	V/ns		0.4 V to 2.4 V
Clock Duty Cycle		45	50	55	%		

Note: 1. Difference of cycle time between two adjoining cycles.

DC Electrical Characteristics / USB & VCH Clock (CK408 Type3A Buffer)

Ta = 0°C to 85°C, VDD = 3.3 V

Item	Symbol	Min	Typ *1	Max	Unit	Test Conditions
Output Voltage	V_{OH}	3.1	—	—	V	I_{OH} = –1 mA, VDD = 3.3 V
	V_{OL}	—	—	50	mV	I_{OL} = 1 mA, VDD = 3.3 V
Output Current	I_{OH}	—	—	–29	mA	V_{OH} = 1.0 V
	I_{OL}	29	—	—	mA	V_{OL} = 1.95 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / USB & VCH Clock

Ta = 0°C to 85°C, VDD = 3.3 V, C_L = 20 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t_{CCS}	—	|350|	—	ps	Fig1	*1
Clock Period		—	20.82985	—	ns		
Slew rate	t_{SL}	1.0	—	2.0	V/ns		0.4 V to 2.4 V
Clock Duty Cycle		45	50	55	%		

Note: 1. Difference of cycle time between two adjoining cycles.

DC Electrical Characteristics / DOT Clock (CK408 Type3B Buffer)

Ta = 0°C to 85°C, VDD = 3.3 V

Item	Symbol	Min	Typ *1	Max	Unit	Test Conditions
Output Voltage	V_{OH}	3.1	—	—	V	I_{OH} = –1 mA, VDD = 3.3 V
	V_{OL}	—	—	50	mV	I_{OL} = 1 mA, VDD = 3.3 V
Output Current	I_{OH}	—	—	–29	mA	V_{OH} = 1.0 V
	I_{OL}	29	—	—	mA	V_{OL} = 1.95 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / DOT Clock

Ta = 0°C to 85°C, VDD = 3.3 V, C_L = 10 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t_{CCS}	—	|350|	—	ps	Fig1	*1
Clock Period		—	20.82985	—	ns		
Slew rate	t_{SL}	2.0	—	4.0	V/ns		0.4 V to 2.4 V
Clock Duty Cycle		45	50	55	%		

Note: 1. Difference of cycle time between two adjoining cycles.

DC Electrical Characteristics / REF Clock (CK408 Type5 Buffer)

Ta = 0°C to 85°C, VDD = 3.3 V

Item	Symbol	Min	Typ *1	Max	Unit	Test Conditions
Output Voltage	V_{OH}	3.1	—	—	V	I_{OH} = –1 mA, VDD = 3.3 V
	V_{OL}	—	—	50	mV	I_{OL} = 1 mA, VDD = 3.3 V
Output Current	I_{OH}	—	—	–33	mA	V_{OH} = 1.0 V
	I_{OL}	30	—	—	mA	V_{OL} = 1.95 V

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

AC Electrical Characteristics / REF Clock

Ta = 0°C to 85°C, VDD = 3.3 V, C_L = 30 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter	t_{CCS}	—	|1000|	—	ps	Fig1	*1
Clock Period		—	69.8413	—	ns		
Slew Rate		1.0	—	4.0	V/ns		
Clock Duty Cycle		45	50	55	%		

Note: 1. Difference of cycle time between two adjoining cycles.

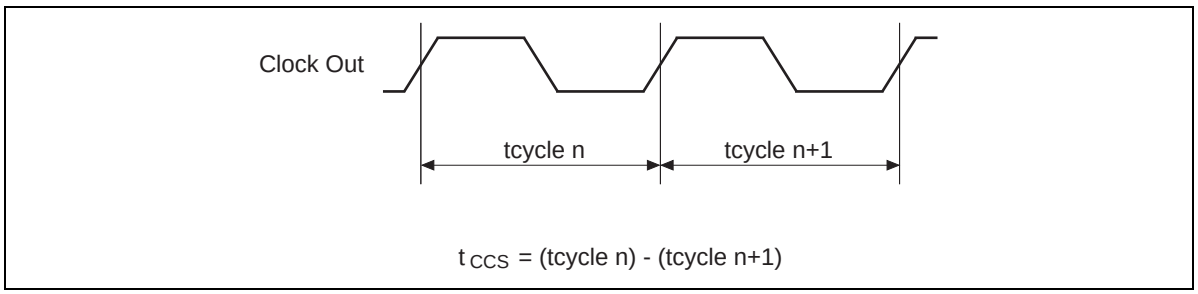


Figure1 Cycle to Cycle Jitter (3.3 V Single Ended Clock Output)

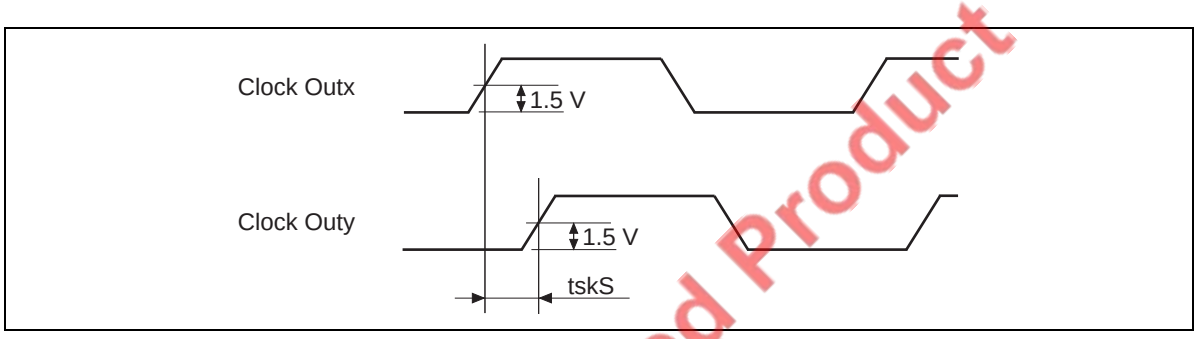


Figure2 Output Clock Skew (3.3 V Single Ended Clock Output)

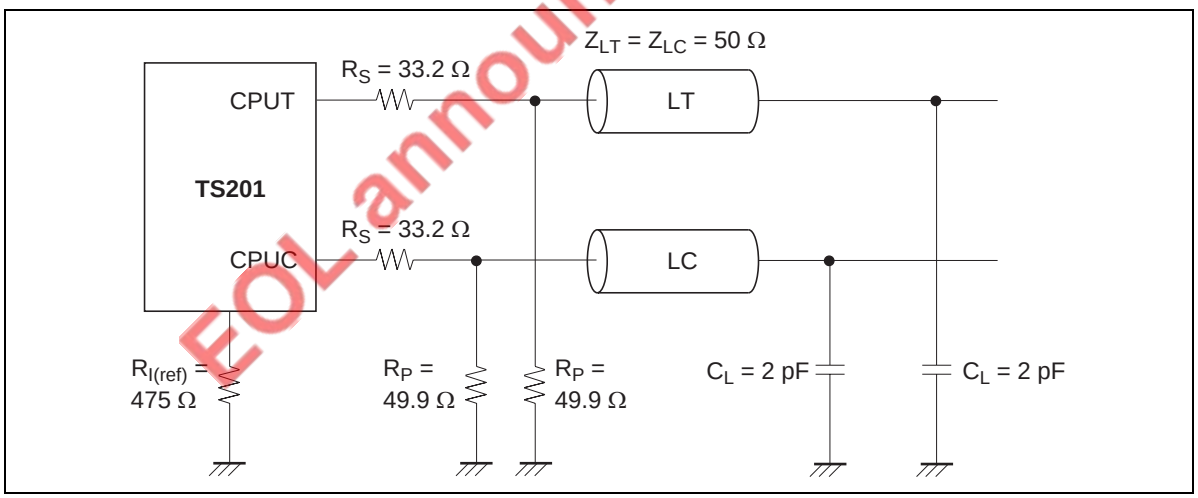


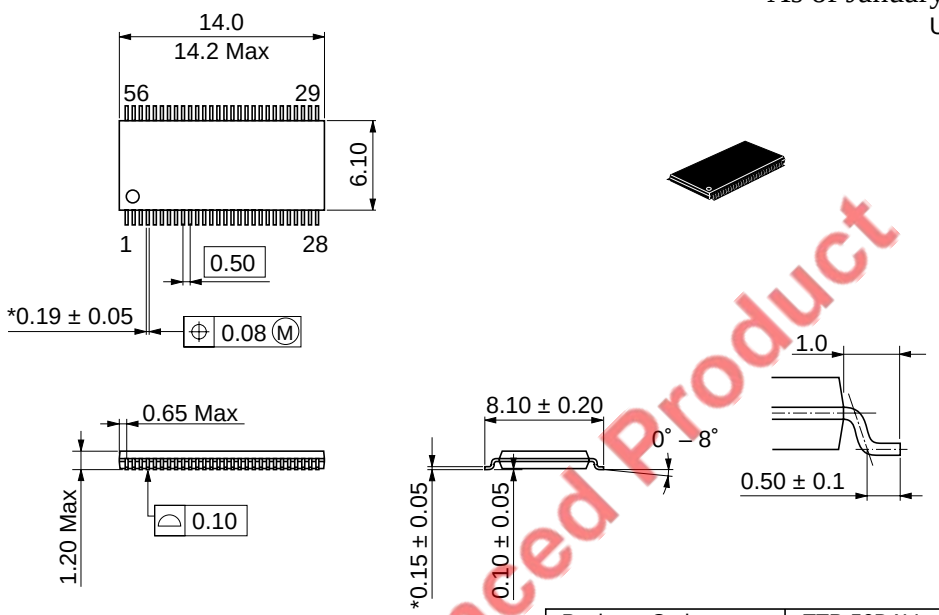
Figure3 Load Circuit for CPUT/C

Package Dimensions

• **TSSOP–56**

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-56DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.23 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Colophon 1.0