FEATURES

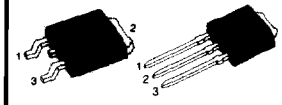
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 μA (Max.) @ V_{DS} = 600V
- Low $R_{DS(ON)}$: 9.390 Ω (Typ.)

BV_{DSS} = 600 V

$R_{DS(on)}$ = 12 Ω

I_D = 1 A

D²-PAK I²-PAK



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	600	V
I_D	Continuous Drain Current (T_C=25℃)	1	A
	Continuous Drain Current (T_C=100℃)	0.6	
I_{DM}	Drain Current-Pulsed ①	3	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy ②	44	mJ
I_{AR}	Avalanche Current ①	1	A
E_{AR}	Repetitive Avalanche Energy ①	3.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
P_D	Total Power Dissipation (T_A=25℃) *	3.1	W
	Total Power Dissipation (T_C=25℃)	34	W
	Linear Derating Factor	0.27	W/℃
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	℃
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–	3.67	℃/W
$R_{\theta JA}$	Junction-to-Ambient *	–	40	
$R_{\theta JA}$	Junction-to-Ambient	–	62.5	

* When mounted on the minimum pad size recommended (PCB Mount).

SAMSUNG ELECTRONICS

Electrical Characteristics (T_C=25℃ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	600	–	–	V	V_{GS}=0V, I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	–	0.74	–	V/℃	I_D=250μA ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–	4.0	V	V_{DS}=5V, I_D=250μA
I_{GSS}	Gate-Source Leakage, Forward	–	–	100	nA	V_{GS}=30V
	Gate-Source Leakage, Reverse	–	–	-100		V_{GS}=-30V
I_{DSS}	Drain-to-Source Leakage Current	–	–	25	μA	V_{DS}=600V
		–	–	250		V_{DS}=480V, T_C=125℃
$R_{DS(on)}$	Static Drain-Source On-State Resistance	–	–	12	Ω	V_{GS}=10V, I_D=0.5A ④
g_{fs}	Forward Transconductance	–	0.83	–	℧	V_{DS}=50V, I_D=0.5A ④
C_{iss}	Input Capacitance	–	145	190	pF	V_{GS}=0V, V_{DS}=25V, f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	–	20	24		
C_{rss}	Reverse Transfer Capacitance	–	7	9		
$t_{d(on)}$	Turn-On Delay Time	–	10	30	ns	V_{DD}=300V, I_D=1A, R_G=24Ω ***See Fig 13*** ④⑤
t_r	Rise Time	–	13	35		
$t_{d(off)}$	Turn-Off Delay Time	–	28	65		
t_f	Fall Time	–	13	35		
Q_g	Total Gate Charge	–	7.5	11	nC	V_{DS}=480V, V_{GS}=10V, I_D=1A ***See Fig 6 & Fig 12*** ④⑤
Q_{gs}	Gate-Source Charge	–	1.2	–		
Q_{gd}	Gate-Drain("Miller") Charge	–	4	–		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	–	–	1	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	–	–	3		
V_{SD}	Diode Forward Voltage ④	–	–	1.2	V	T_J=25℃, I_S=1A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	–	190	–	ns	T_J=25℃, I_F=1A
Q_{rr}	Reverse Recovery Charge	–	0.44	–	μC	di_F/dt=100A/μs ④

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=80mH, I_{AS}=1A, V_{DD}=50V, R_G=27Ω, Starting T_J=25℃

③ I_{SD}≤1A, di/dt≤60A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25℃

④ Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%

⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

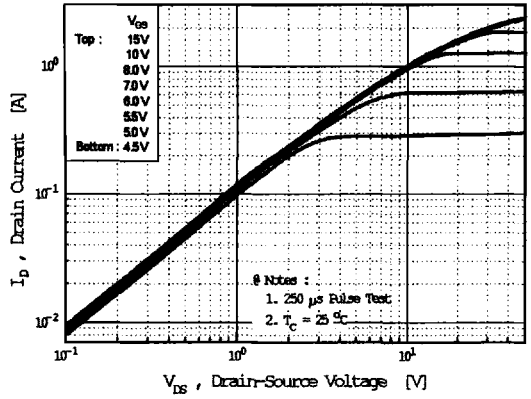


Fig 2. Transfer Characteristics

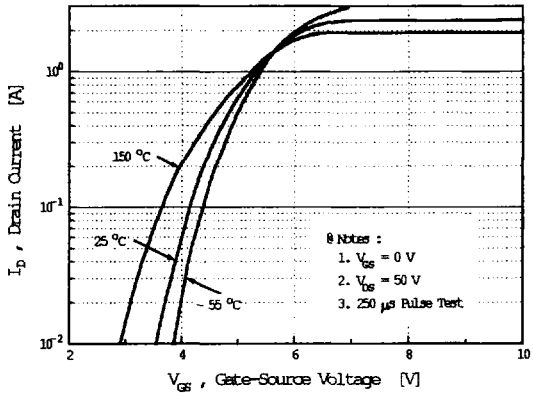


Fig 3. On-Resistance vs. Drain Current

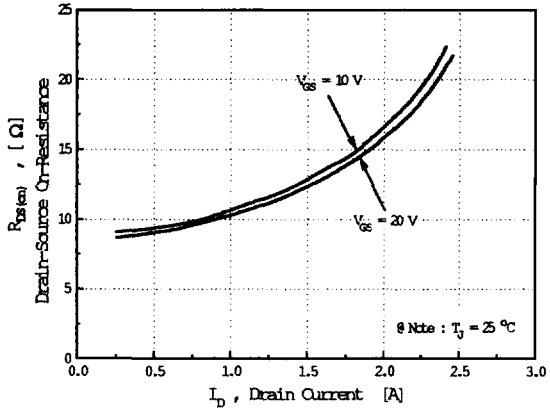


Fig 4. Source-Drain Diode Forward Voltage

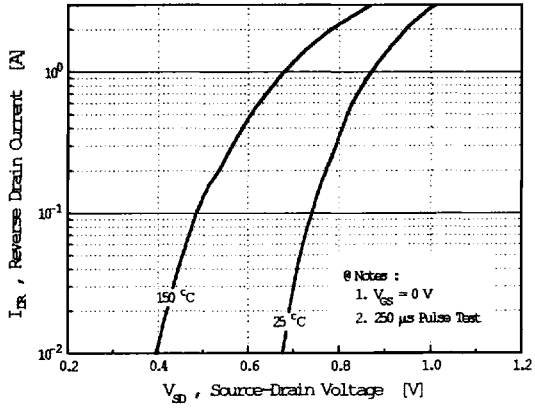


Fig 5. Capacitance vs. Drain-Source Voltage

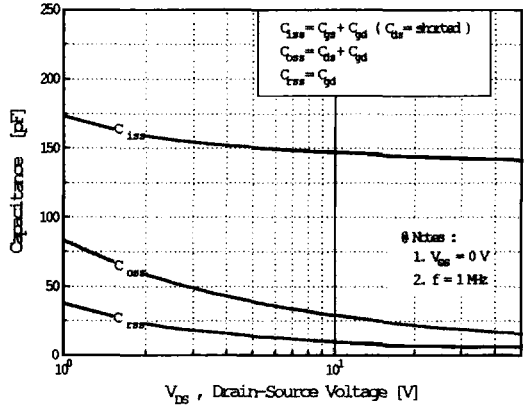


Fig 6. Gate Charge vs. Gate-Source Voltage

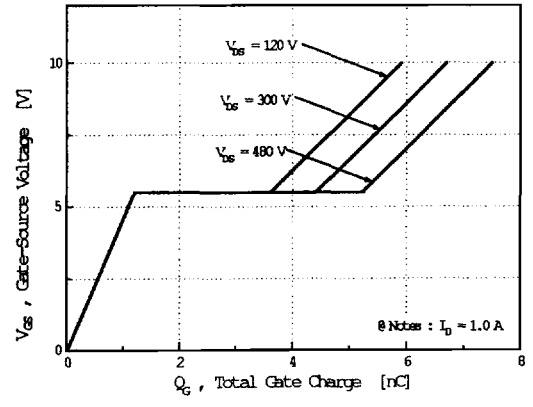


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Fig 7. Breakdown Voltage vs. Temperature

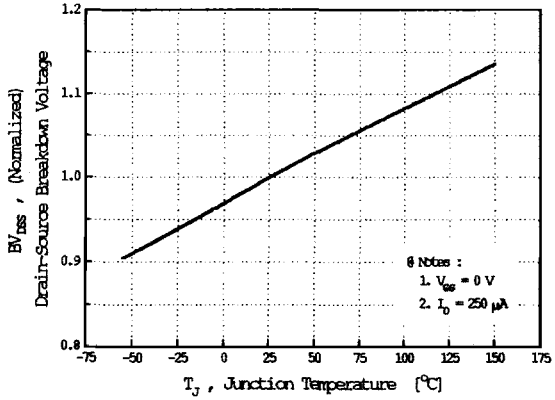

Fig 8. On-Resistance vs. Temperature

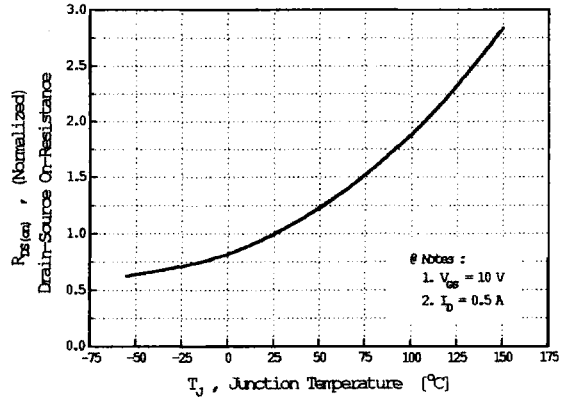

Fig 9. Max. Safe Operating Area

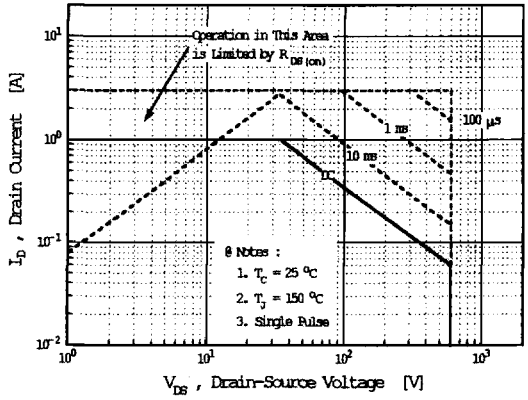

Fig 10. Max. Drain Current vs. Case Temperature

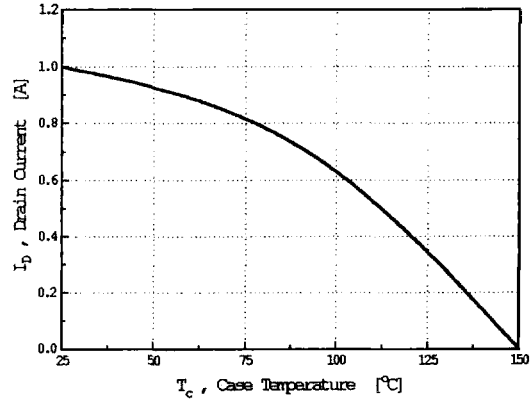

Fig 11. Thermal Response

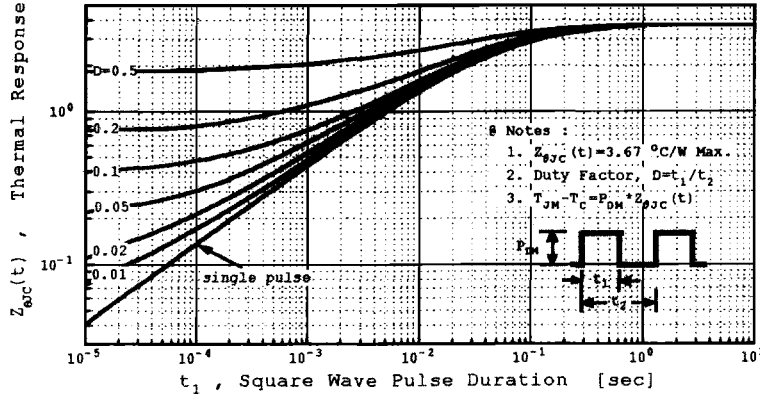

Fig 12. Gate Charge Test Circuit & Waveform

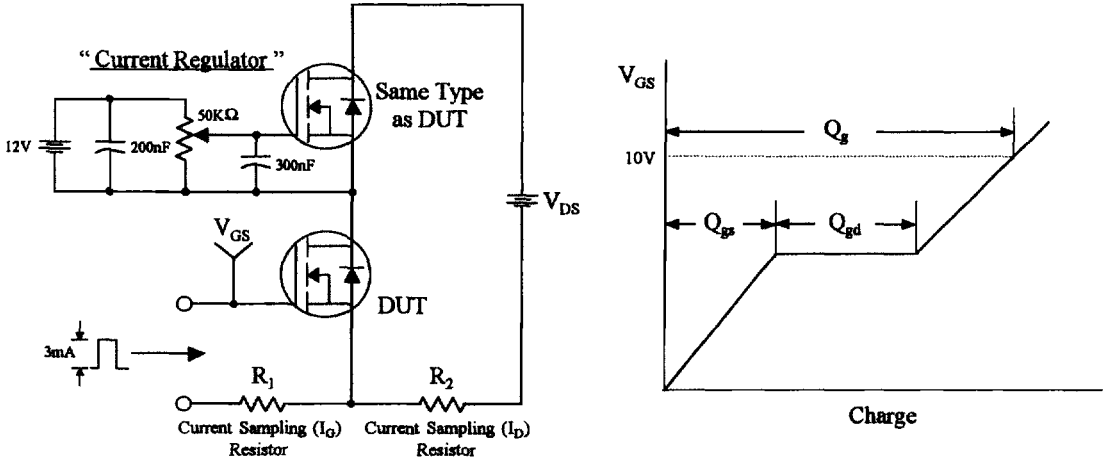

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Fig 13. Resistive Switching Test Circuit & Waveforms

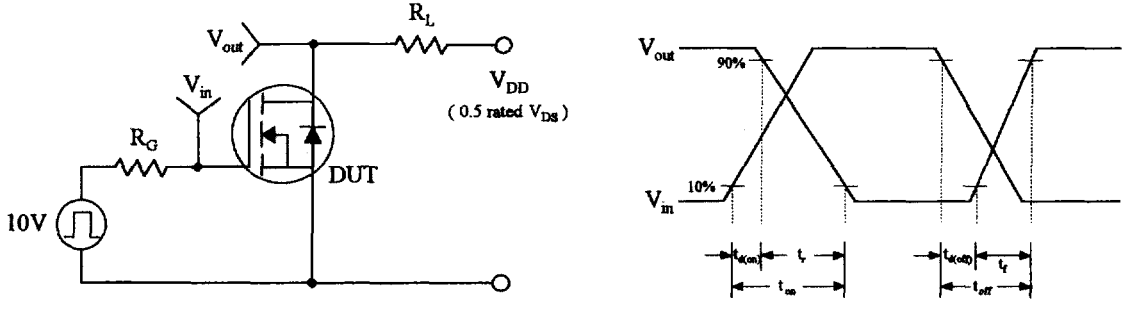

Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

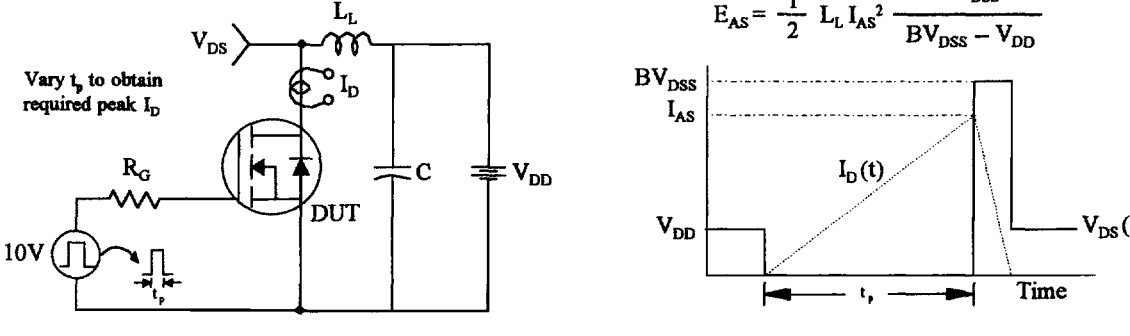

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms