

SCD#QM5266
Source Control Drawing

Upscreening/Manufacturing Specification FT9128-20BJA-AMD

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1 **INTRODUCTION**

This document specifies the procurement details and screening requirements

In brief the part is: 16,384-bit Static Ram SRAM 2048x8bits 200nS in 24-pin Ceramic DIL
A package description is given in section 6 of this document.

2 **REFERENCE DOCUMENTS**

Test Method Standard
Microcircuits

MIL-STD-883
(latest issue)

Department of Defence
Washington
DC 20363-5100, USA

Sort, incoming and outgoing
Inspection procedures

3 **SOURCE OF PARTS**

This section provides an overview of the companies involved in the manufacture, screening and supply of the part. Original procurement of parts shall be from the address specified in section 3.3.

3.1 **Original Part Manufacturer**

The original part (Untested packaged) are/were produced by Advanced Micro Devices

AMD Inc
PO Box 3453
Sunnyvale
CA94088-3453

The AMD donor part number is: AM9128-20DC

3.2 **Assy /Manu./Screening Company**

The above AMD parts are then assembled (if Applicable) and screened by:

Classified

Refer to section 4 for screening specifications.

3.3 UK Supplier

The assembled/screened parts shall be procured from:

Force Technologies Ltd
Ashley Court,
Henley,
Marlborough,
Wilts, UK
SN8 3RH

Tel: +44(0)1264 731200
Fax: +44(0)1264 731444

The Force Technologies part number(Ordering Code) is: **FT9128-20BJA-AMD**

4.0 Manufacture

Manufacturing processes as original manufacturer.....Advanced Micro Devices
(Manufacturing processes, assembly, Screen and test equipment listings available for inspection upon request.

4.1 SCREENING

The FT9128-20BJA-AMD shall be screened as specified in the table below.

All batches of parts shall be supplied with a Certificate of Conformity. The certificate of conformity shall reference the screening specified below.

Screening	Method	Req.t	Note
Internal visual	Sort, Incoming and Outgoing Inspection Procedures procedure: 05P-00212 10		N/A
Temperature cycling	1010, test condition C	100%	N/A
Constant acceleration	2001, test condition E (min) Y1 orientation only	100%	
Visual inspection		100%	N/A
Pre burn-in electrical parameters	In accordance with applicable device specification.	100%	N/A
Burn-in test	1015, 160 hours at 125°C minimum	100%	N/A
Interim (post burn-in) electrical parameters	In accordance with applicable device specification.	100%	N/A
Percentage defective allowable (PDA) calculation	5 percent	All lots	N/A
Seal a. Fine b. Gross	1014	100%	N/A
Final electrical test -55oC +25oC +125oC	In accordance with applicable device specification.	100%	4
External Visual	2009		N/A
Radiation latch-up	1020	Option	N/A

Notes:

4/ AM9128-20BJA

Am9128

2048 x 8 Static RAM

Am9128

DISTINCTIVE CHARACTERISTICS

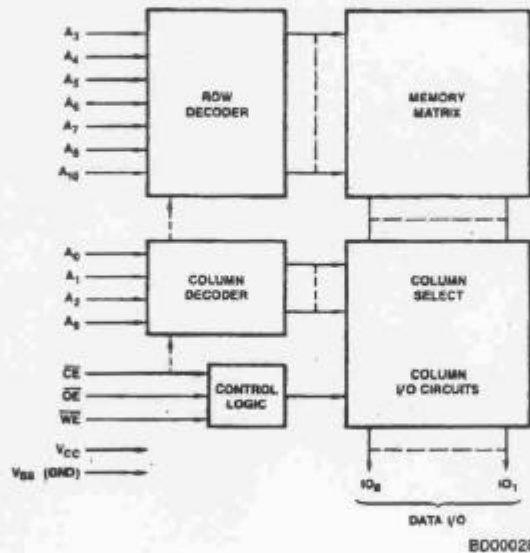
- Logic voltage levels compatible with TTL
- Three-state output buffers and common I/O
- I_{CC} Max. as low as 100 mA
- T_{AA}/T_{ACS} as low as 70 ns
- Power-Down mode (I_{SB} as low as 15 mA)

GENERAL DESCRIPTION

The Am9128 is a 16,384-bit Static Random Access Read-write Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5 V supply simplify system

designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROMs).

BLOCK DIAGRAM

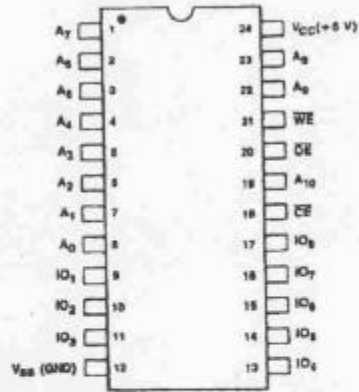


4

PRODUCT SELECTOR GUIDE

Part Number	Am9128-70	Am9128-90	Am9128-10	Am9128-12	Am9128-15	Am9128-20
Maximum Access Time (ns)	70	90	100	120	150	200
Maximum Operating Current (mA)	0 to 70°C	N/A	120	N/A	130	140
	-55° to 125°C	N/A	180	N/A	150	150
Maximum Standby Current (mA)	0° to 70°C	30	N/A	15	N/A	30
	-55° to 125°C	N/A	30	N/A	30	30

**CONNECTION DIAGRAM
Top View**



CD000121

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A ₃	AX ₀
A ₄	AX ₁
A ₅	AX ₂
A ₆	AX ₃
A ₇	AX ₄
A ₈	AX ₅
A ₁₀	AX ₆
A ₀	AY ₀
A ₁	AY ₁
A ₂	AY ₂
A ₉	AY ₃

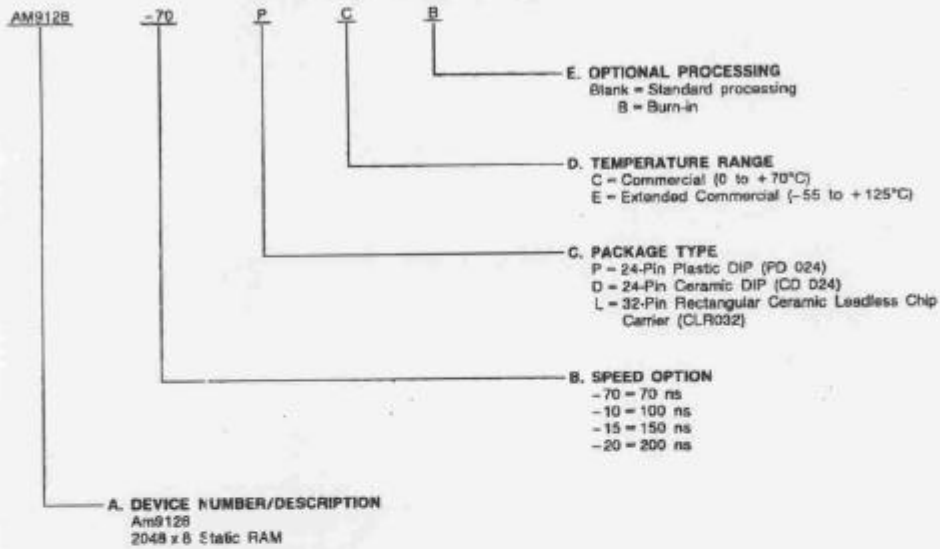


ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option (if applicable)**
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



Valid Combinations	
9128-70	PC, IC, DCB, DE, DEB, LC, LCB
9128-10	
9128-15	
9128-20	

Valid Combinations

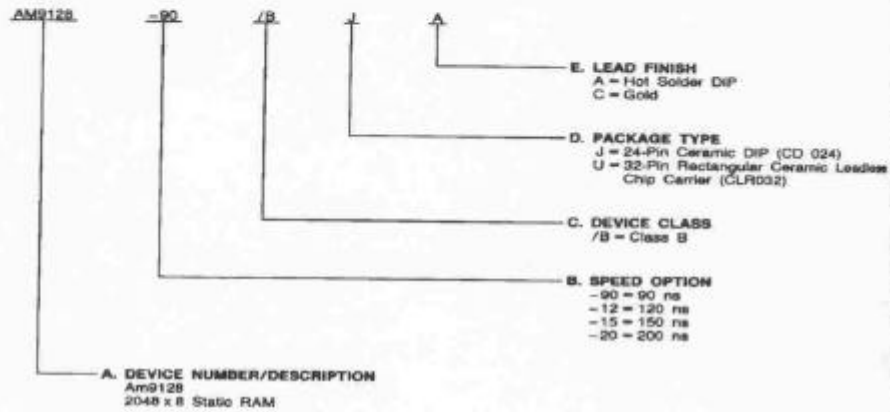
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by the combination of:

- A. Device Number
- B. Speed Option (if applicable)
- C. Device Class
- D. Package Type
- E. Lead Finish



Valid Combinations	
9128-90	/BJA, /BUC
9128-12	
9128-15	
9128-20	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local sales office to confirm availability of specific combinations or to check for newly released combinations.

PIN DESCRIPTION

A₀ - A₁₀ Addresses (Input)

The 10-bit field presented at the address inputs selects one of the 2048 memory locations to be read from — or written into — via the data lines.

I/O₁ - I/O₈ Data In/Out Port (Input/Output)

If WE is LOW, the data represented on the I/O lines can be written into the selected memory location. If WE is HIGH, the I/O lines represent the data read from the selected memory location.

CE Chip Enable (Input, Active LOW)

Read and Write cycles can be executed only when CE is LOW.

WE Write Enable (Input, Active LOW)

Data is written into the memory if WE is LOW and read the memory if WE is HIGH.

OE Output Enable (Input, Active LOW)

Read cycles can be executed only when OE is LOW.

ABSOLUTE MAXIMUM RATINGS (Note 11)

Storage Temperature	-65 to +150°C
Ambient Temperature with Power Applied	-55 to +125°C
Supply Voltage	-0.5 V to +7.0 V
Signal Voltage with Respect to Ground	-3.0 V to +7.0 V
Power Description	1.0 W
DC Output Current	10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Temperature	0 to +70°C
Supply Voltage	+4.5 V to +5.5 V

Military (M) Devices*	
Temperature	-55 to +125°C
Supply Voltage	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at $T_C = +25^\circ\text{C}$, $+125^\circ\text{C}$, and -55°C .

DC CHARACTERISTICS over operating range unless otherwise specified (Note 3)*

Parameter Symbol	Parameter Description	Test Conditions	Am9128-90 Am9128-10		Am9128-15		Am9128-70 Am9128-12 Am9128-20		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{OH}	Output HIGH Current	$V_{OH} = 2.4\text{ V}$	-2		-2		-2		mA
I_{OL}	Output LOW Current	$V_{OL} = 0.4\text{ V}$	4		4		4		mA
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 1.0$	2.0	$V_{CC} + 1.0$	2.0	$V_{CC} + 1.0$	Volts
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} < V_I < V_{CC}$		10		10		10	μA
I_{OZ}	Output Leakage Current	$V_{SS} < V_O < V_{CC}$ Output Disabled		10		10		10	μA
C_{IH}	Input Capacitance (Note 12)	Test Frequency = 1.0 MHz, $T_A = 25^\circ\text{C}$, All pins at 0		6		6		6	pF
C_{iO}	Input/Output Capacitance (Note 12)			7		7		7	pF
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC} , $\overline{CE} < V_{IL}$ Outputs Open	COM'L	120		100		140	mA
I_{SB}	Automatic \overline{CE} Power Down Current	Max. V_{CC} , $\overline{CE} > V_{IH}$	MIL	180		150		150	mA
			COM'L	15		15		30	mA
I_{PO}	Peak Power On Current (Note 12)	$V_{CC} = \text{GND to } V_{CC}$ Max. $\overline{CE} > V_{IH}$ (Note 2)	MIL	30		30		30	mA
			COM'L	15		15		30	mA

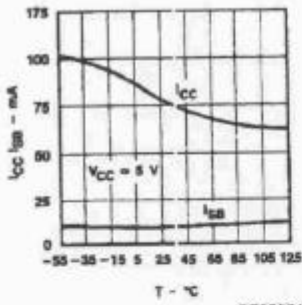
- Notes: 1. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. A pull up resistor to V_{CC} on the \overline{CE} input is required during power up to keep the device deselected, otherwise I_{PO} will exceed values given.
3. Ambient temperature is defined as the case temperature.
4. At any given temperature and voltage condition, I_{OZ} is less than I_{IX} .
5. \overline{WE} is HIGH for read cycle.
6. Device is continuously selected, $\overline{CE} = V_{IL}$.
7. Address valid prior to or coincident with \overline{CE} transition LOW.
8. $\overline{CE} = V_{IL}$.
9. $C_i = 30\text{ pF}$.
10. Transition is measured from 1.4 V on the input to 0.9 V and 1.9 V on the output using the load shown under Switching Test Circuit.
11. The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling, and use to avoid exposure to excessive voltages.
12. The parameter is guaranteed by characterization, but is not tested.

*See the last page of this spec for Group A Subgroup Testing information.

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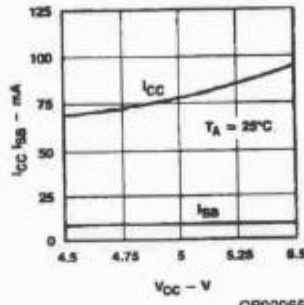
TYPICAL DC and AC CHARACTERISTICS

Supply Current
Versus Ambient Temperature



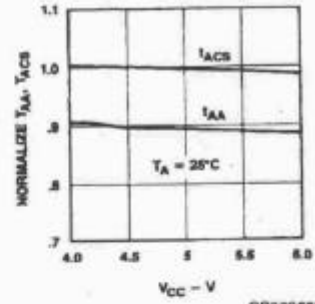
OP000640

Supply Current
Versus Supply Voltage



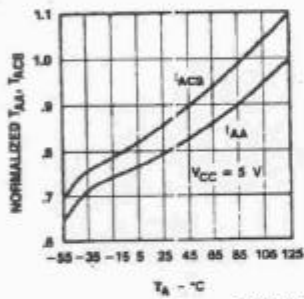
OP000650

Normalized Access Time
Versus Supply Voltage



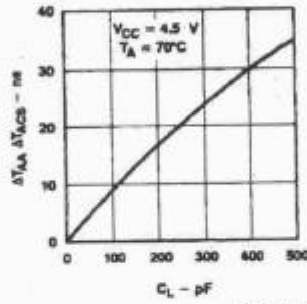
OP000660

Normalized Access Time
Versus Ambient Temperature



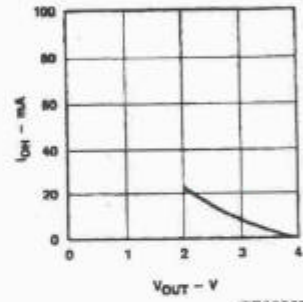
OP000670

Access Time Change
Versus Output Loading



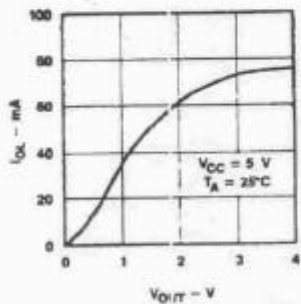
OP000680

Output Source Current
Versus Output Voltage



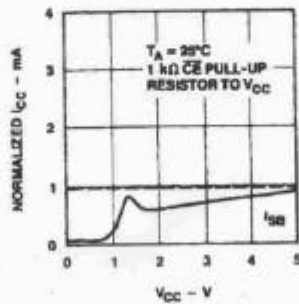
OP000690

Output Sink Current
Versus Output Voltage



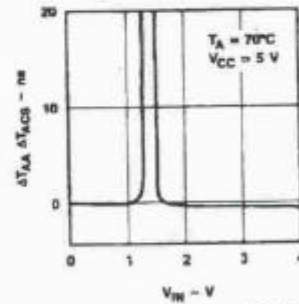
OP000700

Typical Power-On Current
Versus Power Supply



OP000710

Access Time Change
Versus Input Voltage



OP000720

SWITCHING TEST CONDITIONS

Input Pulse Levels	.4 to 2.4 V
Input Rise and Fall Times	10 ns
Input Timing Reference Levels	1.4 V
Output Timing Reference Levels	1.4 V

SWITCHING TEST CIRCUIT

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Cont'd.)

No.	Parameter Symbol	Parameter Description	Am9128-70		Am9128-90		Am9128-10		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle									
1	t _{RC}	Read Cycle Time	70		80		100		ns
2	t _{ACC}	Address Access Time (Note 9)		70		90		100	ns
3	t _{ACS}	Chip Select Access Time (Note 9)		70		90		100	ns
4	t _{OE}	Output Enable Time (Note 9)	COM'L	40		N/A		50	ns
			MIL		N/A		50	N/A	
5	t _{OH}	Output Hold Time from Address Change	5		5		5		ns
6	t _{OLZ}	Output in Low-Z from CE (Notes 4, 10)	5		5		5		ns
7	t _{CHZ}	Output in Hi-Z from CE (Notes 4, 10)		35		40		40	ns
8	t _{OLZ}	Output in Low-Z from OE (Notes 4, 10)	5		5		5		ns
9	t _{OHZ}	Output in Hi-Z from OE (Notes 4, 10)		30		35		35	ns
10	t _{PU}	Chip Selection to Power-Up Time (Note 12)	0		0		0		ns
11	t _{PD}	Chip Deselection to Power-Down Time (Note 12)		40		45		50	ns
Write Cycle									
12	t _{WC}	Write Cycle Time	70		90		100		ns
13	t _{CW}	Chip Selection to End of Write (Note 1)	0 to +70°C	80		N/A		90	ns
			-55 to -125°C	N/A		80		N/A	
14	t _{AS}	Address Setup Time	5		10		10		ns
15	t _{WP}	Write Pulse Width (Note 1)	40		55		60		ns
16	t _{WR}	Write Recovery Time	5		5		5		ns
17	t _{DS}	Data Setup Time	30		35		40		ns
18	t _{DH}	Data Hold Time	5		5		5		ns
19	t _{WLZ}	Output in Low-Z from WE (Notes 4, 10)	5		5		5		ns
20	t _{WHZ}	Output in Hi-Z from WE (Notes 4, 10)		30		35		35	ns
21	t _{AW}	Address to End of Write	65		80		80		ns

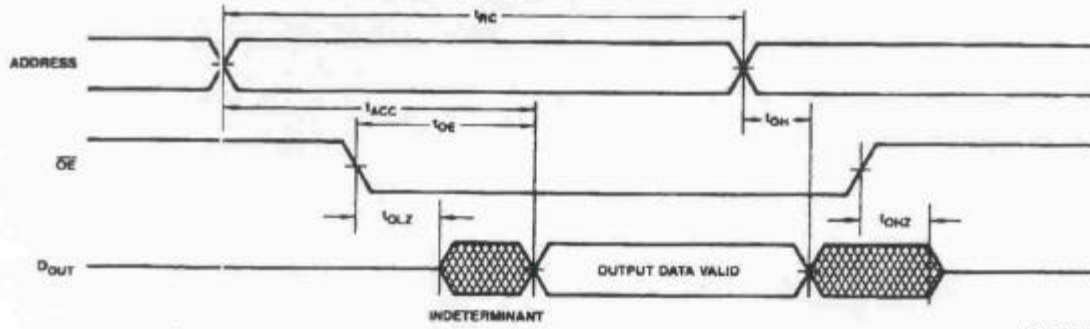
Notes: See notes to following DC Characteristics table.
 *See the last page of this spec for Group A Subgroup Testing information.

4

SWITCHING CHARACTERISTICS*									
No.	Parameter Symbol	Parameter Description	Am9128-12		Am9128-15		Am9128-20		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle									
1	t _{RC}	Read Cycle Time	120		150		200		ns
2	t _{ACC}	Address Access Time (Note 9)		120		150		200	ns
3	t _{ACS}	Chip Select Access Time (Note 9)		120		150		200	ns
4	t _{OE}	Output Enable Time (Note 9)	COM'L		N/A		60		ns
			MIL		70		70		
5	t _{OH}	Output Hold Time from Address Change	5		5		5		ns
6	t _{CLZ}	Output in Low-Z from \overline{CE} (Notes 4, 10)	5		5		5		ns
7	t _{CHZ}	Output in Hi-Z from \overline{CE} (Notes 4, 10)		50		55		55	ns
8	t _{OLZ}	Output in Low-Z from \overline{OE} (Notes 4, 10)	5		5		5		ns
9	t _{CHZ}	Output in Hi-Z from \overline{OE} (Notes 4, 10)		45		50		50	ns
10	t _{PU}	Chip Selection to Power-Up Time (Note 12)	0		0		0		ns
11	t _{PD}	Chip Deselection to Power-Down Time (Note 12)		55		60		60	ns
Write Cycle									
12	t _{WC}	Write Cycle Time	120		150		200		ns
13	t _{OW}	Chip Selection to End of Write (Note 1)	COM'L		N/A		150		ns
			MIL		105		130		
14	t _{AS}	Address Setup Time	10		20		20		ns
15	t _{WP}	Write Pulse Width (Note 1)	70		85		100		ns
16	t _{WR}	Write Recovery Time	5		5		5		ns
17	t _{DS}	Data Setup Time	45		50		60		ns
18	t _{DH}	Data Hold Time	5		5		5		ns
19	t _{WLZ}	Output in Low-Z from \overline{WE} (Notes 4, 10)	5		5		5		ns
20	t _{WHZ}	Output in Hi-Z from \overline{WE} (Notes 4, 10)		50		50		50	ns
21	t _{AW}	Address to End of Write	105		120		120		ns
<p>Notes: See notes following DC Characteristics table. *See the last page of this spec for Group A Subgroup Testing information.</p>									

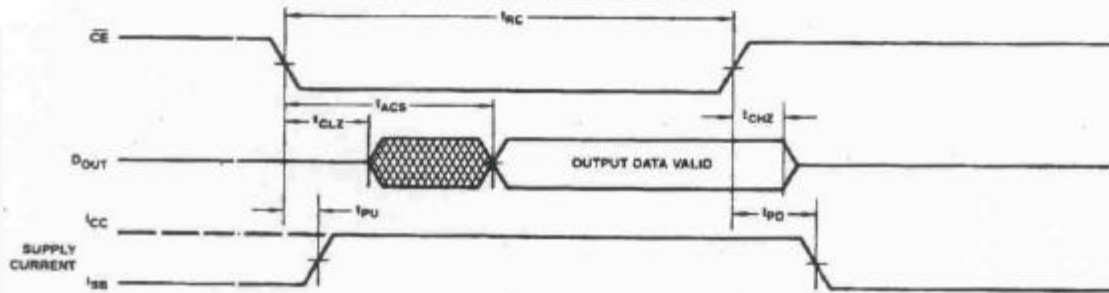
SWITCHING WAVEFORMS (Cont'd.)

READ CYCLE NO. 1 (Notes 5, 6)



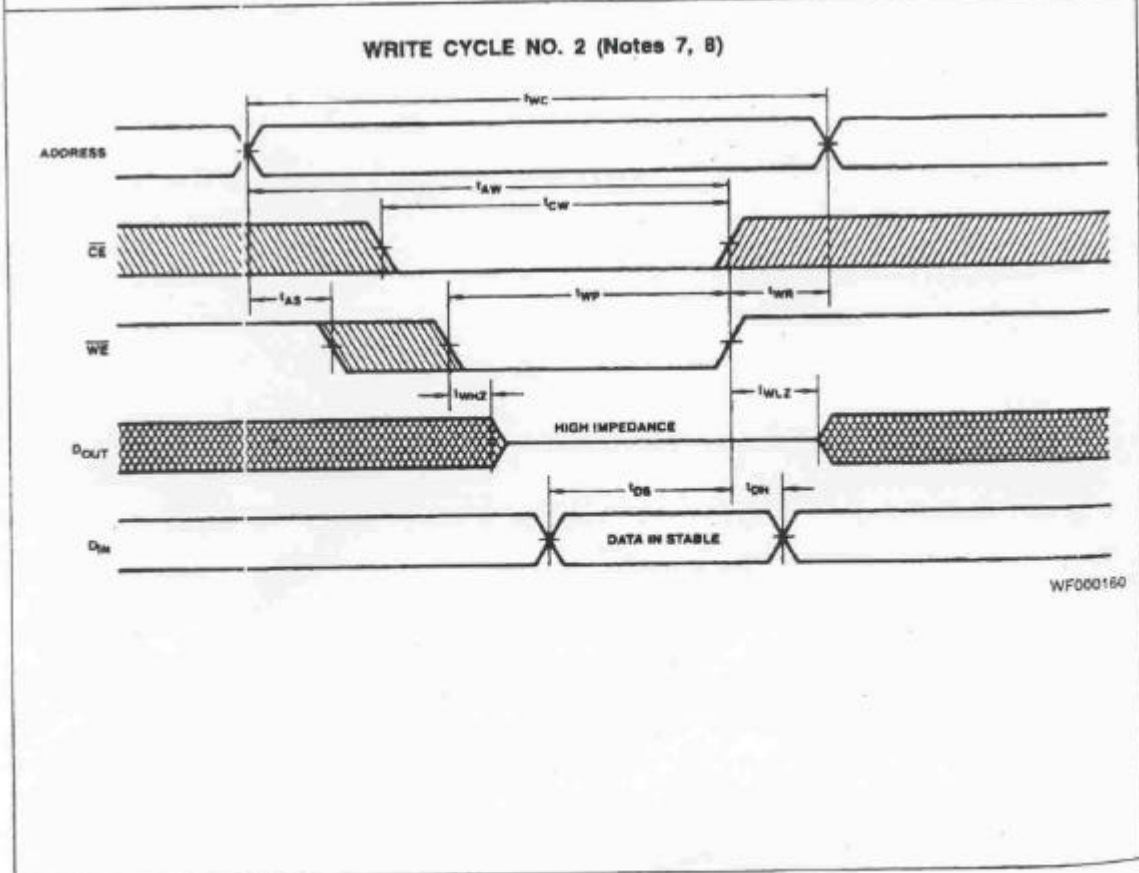
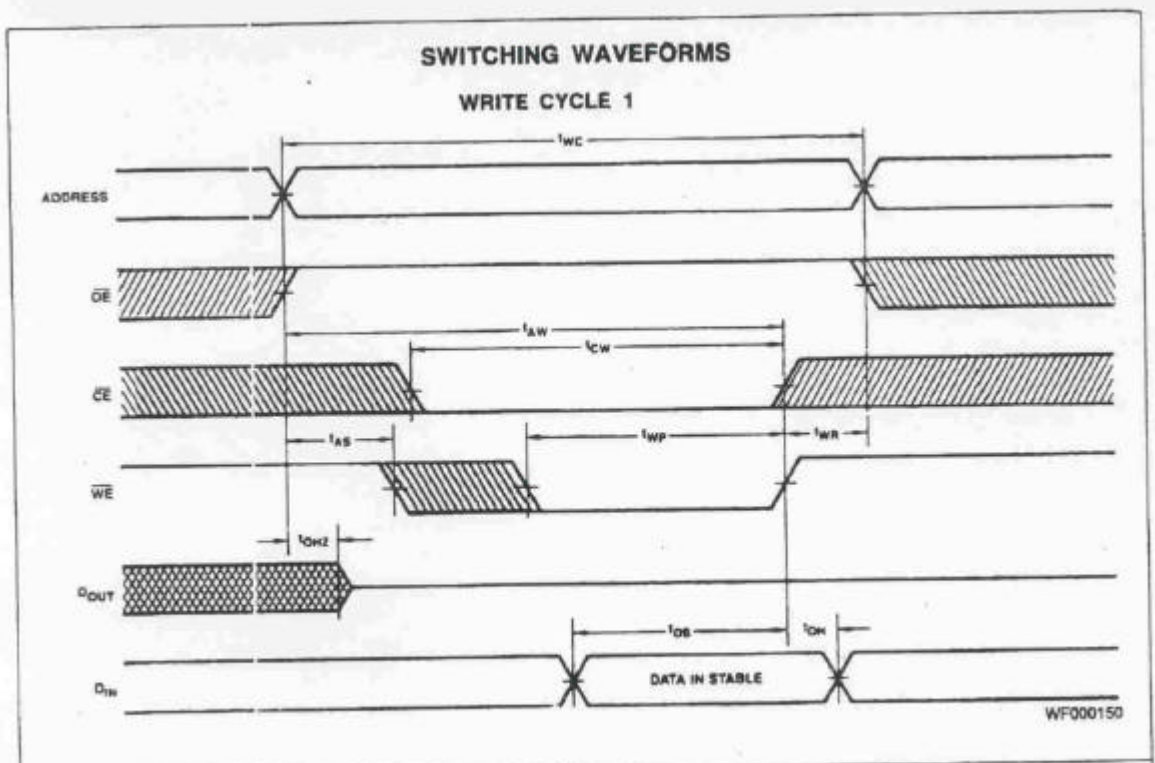
WF000130

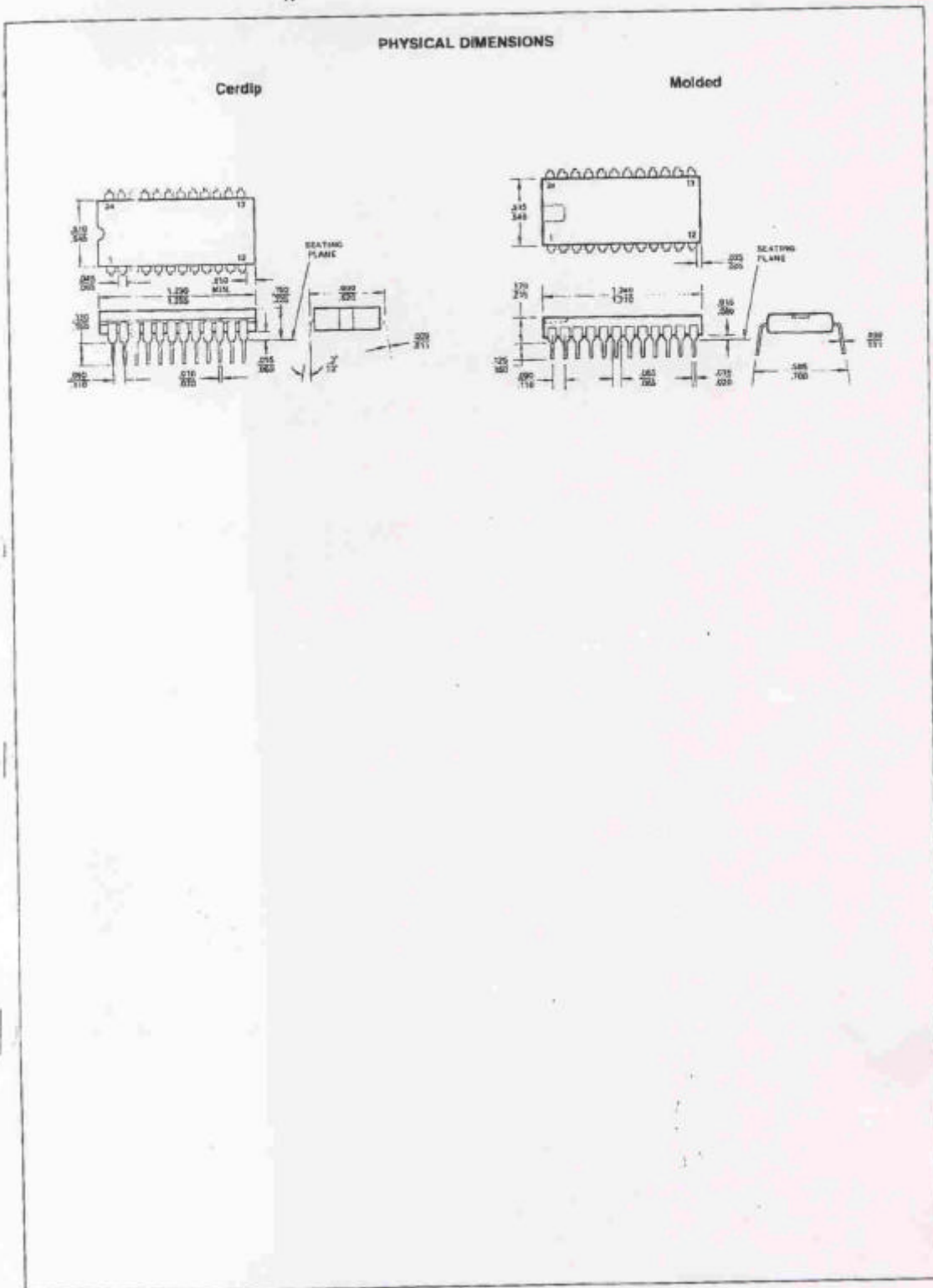
READ CYCLE 2 (Notes 5, 7, 8)



WF000140

Notes: See notes following DC Characteristics table.





5 **CERTIFICATE OF CONFORMITY**

All batches of parts shall be supplied with certificates of conformity. The certificate of conformity shall reference the test certificate.

5.1 **Force Technologies Certificate of Conformity**

Screening specified in section 4 of this document.
Force Technologies part number.

6 **PACKAGE DESCRIPTION**

24 pin Ceramic DIL dimensions to AMD Type CD024
Pin out to AMD part AM9128-20BJA
Part shall carry marking FT9128-20BJA-AMD (will exclude “-AMD” if space limited)

7 **TRACEABILITY (IF APPLICABLE)**

Traceability shall be provided by the date code printed on the top/bottom side of each device.
ISO9002 traceability procedures to apply using batch codes

COMPONENT SELECTION

8.1 **General**

No component or component supplier shall be changed without the express written consent of the customer, following the submission of evidence to justify that the replacement component will meet all required parameters, including radiation immunity.

8.2 Nuclear Hardness (Not applicable)

8.3 The baseline component:

Original Manufacturer:	AMD
Part number:	AM9128-20DC

The vendor shall determine that the die size, mask and if possible the manufacturing process has not changed since the manufacture of the baseline component. This shall be done prior to acceptance of any order by the vendor. If such a change has occurred, written notification shall be given to the customer the changes and possible alternatives. The vendor shall take no further action until a way forward has been agreed with the customer.

8.4 **Obsolescence**

Upon acceptance of an order the vendor becomes responsible for all component obsolescence until completion of that order. The vendor will inform customer of any PCN.

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