MN40013B/MN4013BS

## Dual D-Type Flip-Flop

■ Outline

The MN4013B/S has 2 built-in circuits of D-type flip-flops in one chip. The respective flip-flop has independent data, set, clear, and clock inputs and complementary outputs (O, $\overline{O}$).
The input applied to the data input is transmitted to the O output and $\overline{O}$ output at the rise of the clock pulse. The logic state is held to "H" or "L" by the clock level. This MN4013B/S is equivalent to Motorola's MC14013B and RCA's CD4013B.
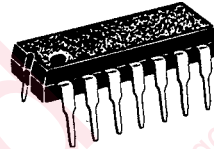
■ Trush Table

Input				Output	
S_D	C_D	CP	D	O_{n+1}	$\overline{O}_{n+1}$
H	L	×	×	H	L
L	H	×	×	L	H
H	H	×	×	H	H
L	L	⌐_	×	O_n	$\overline{O}_n$
L	L	_⌐	L	L	H
L	L	_⌐	H	H	L

Note) × : don't care

■ Logic Diagram
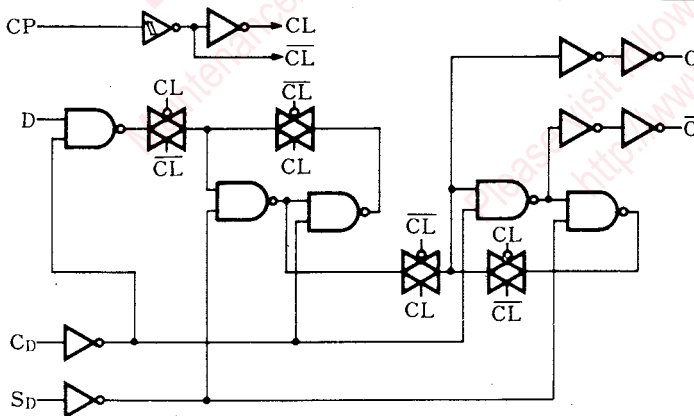
P-1

14-pin plastic DIL package

P-2
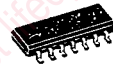
14-pin PANAFLAT package (SO-14D)

Pin Configuration

O_1	1	14 V_{DD}
$\overline{O}_1$	2	13 O_2
CP_1	3	12 $\overline{O}_2$
C_{D1}	4	11 CP_2
D_1	5	10 C_{D2}
S_{D1}	6	9 D_2
V_{SS}	7	8 S_{D2}

D-Type Flip-Flop (1)   D-Type Flip-Flop (2)
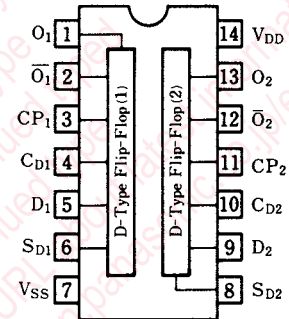
Pin description

S_D : Data set input
C_D : Data clear input
D : Data input
CP : Clock input
O, $\overline{O}$: Output (complementary)

Panasonic

■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Supply voltage		V_{DD}	$-0.5\sim+18$	V
Input voltage		V_I	$-0.5\sim V_{DD}+0.5*$	V
Output pin voltage		V_O	$-0.5\sim V_{DD}+0.5*$	V
Peak input · output pin current		$\pm I_I$	max. 10	mA
Power dissipation (per package)	Ta=$-40\sim+60$°C	P_D	max. 400	mW
	Ta=$+60\sim+80$°C		Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)		P_D	max. 100	mW
Operating ambient temperature		T_{opr}	$-40\sim+85$	°C
Storage temperature		T_{stg}	$-65\sim+150$	°C

＊ $V_{DD}+0.5V$ should be lower than 18V.

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Condition		Ta=-40°C min.	max.	Ta=25°C min.	max.	Ta=85°C min.	max.	Unit
Static supply current	5	I_{DD}	$V_I=V_{SS}$ or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output voltage low level	5	V_{OL}	$V_I=V_{SS}$ or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$|I_O|<1\mu$A		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V_{OH}	$V_I=V_{SS}$ or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$|I_O|<1\mu$A		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V_{IL}	$|I_O|<1\mu$A	$V_O=0.5V$ or $4.5V$	—	1.5	—	1.5	—	1.5	V
	10			$V_O=1V$ or $9V$	—	3	—	3	—	3	
	15			$V_O=1.5V$ or $13.5V$	—	4	—	4	—	4	
Input voltage high level	5	V_{IH}	$|I_O|<1\mu$A	$V_O=0.5V$ or $4.5V$	3.5	—	3.5	—	3.5	—	V
	10			$V_O=1V$ or $9V$	7	—	7	—	7	—	
	15			$V_O=1.5V$ or $13.5V$	11	—	11	—	11	—	
Output current low level	5	I_{OL}	$V_O=0.4V$, $V_I=0$ or $5V$		0.52	—	0.44	—	0.36	—	mA
	10		$V_O=0.5V$, $V_I=0$ or $10V$		1.3	—	1.1	—	0.9	—	
	15		$V_O=1.5V$, $V_I=0$ or $15V$		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	$V_O=4.6V$, $V_I=0$ or $5V$		0.52	—	0.44	—	0.36	—	mA
	10		$V_O=9.5V$, $V_I=0$ or $10V$		1.3	—	1.1	—	0.9	—	
	15		$V_O=13.5V$, $V_I=0$ or $15V$		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	$V_O=2.5V$, $V_I=0$ or $5V$		1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	$\pm I_I$	$V_I=0$ or $15V$		—	0.3	—	0.3	—	1	μA

■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output rise time (Fig. 1)	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time (Fig. 1)	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Minimum data set-up time	5	t_{su}	—	30	90	ns
	10		—	10	30	
	15		—	10	30	
Maximum clock rise time Maximum clock fall time	5	$tr\phi$, $tf\phi$	20	—	—	μs
	10		2.5	—	—	
	15		1	—	—	
Maximum clock frequency	5	f_{max}	6	12	—	MHz
	10		12	25	—	
	15		18	36	—	
Propagation time (Fig. 1) (CP-O, $\overline{O}$)	5	t_{PLH}	—	100	300	ns
	10		—	40	120	
	15		—	30	90	
Propagation time (Fig. 1) (CP-O, $\overline{O}$)	5	t_{PHL}	—	110	330	ns
	10		—	45	135	
	15		—	30	90	
Propagation time (Fig. 2) (C_D, S_D-O, $\overline{O}$)	5	t_{PLH}	—	135	405	ns
	10		—	50	150	
	15		—	35	105	
Propagation time (Fig. 2) (C_D, S_D-O, $\overline{O}$)	5	t_{PHL}	—	100	300	ns
	10		—	40	120	
	15		—	30	90	
Minimum clear pulse width (Fig. 2) Minimum pre-set pulse width	5	t_{WCD} t_{WSD}	—	45	135	ns
	10		—	20	60	
	15		—	20	60	
Input capacitance		C_I	—	—	7.5	pF

● Switching waveforms

Fig. 1 t_{TLH}, t_{PLH} (CO-O, $\overline{O}$)
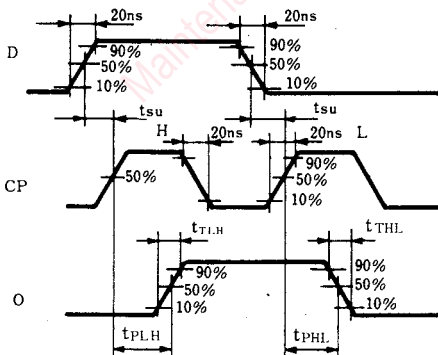
Fig. 2 t_{TLH}, (S_D-O, C_D-$\overline{O}$), t_{PLH} S_D-O, C_D-$\overline{O}$), t_{WCD}, t_{WSD}

Panasonic
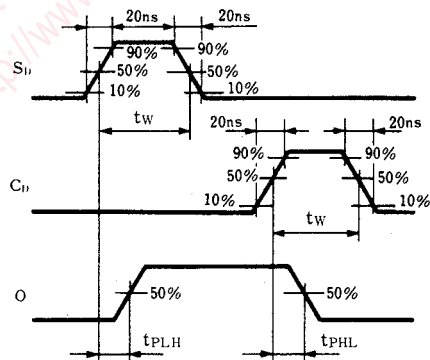
Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
    Consult our sales staff in advance for information on the following applications:
    ・Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
    ・Any applications other than the standard applications intended.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
    Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

(7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of our company.

20080805