Original

Am99C164/Am99CL164
Am99C165/Am99CL165

16,384 x 4 Static R/W Random-Access Memory

PRELIMINARY

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Fast access time – 35/45/55/70 ns maximum
- 16K x 4 organization
- Output Enable ($\overline{OE}$) control to alleviate bus-contention conditions (Am99C165)
- Single 5-V ±10% power-supply operation
- Fully static storage and interface circuitry
- Automatic power-down when deselected
- Low power dissipation
  - 550 mW operating power
  - 200 µW data retention
- 2-V data-retention capability
- 22-pin 0.300-inch DIP (Am99C164)
- 22-pin LCC (Am99C164)
- 24-pin 0.300-inch DIP (Am99C165)
- 28-Pin LCC (Am99C165)

GENERAL DESCRIPTION

The Am99C164 and Am99C165 are high-performance 16,384 x 4-bit static random-access memories (RAMs) manufactured with state-of-the-art CMOS processing techniques.

The Am99C164 device features common input/output pins and two control signals, $\overline{CE}$ and $\overline{WE}$. While $\overline{CE}$ controls read, write, and selection/deselection of the device, $\overline{WE}$ controls the write operation and output buffers only.

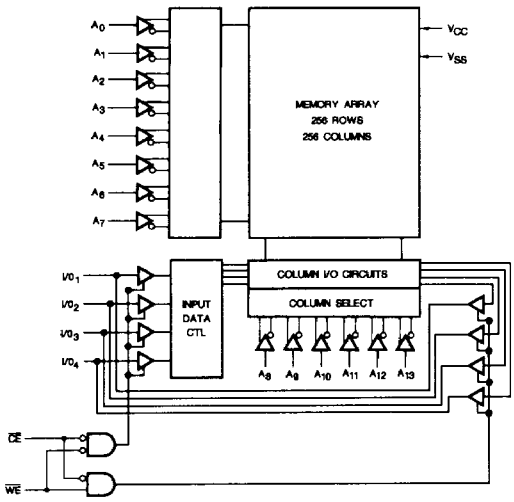
The Am99C165 device features three control signals ($\overline{CE}$, $\overline{WE}$, and $\overline{OE}$) to facilitate not only memory expansion, but also alleviate any bus-contention conditions which might limit high-performance read/write operation. While $\overline{WE}$ activates only the input buffers during a write cycle, $\overline{OE}$ activates only the output buffers during a read cycle. $\overline{CE}$ in the HIGH state deselects the entire device and reduces power consumption. All input/output interface levels are fully TTL-compatible for both the Am99C164 and Am99C165.

The Am99C164 and Am99C165 require a single 5-volt power supply while operating but can hold the data when power-supply level is maintained at a voltage as low as 2 volts.

The Am99C164 is available in 22-pin 0.300-inch wide ceramic and plastic DIPs, and 22-pin rectangular ceramic leadless chip carriers. The Am99C165 is available in 24-pin 0.300-inch wide ceramic and plastic DIPs, and 28-pin rectangular ceramic leadless chip carriers.

BLOCK DIAGRAM

Am99C164



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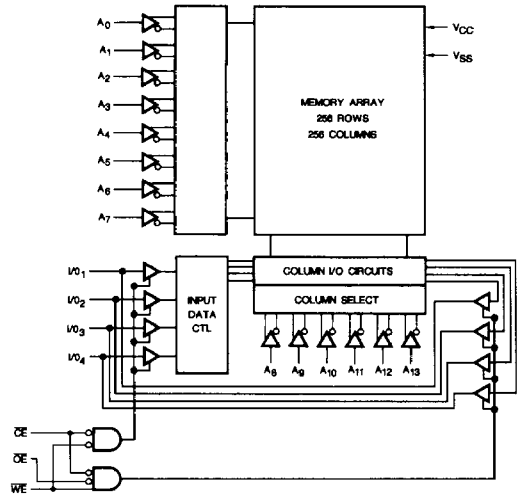
Am99C165



BD005712

3 Prior Orig

004781

Publication # 07437 | Rev. E | Amendment /0
Issue Date: June 1987

4781

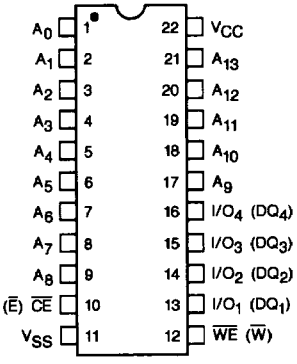
PRODUCT SELECTOR GUIDE

Family Part No.			Am99C164/Am99CL164 Am99C165/Am99CL165			
Ordering Part No.			-35	-45	-55	-70
Access Time (ns)			35	45	55	70
	Symbol	Power*				
Commercial (C) Devices: 0 to +70°C	I_{CC} (mA)	S	110	110	110	110
		L	105	95	90	90
	I_{SB1} (mA)	S	45	45	45	45
		L	25	25	25	25
	I_{SB2} (mA)	S	25	25	25	25
		L	20	20	20	20
	I_{SB3} (mA)	S	15	15	15	15
		L	0.3	0.3	0.3	0.3
	I_{CCDR} (mA) @ 2 V	S	–	–	–	–
		L	0.1	0.1	0.1	0.1
Extended Commercial (E) and Military (M) Devices -55 to +125°C	I_{CC} (mA)	S	–	120	120	120
		L	–	110	105	105
	I_{SB1} (mA)	S	–	50	50	50
		L	–	30	30	30
	I_{SB2} (mA)	S	–	35	35	35
		L	–	25	25	25
	I_{SB3} (mA)	S	–	20	20	20
		L	–	1.0	1.0	1.0
	I_{CCDR} (mA) @ 2 V	S	–	–	–	–
		L	–	0.3	0.3	0.3

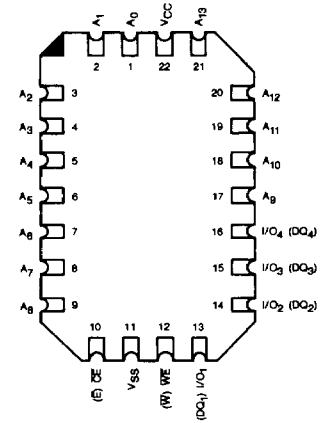
*S = Standard Power (Am99C164, Am99C165)
L = Low Power (Am99CL164, Am99CL165)

CONNECTION DIAGRAMS
Top View

Am99C164/Am99CL164



CD009921



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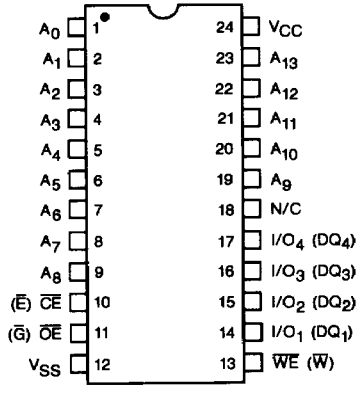
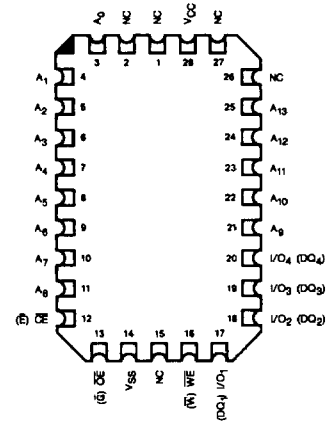
Note: Pin 1 is marked for orientation.

Am99C165/Am99CL165



CD009941



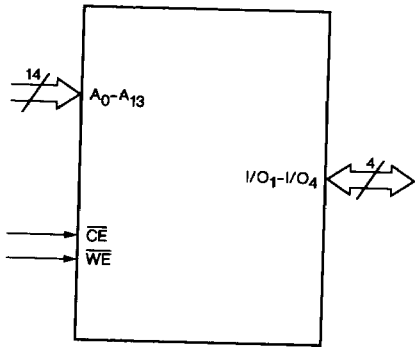
CD009951

Note: Pin 1 is marked for orientation.

IEEE Nomenclature in Brackets.

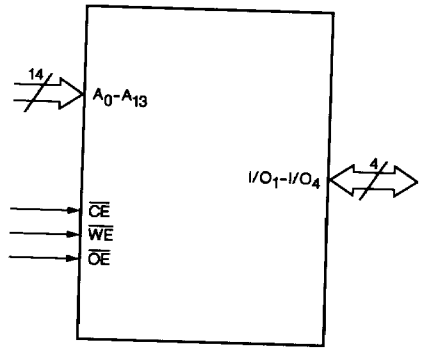
LOGIC SYMBOLS

Am99C164/Am99CL164



LS002660

Am99C165/Am99CL165



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Address Designators

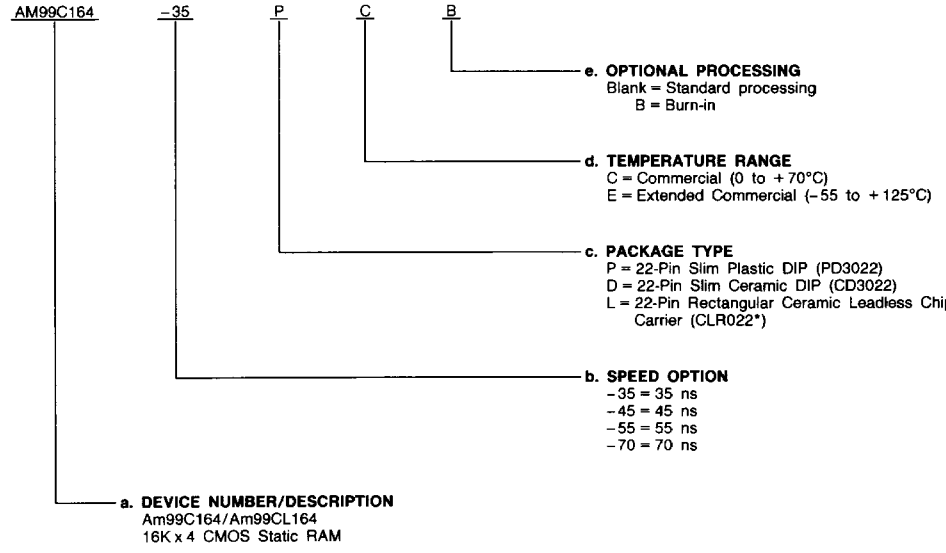
External	Internal*	Pin Number DIP Package
A_0	AX_5	1
A_1	AX_6	2
A_2	AX_3	3
A_3	AX_4	4
A_4	AX_7	5
A_5	AY_0	6
A_6	AY_1	7
A_7	AY_2	8
A_8	AY_3	9
A_9	AY_4	17, 19*
A_{10}	AY_5	18, 20*
A_{11}	AX_0	19, 21*
A_{12}	AX_2	20, 22*
A_{13}	AX_3	21, 23*

*For Am99C165, Am99CL165

ORDERING INFORMATION — Am99C164

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



*Preliminary. Subject to change.

Valid Combinations	
AM99C164-35	PC, PCB, DC, DCB, LC, LCB
AM99CL164-35	
AM99C164-45	PC, PCB, DC, DCB, DE, DEB, LC, LCB, LE, LEB
AM99CL164-45	
AM99C164-55	
AM99CL164-55	
AM99C164-70	
AM99CL164-70	

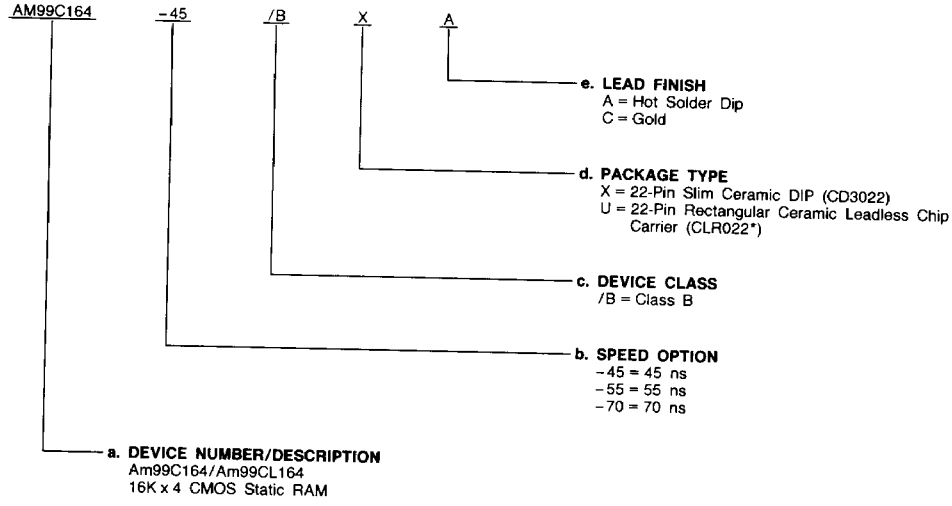
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION — Am99C164 (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



*Preliminary. Subject to change.

Valid Combinations	
AM99C164-45	/BXA, /BXC, /BUA
AM99CL164-45	
AM99C164-55	
AM99CL164-55	
AM99C164-70	
AM99CL164-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

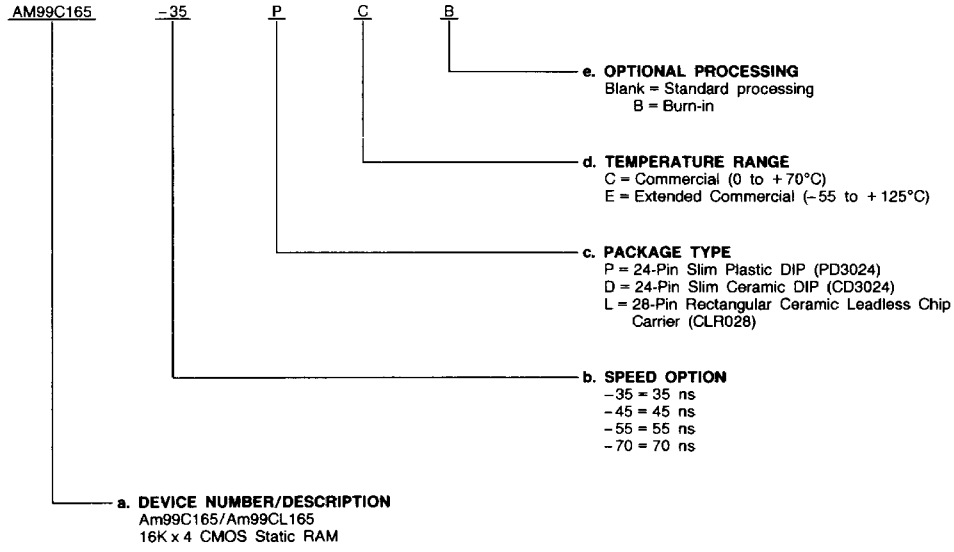
Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11

ORDERING INFORMATION — Am99C165

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM99C165-35	PC, PCB, DC, DCB, LC, LCB
AM99CL165-35	
AM99C165-45	PC, PCB, DC, DCB, DE, DEB, LC, LCB, LE, LEB
AM99CL165-45	
AM99C165-55	
AM99CL165-55	
AM99C165-70	
AM99CL165-70	

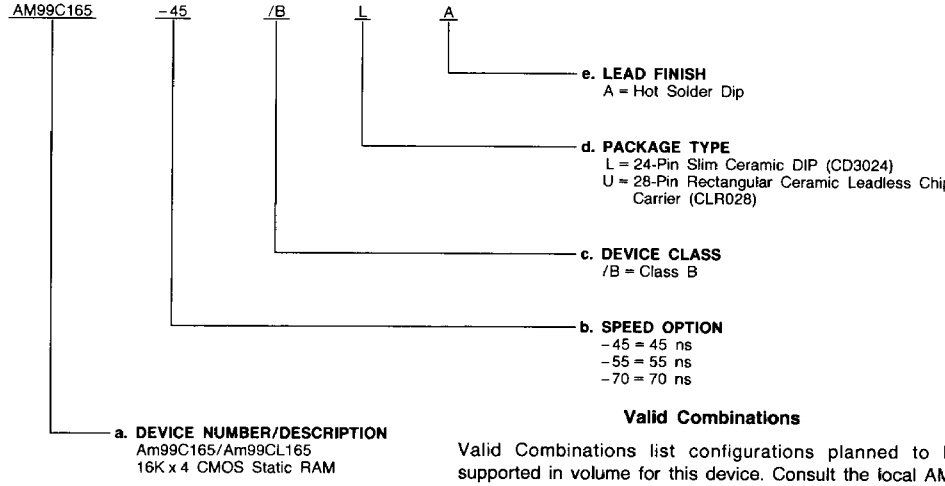
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION — Am99C165 (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM99C165-45	/BLA, /BUA
AM99CL165-45	
AM99C165-55	
AM99CL165-55	
AM99C165-70	
AM99CL165-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11

PIN DESCRIPTION

$A_0 - A_{13}$ Address Lines (Input)
The address input lines select the RAM location to be read from or written into.

$\overline{CE}$ Chip Enable (Input, Active LOW)
$\overline{CE}$ selects the memory device. $\overline{WE}$ is ignored when $\overline{CE}$ is HIGH.

$\overline{WE}$ Write Enable (Input, Active LOW)
When $\overline{WE}$ is LOW and $\overline{CE}$ is also LOW, data will be written into the location specified on the address pins. When $\overline{WE}$ is HIGH and $\overline{CE}$ is LOW (and $\overline{OE}$ is LOW for Am99C165) data will be read out and placed on the I/O pin.

$\overline{OE}$ Output Enable (Input, Active LOW)
When $\overline{OE}$ is LOW, it activates the output buffers during a read cycle, for Am99C165 only.

$I/O_1 - I/O_4$ Data In/Out Bus (Input/Output)
These I/O lines provide the path for data to be read from or written into the selected memory location.

V_{CC} +5-Volt Power Supply

V_{SS} 0-Volt Ground

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature
- Ceramic DIPs & LCCs ..... −65 to +150°C
- Plastic DIPs ..... −55 to +125°C

Ambient Temperature with Power Applied
- Ceramic DIPs & LCCs ..... −65 to +135°C
- Plastic DIPs ..... −10 to +85°C

DC Supply Voltage
- to Ground Potential Continuous ..... −0.5 to +7.0 V

All Signal Voltages ..... −0.5 to +7.0 V
DC Output Current ..... 20 mA
Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
- Temperature (T_A) ..... 0 to +70°C
- Supply Voltage (V_{CC}) ..... 4.5 to +5.5 V

Extended Commercial (E) and Military (M) Devices
- Temperature (T_A) ..... −55 to +125°C
- Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V	−4		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	8		mA
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 1.0	V
V_{IL}	Input LOW Voltage	Note 8	−0.5	0.8	V
$\lvert I_{IX} \rvert$	Input Load Current	$GND \leq V_{IN} \leq V_{CC}$		2.0	μA
$\lvert I_{OZ} \rvert$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, $\overline{CE} \geq V_{IH}$		2.0	μA

DC CHARACTERISTICS over Commercial (0 to +70°C) Operating Range*

Parameter Symbol	Parameter Description	Test Conditions	Power**	Am99C164/Am99CL164 Am99C165/Am99CL165 −35	−45	−55	−70	Unit
I_{CC}	Dynamic Operating Supply Current	Cycle = Min., Duty = 100%, $\overline{CE} \leq V_{IL}$, I/O = 0 mA	S	110	110	110	110	mA
			L	105	95	90	90	
I_{CC1}	Static Operating Supply Current	$\overline{CE} \leq V_{IL}$, I/O = 0 mA	S	80	80	80	80	mA
			L	60	60	60	60	
I_{SB1}	Standby Current, Cycling TTL Levels	$\overline{CE} \geq V_{IH}$; V_{CC} = Max., Cycle = Min.	S	45	45	45	45	mA
			L	25	25	25	25	
I_{SB2}	Standby Current, Stable TTL Levels	$\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$	S	25	25	25	25	mA
			L	20	20	20	20	
I_{SB3}	Standby Current, Stable CMOS Input Levels	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $\leq$ 0.2 V	S	15	15	15	15	mA
			L	0.3	0.3	0.3	0.3	

Notes: See notes following Capacitance table on the following page.

*All values are guaranteed maximum limits.
**S = Standard Power (Am99C164/Am99C165)
L = Low Power (Am99CL164/Am99CL165)

DC CHARACTERISTICS over Extended Commercial and Military (−55 to +125°C) Operating Ranges*

Parameter Symbol	Parameter Description	Test Conditions	Power**	Am99C164/Am99CL164 Am99C165/Am99CL165			Unit
				−45	−55	−70	
I_{CC}	Dynamic Operating Supply Current	Cycle = Min., Duty = 100%, $\overline{CE} \leq V_{IL}$, I/O = 0 mA	S	120	120	120	mA
			L	110	105	105	
I_{CC1}	Static Operating Supply Current	$\overline{CE} \leq V_{IL}$, I/O = 0 mA	S	100	100	100	mA
			L	80	80	80	
I_{SB1}	Standby Current, Cycling TTL Levels	$\overline{CE} \geq V_{IH}$, V_{CC} = Max., Cycle = Min.	S	50	50	50	mA
			L	30	30	30	
I_{SB2}	Standby Current, Stable TTL Levels	$\overline{CE} \geq V_{IH}$, $V_{IN} = V_{IH}$ or $\leq V_{IL}$	S	35	35	35	mA
			L	25	25	25	
I_{SB3}	Standby Current, Stable CMOS Input Levles	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $\leq$ 0.2 V	S	20	20	20	mA
			L	1.0	1.0	1.0	

*All values are guaranteed maximum limits.
**S = Standard Power (Am99C164/Am99C165)
L = Low Power (Am99CL164/Am99CL165)

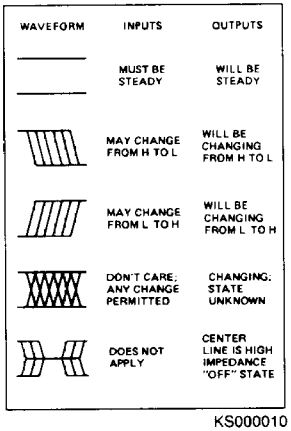
CAPACITANCE†

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_I ††	Input Capacitance Except $\overline{CE}$	f = 1 MHz, V_{IN} = 0 V		7	pF
C_O ††	Output Capacitance	V_{OUT} = 0 V		7	
$\overline{CE}$ ††	Chip Enable Input Capacitance	f = 1 MHz, V_{IN} = 0 V		7.5	pF

† These capacitances are not 100% tested, but are evaluated at initial characterization and at any time the product is modified where capacitance may be affected. Measurement performed at T_A = +25°C.
†† = Not included in Group A tests.

Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, operating temperature is defined as the "instant-on" case temperature.
3. Parameter not tested—guaranteed by characterization.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input-pulse levels of 0 to 3.0 V, and output loading of specified I_{OL}/I_{OH} and 30-pF load capacitance. Output timing reference is 1.5 V (see Test Load A in Switching Test Circuits section).
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ LOW. Both signals must be active to initiate a write and either signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the transition edge that terminates the write.
6. The minimum limit is not tested and is included for design information only.
7. Parameter not tested, guaranteed by characterization using the load shown in Test Load B—Switching Test Circuits. Transition is measured ±500 mV from steady state voltage.
8. Undershoot to −3.0 V for a duration of 10 ns between the 50% amplitude points is permissible.
9. Address input rise and fall times must not exceed 1 μs when $\overline{CE}$ is active. This limit is not tested and is intended for design information only.

KEY TO SWITCHING WAVEFORMS



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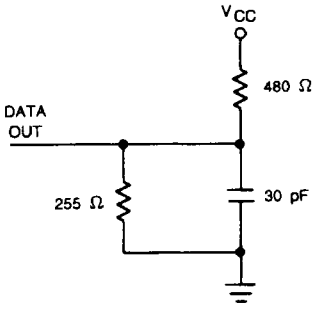
SWITCHING TEST CIRCUITS



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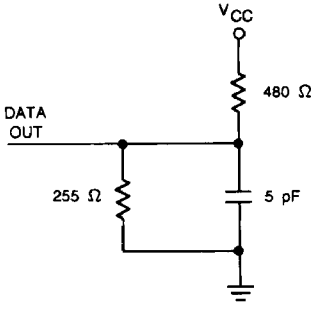
Test Load A



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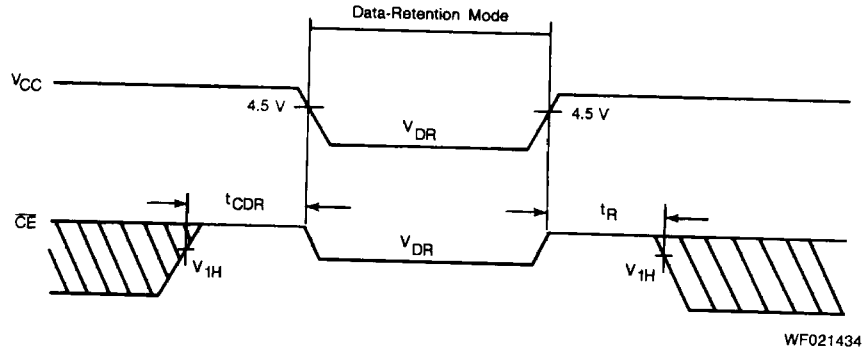
Test Load B

SWITCHING TEST WAVEFORM



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Low V_{CC} Data Retention Characteristics (Low-Power Version Only)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CE} \geq V_{CC} - 0.2$ V		2.0		V
I_{CCDR}	Data Retention Current	V_{CC} = 2 V	COM'L		0.1	mA
			MIL		0.3	
I_{CCDR}	Data Retention Current	V_{CC} = 3 V	COM'L		0.15	mA
			MIL		0.45	
t_{CDR}	Chip Deselect to Data Retention Time (Note 1)	See Waveform (Note 2)		0		ns
t_R	Operating Recovery Time (Note 1)			t_{RC}		ns

Notes: 1. Parameter not tested, guaranteed by design.
2. Waveforms shown are not actual and may vary in use.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 7, 8, 9 10, 11 are tested unless otherwise noted)

No.	Parameter Symbols		Parameter Description	Am99C164/Am99CL164 Am99C165/Am99CL165								Units
				-35		-45		-55		-70		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLES ONE, TWO, AND THREE (Note 9)												
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		35		45		55		70	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	35		45		55		70		ns
3	t_{AVQV}	t_{AA}	Address Access Time		35		45		55		70	ns
4	t_{AXQX}	t_{OH}	Output Hold After Address	5		5		5		5		ns
5†	t_{ELQX}	t_{LZ}	Chip Enable to Output Active (Note 7)	5		5		5		5		ns
6†	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable (Note 7)		15		15		20		25	ns
7†	t_{ELICCH}	t_{PU}	Chip Enable to Power Up (Note 3)	0		0		0		0		ns
8†	t_{EHICCL}	t_{PD}	Chip Disable to Power Down (Note 3)	0	35	0	45	0	55	0	70	ns
WRITE CYCLES ONE AND TWO (Note 9)												
9†	t_{AVAV}	t_{WC}	Write Cycle Time	35		45		55		70		ns
10†	t_{WLWH}	t_{WP}	Write Pulse Width (Note 5)	30		40		50		60		ns
11†	t_{ELWH}	t_{CW}	Chip Enable to End of Write (Note 5)	35		40		50		60		ns
12	t_{DVWH}	t_{DW}	Data Setup to End of Write	20		25		30		30		ns
13†	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns
14†	t_{AVWH}	t_{AW}	Address Setup to End of Write (Note 5)	30		40		50		60		ns
15	t_{AVWL}	t_{AS}	Address Setup to Beginning of Write	0		0		0		0		ns
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns
17†	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable (Notes 6 & 7)	0	10	0	15	0	20	0	25	ns
18†	t_{WHQX}	t_{OW}	Output Active After End of Write (Notes 6 & 7)	5		5		5		5		ns
19†	t_{GLQV}	t_{OE}	Output Enable Access Time (Am99C165/ Am99CL165 only)		15		20		25		30	ns

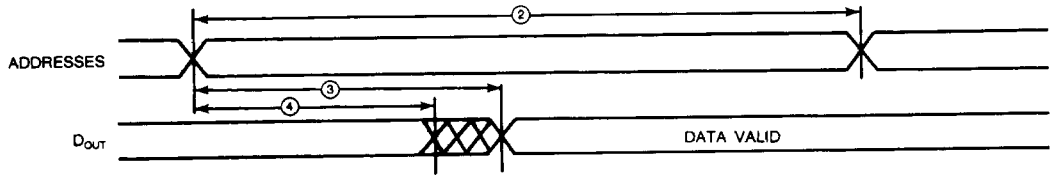
SWITCHING CHARACTERISTICS (Cont'd.)

No.	Parameter Symbols		Parameter Description	Am99C164/Am99CL164 Am99C165/Am99CL165								Units
				-35		-45		-55		-70		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
20†	t_{GLQX}	t_{OLZ}	Output Enable to Output Active (Am99C165/ Am99CL165 only) (Note 7)	5		5		5		5		ns
21†	t_{GHQZ}	t_{OHZ}	Output Enable to Output Disable (Am99C165/ Am99CL165 only) (Note 7)	0	15	0	15	0	15	0	15	ns

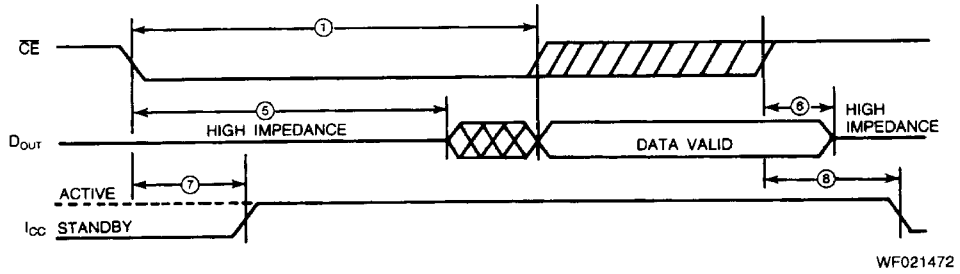
Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, operating temperature is defined as the "instant-on" case temperature.
3. Parameter not tested—guaranteed by characterization.
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input-pulse levels of 0 to 3.0 V, and output loading of specified I_{OL}/I_{OH} and 30-pF load capacitance. Output timing reference is 1.5 V (see Test Load A in Switching Test Circuits section).
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ LOW. Both signals must be active to initiate a write and either signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the transition edge that terminates the write.
6. The minimum limit is not tested and is included for design information only.
7. Parameter not tested, guaranteed by characterization using the load shown in Test Load B—Switching Test Circuits. Transition is measured ±500 mV from steady state voltage.
8. Undershoot to −3.0 V for a duration of 10 ns between the 50% amplitude points is permissible.
9. Address input rise and fall times must not exceed 1 μs when $\overline{CE}$ is active. This limit is not tested and is intended for design information only.

† Not included in Group A tests

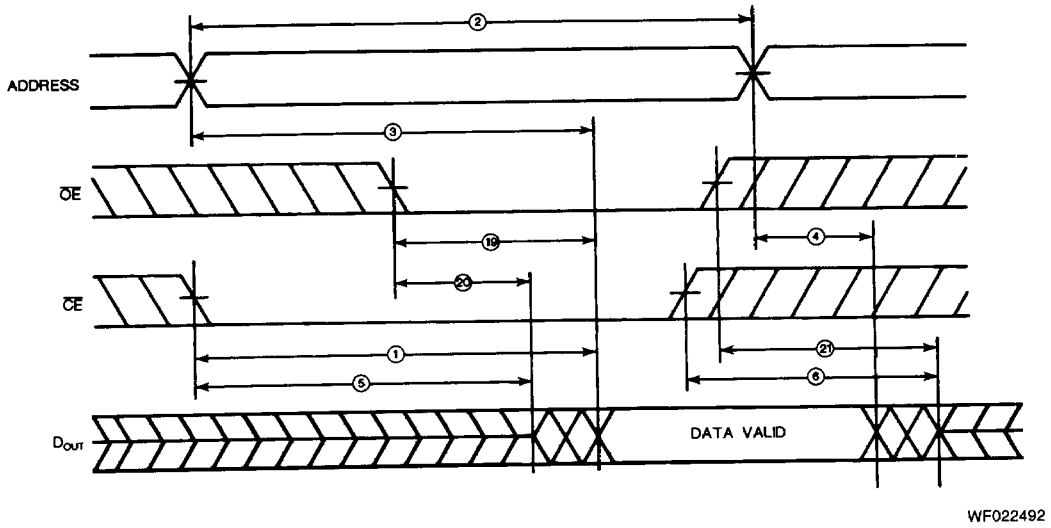
SWITCHING WAVEFORMS



Read Cycle One (Notes 1, 2, & 4)



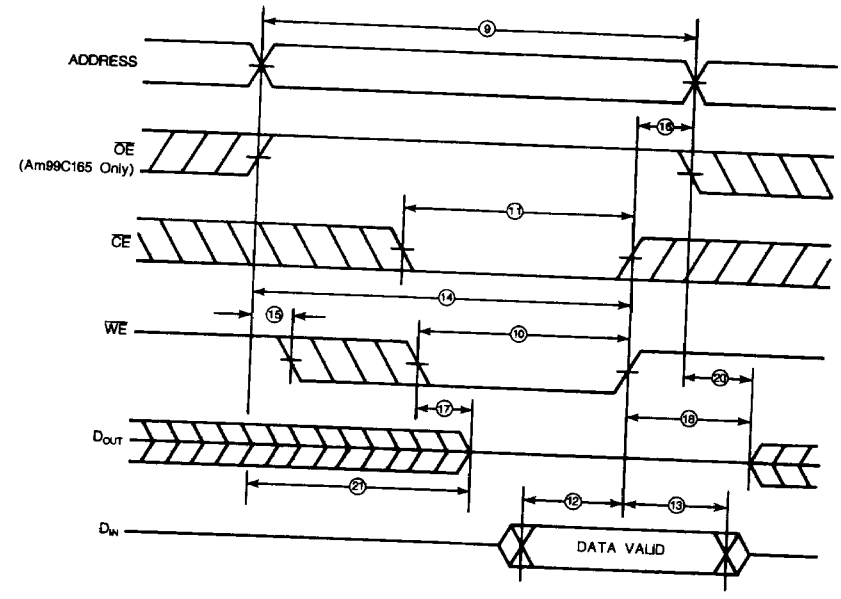
Read Cycle Two (Notes 1, 3, & 4)



Read Cycle Three (Notes 1 & 3)
(Am99C165/Am99CL165 Only)

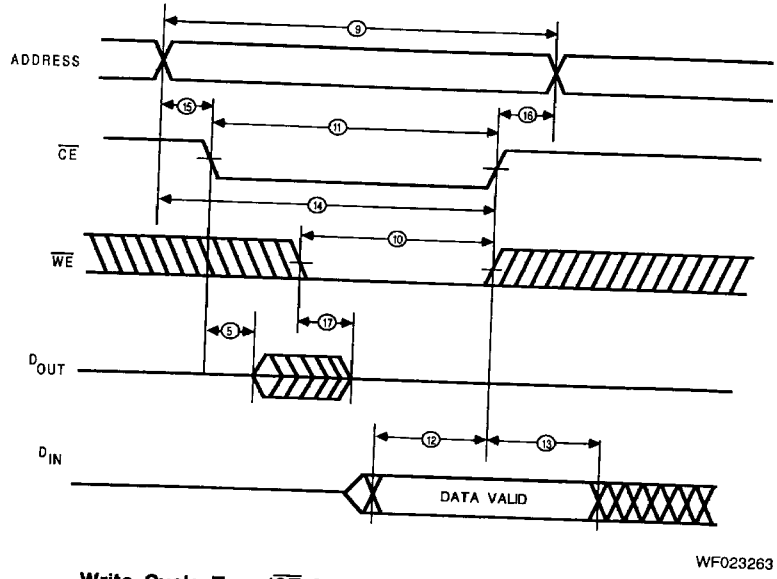
Notes: 1. $\overline{WE}$ is HIGH for Read Cycle.
2. $\overline{CE}$ is LOW for Read Cycle.
3. Address Valid prior to or coincident with $\overline{CE}$ transition LOW.
4. $\overline{OE} = V_{IL}$ (Am99C165/Am99CL165 only)

SWITCHING WAVEFORMS (Cont'd.)



WF022503

Write Cycle One ($\overline{WE}$-Controlled) (Notes 1 & 3)



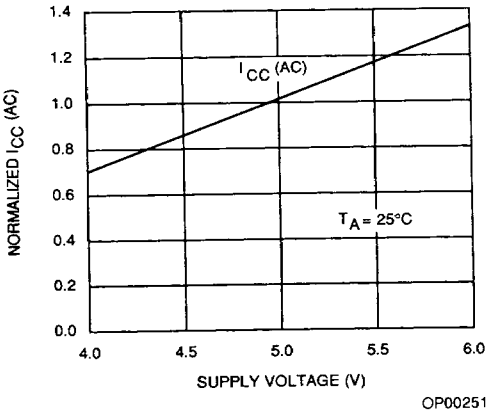
WF023263

Write Cycle Two ($\overline{CE}$-Controlled) (Notes 1, 2, & 3)

Notes: 1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. $\overline{OE}$ is continuously LOW ($\overline{OE} = V_{IL}$) for Am99C165.
3. If $\overline{CE}$ LOW transition occurs simultaneously with $\overline{WE}$ LOW transition or after $\overline{WE}$ transition, outputs remain in a high-impedance state.

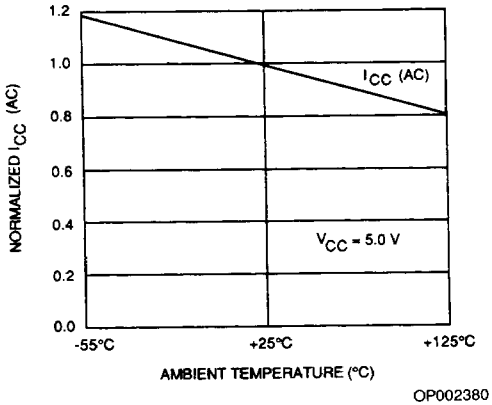
TYPICAL PERFORMANCE CURVES

NORMALIZED SUPPLY CURRENT
vs SUPPLY VOLTAGE



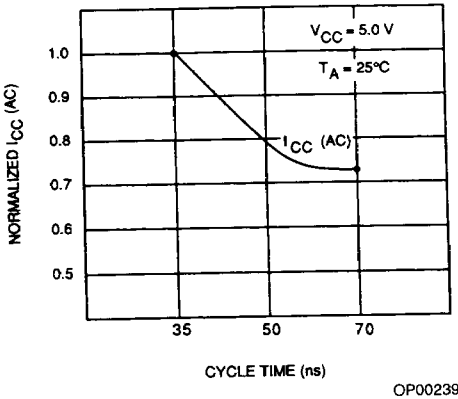
OP002510

NORMALIZED SUPPLY CURRENT
vs AMBIENT TEMPERATURE



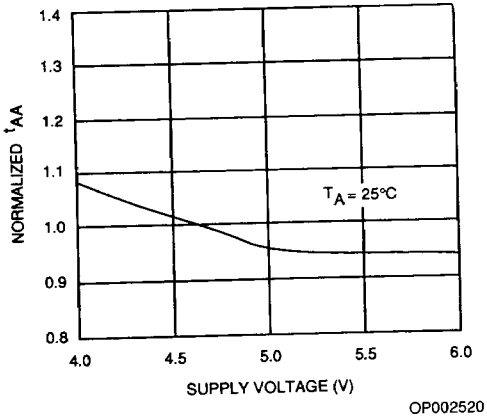
OP002380

NORMALIZED I_{CC} (AC)
vs CYCLE TIME



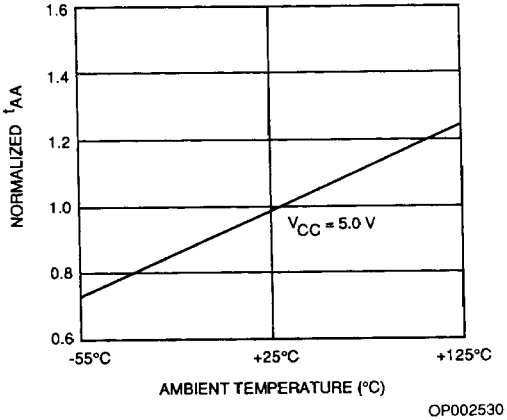
OP002390

NORMALIZED ACCESS TIME
vs SUPPLY VOLTAGE



OP002520

NORMALIZED ACCESS TIME
vs AMBIENT TEMPERATURE

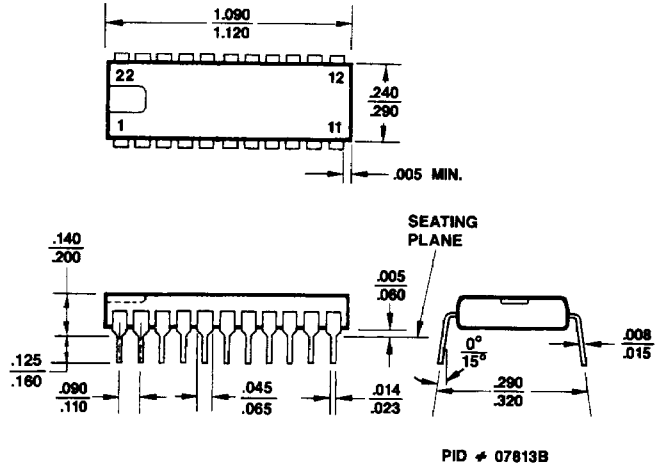


OP002530

PHYSICAL DIMENSIONS*

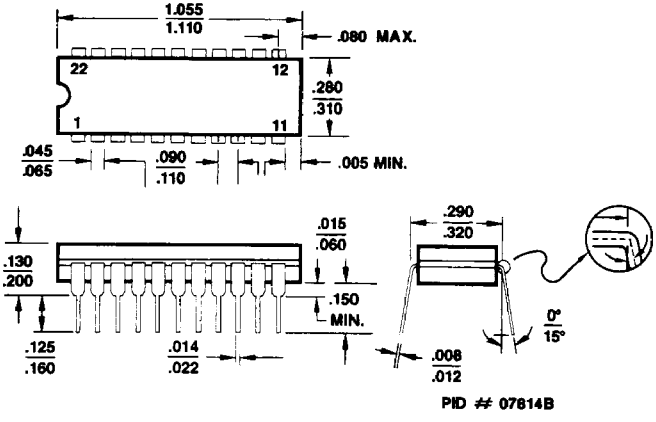
Am99C164

PD3022



PID # 07813B

CD3022

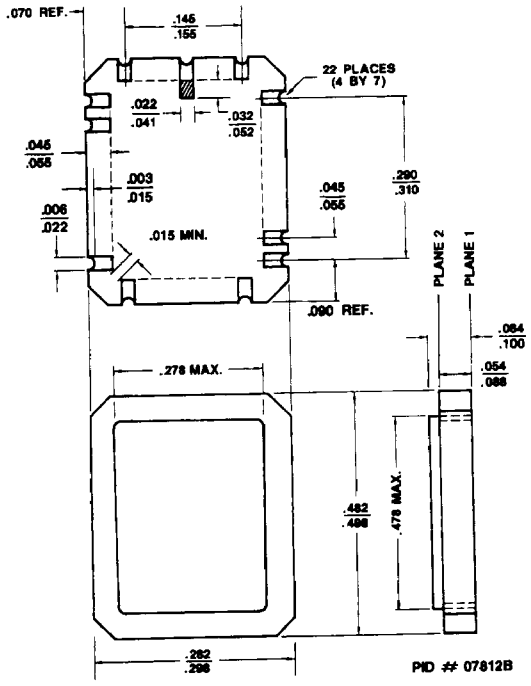


PID # 07814B

*For reference only.

PHYSICAL DIMENSIONS (Cont'd.)

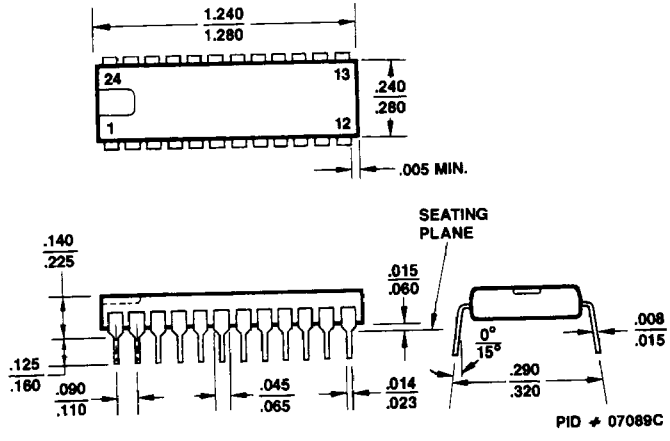
CLR022*



*Preliminary; subject to change.

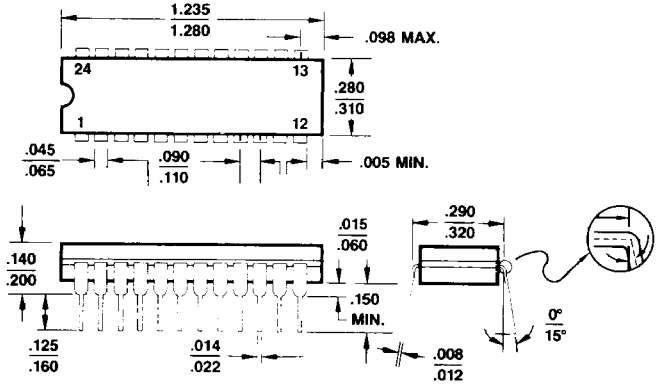
Am99C165

PD3024



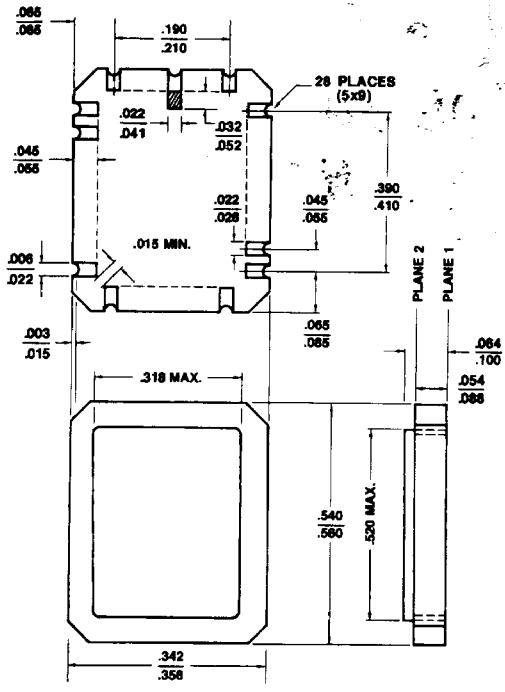
PHYSICAL DIMENSIONS (Cont'd.)

CD3024



PID # 06850B

CLR028



PID # 06852B

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