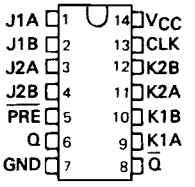
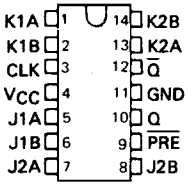
REVISED DECEMBER 1983

- **Package Options Include Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54H101 . . . J PACKAGE
SN74H101 . . . J OR N PACKAGE
(TOP VIEW)



SN54H101 . . . W PACKAGE
(TOP VIEW)



description

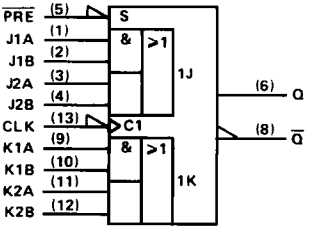
These monolithic J-K flip-flops are negative-edge-triggered. The AND-OR gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

The SN54H101 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74H101 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

logic symbol



Pin numbers shown are for J and N packages.

positive logic

$$J = (J1A \cdot J1B) + (J2A \cdot J2B)$$

$$K = (K1A \cdot K1B) + (K2A \cdot K2B)$$

PRODUCTION DATA
This document contains information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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