

# Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

# **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

# **Quad D Flip-Flop**

The LSTTL/MSI SN74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Clock to Output Delays of 30 ns
- Asynchronous Common Reset
- True and Complement Output
- Input Clamp Diodes Limit High Speed Termination Effects

#### **GUARANTEED OPERATING RANGES**

Symbol	Parameter	Min	Тур	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	ŷ
I <sub>OH</sub>	Output Current - High			-0.4	mA
l <sub>OL</sub>	Output Current - Low			8.0	mA



### ON Semiconductor™

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# LOW POWER SCHOTTKY



PLASTIC N SUFFIX CASE 648



SOIC D SUFFIX CASE 751B



SOEIAJ M SUFFIX CASE 966

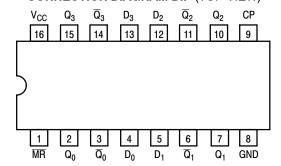
#### **ORDERING INFORMATION**

Device	Package	Shipping
SN74LS175N	16 Pin DIP	2000 Units/Box
SN74LS175D	SOIC-16	38 Units/Rail
SN74LS175DR2	SOIC-16	2500/Tape & Reel
SN74LS175M	SOEIAJ-16	See Note 1
SN74LS175MEL	SOEIAJ-16	See Note 1

 For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

1

#### **CONNECTION DIAGRAM DIP (TOP VIEW)**



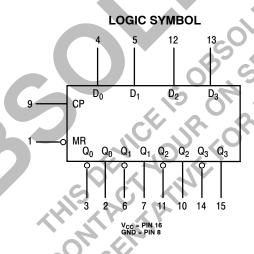
NOTE:

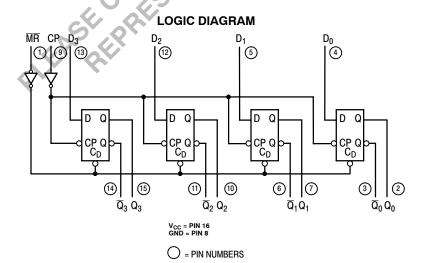
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

	_	LOADING	(Note a)
PIN NAMES		HIGH	LOW
D <sub>0</sub> - D <sub>3</sub>	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_3$	True Outputs	10 U.L.	5 U.L.
$\overline{Q}_0 - \overline{Q}_3$	Complemented Outputs	10 U.L.	5 U.L.

#### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.





#### **FUNCTIONAL DESCRIPTION**

The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and  $\overline{Q}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and  $\overline{Q}$  outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and  $\overline{Q}$  outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

#### **TRUTH TABLE**

Inputs (t = n, MR = H)	Outputs (t =	n+1) Note 1
D	Q	Q
L	L	Н
Н	Н	L

Note 1: t = n + 1 indicates conditions after next clock.

#### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

		Limits			ΛΟ,		
Symbol	Parameter	Min	Тур	Max	Unit	Tes	t Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Inpu All Inputs	t LOW Voltage for
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	CV	V <sub>CC</sub> = MIN, I <sub>IN</sub> =	–18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5	O	V	$V_{CC} = MIN, I_{OH} = $ or $V_{IL}$ per Truth 1	= MAX, V <sub>IN</sub> = V <sub>IH</sub> Table
.,			0.25	0.4	V	I <sub>OL</sub> = 4.0 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN,
$V_{OL}$	Output LOW Voltage		0.35	0.5	V	I <sub>OL</sub> = 8.0 mA	<ul> <li>V<sub>IN</sub> = V<sub>IL</sub> or V<sub>IH</sub> per Truth Table</li> </ul>
	1			20	μΑ	$V_{CC} = MAX, V_{IN}$	= 2.7 V
I <sub>IH</sub>	Input HIGH Current		1	0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub>	= 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	$V_{CC} = MAX, V_{IN}$	= 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 2)	-20	10	-100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current	77	77	18	mA	V <sub>CC</sub> = MAX	
. Not more th	an one output should be shorted at a t	ijme, n <b>o</b> r t	for more t	than 1 sec	cond.		

<sup>2.</sup> Not more than one output should be shorted at a time, nor for more than 1 second.

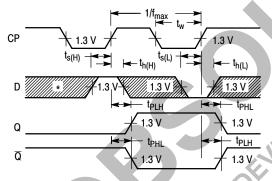
#### AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

		Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
f <sub>MAX</sub>	Maximum Input Clock Frequency	30	40		MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, MR to Output		20 20	30 30	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		13 16	25 25	ns	-1 17 [

#### AC SETUP REQUIREMENTS $(T_A = 25^{\circ}C)$

			Limits			
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
t <sub>W</sub>	Clock or MR Pulse Width	20			ns	
ts	Data Setup Time	20			ns	V 50V
t <sub>h</sub>	Data Hold Time	5.0			ns	V <sub>CC</sub> = 5.0 V
t <sub>rec</sub>	Recovery Time	25			ns	.0%

#### **AC WAVEFORMS**



<sup>\*</sup>The shaded areas indicate when the input is permitted to change for predictable output performance.

The state of the s

Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock

#### **DEFINITIONS OF TERMS**

SETUP TIME  $(t_s)$  — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

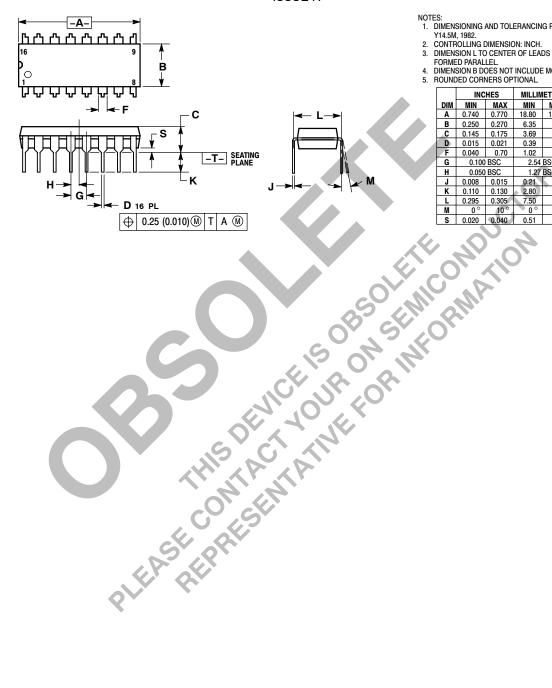
HOLD TIME (t<sub>h</sub>) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME ( $t_{rec}$ ) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

#### PACKAGE DIMENSIONS

#### **N SUFFIX** PLASTIC PACKAGE CASE 648-08 **ISSUE R**



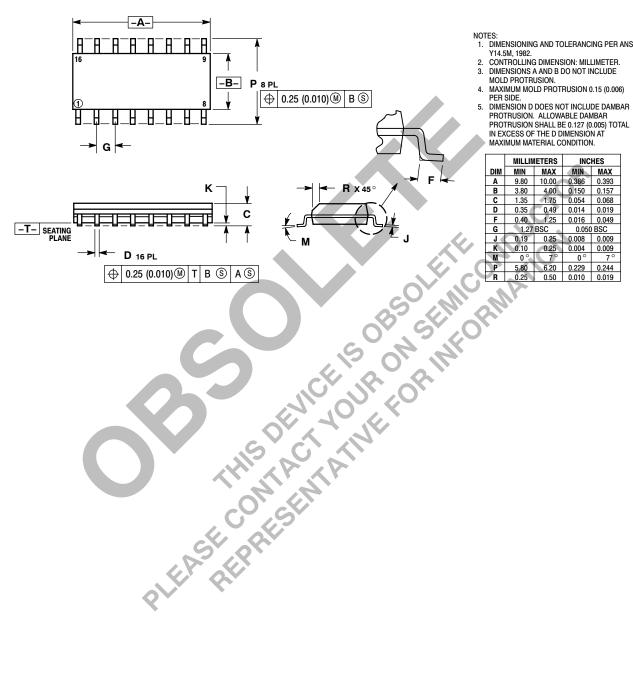
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN
- FORMED PARALLEL.
  DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
Ç	0.145	0.175	3.69	4.44	
Ê	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27	BSC	
7	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10°	0 °	10 °	
S	0.020	0.040	0.51	1.01	

#### PACKAGE DIMENSIONS

#### **D SUFFIX**

PLASTIC SOIC PACKAGE CASE 751B-05 **ISSUE J** 



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- Y14.5M, 1982.

  CONTROLLING DIMENSION: MILLIMETER.

  DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

  MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

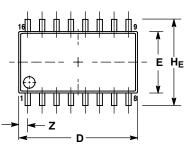
  DIMENSION D DOES NOT INCLUDE DAMBAR
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

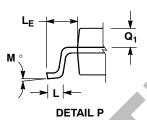
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J∢	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
Р	0.25	0.50	0.010	0.010

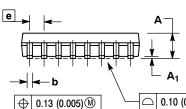
#### PACKAGE DIMENSIONS

#### **M SUFFIX**

SOEIAJ PACKAGE CASE 966-01 ISSUE O









#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

MILLIMETERS		INC	HES
MIN	MAX	MIN	MAX
	2.05		0.081
0.05	0.20	0.002	0.008
0.35	0.50	0.014	0.020
0.18	0.27	0.007	0.011
9.90	10.50	0.390	0.413
5.10	5.45	0.201	0.215
1.27	BSC	0.050 BSC	
7.40	8.20	0.291	0.323
0.50	0.85	0.020	0.033
1.10	1.50	0.043	0.059
0 °	10 °	0 °	10°
0.70	0.90	0.028	0.035
	0.78		0.031
	MIN 0.05 0.35 0.18 9.90 5.10 1.27 7.40 0.50 1.10 0 °	MIN MAX 2.05 0.05 0.20 0.35 0.50 0.18 0.27 9.90 10.50 5.10 5.45 1.27 BSC 7.40 8.20 0.50 0.85 1.10 1.50 0 0 10 0 0.70 0.90	MIN   MAX   MIN

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