

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

D3042, AUGUST 1987—REVISED MAY 1990

- Meets EIA Standards RS-422A and RS-485, CCITT Recommendations V.11 and X.27, and ISO 8482:1987(E)
- Designed and Tested for Data Rates up to 35 Mbaud
- SN65ALS176 Operating Temperature – 40°C to 85°C
- Three Skew Limits Available:
 - ALS176 . . . 10 ns
 - ALS176A . . . 7.5 ns
 - ALS176B . . . 5 ns
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements
30 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fall-Safe Design

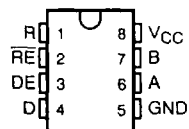
description

The SN65ALS176 and SN75ALS176 series Differential Bus Transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet EIA Standards RS-422-A and RS-485, CCITT recommendations V.11 and X.27, and ISO 8482:1987(E).

The SN65ALS176 and SN75ALS176 series combine a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from – 40°C to 85°C and the SN75ALS176 series is characterized for operation from 0°C to 70°C.

D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLE (DRIVER)

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2V$	L	H
$-0.2V < V_{ID} < 0.2V$	L	?
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

AVAILABLE OPTIONS

T _A	t _{pmax} - t _{pmin} t _{sk(1)} †	PACKAGE	
		SMALL OUTLINE (D)†	PLASTIC DIP (P)
0°C to 70°C	10 7.5 5	SN75ALS176D SN75ALS176AD SN75ALS176BD	SN75ALS176P SN75ALS176AP SN75ALS176BP
-40°C to 85°C	10	SN65ALS176D	SN65ALS176P

† The D package is available taped and reeled. Add the suffix R to the device type, (e.g., SN75ALS176DR).

‡ t_{sk(1)} is the greater of 1) the difference between the maximum and minimum specified values of t_{PLH} of (t_{DDH}), and 2) the difference between the maximum and minimum specified values of t_{pHL} (or t_{DDL}). This is the maximum range that the driver or receiver delay time will vary over temperature, V_{CC}, and device-to-device.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

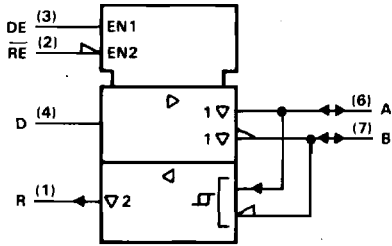
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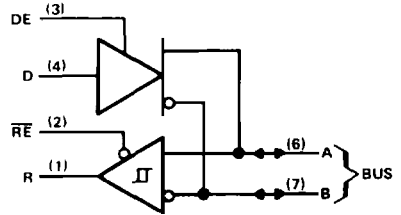
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SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

logic symbol†

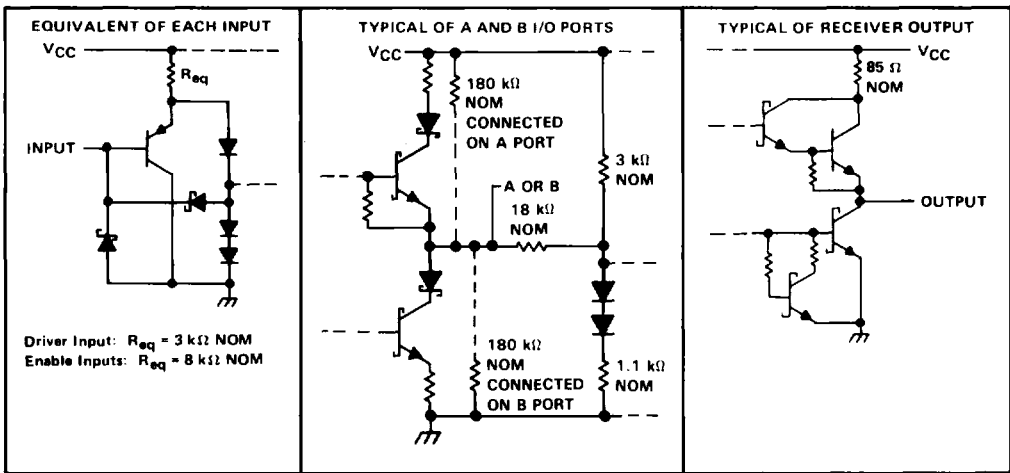


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage at any bus terminal	-10 V to 15 V
Enable input voltage	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN65ALS176	-40°C to 85°C
SN75ALS176 Series	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
	POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING	POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		12			V
		-7			
High-level input voltage, V_{IH}	D, DE, and RE	2			V
Low-level input voltage, V_{IL}	D, DE, and RE	0.8			V
Differential input voltage, V_{ID} (see Note 2)		± 12			V
High-level output current, I_{OH}	Driver	-60			mA
	Receiver	-400			μA
Low-level output current, I_{OL}	Driver	60			mA
	Receiver	8			
Operating free-air temperature, T_A	SN65ALS176	-40	85		°C
	SN75ALS176	0	70		

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_O Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$, See Figure 1	$1/2 V_{OD1}$			
	$R_L = 54 \Omega$, See Figure 1	1.5	2.5	5	V
V_{OD3} Differential output voltage	$V_{test} = -7 \text{ V to } 12 \text{ V}$, See Figure 2	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage §	$R_L = 54 \Omega$ or 100Ω , See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage				3 -1	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage §				± 0.2	V
I_O Output current	Output disabled, See Note 3	$V_O = 12 \text{ V}$		1	mA
		$V_O = -7 \text{ V}$		-0.8	
I_{IH} High-level input current	$V_I = 2.4 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_I = 0.4 \text{ V}$			-400	μA
I_{OS} Short-circuit output current ¶	$V_O = -6 \text{ V}$	SN65ALS176		-250	mA
	$V_O = -7 \text{ V}$	SN75ALS176			
	$V_O = 0$	All		-150	
	$V_O = V_{CC}$	All		250	
	$V_O = 8 \text{ V}$	SN65ALS176			
$V_O = 12 \text{ V}$	SN75ALS176				
I_{CC} Supply current	No load	Outputs enabled	23	30	mA
		Outputs disabled	19	26	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

¶ Duration of the short circuit should not exceed one second.

NOTE 3: This applies for both power on and off; refer to EIA standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

driver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{DD}	Differential output delay time				15	ns
t _{sk(p)}	Pulse skew (t _{DDL} - t _{DDH})	R _L = 54 Ω, C _L = 50 pF, See Figure 3		0	2	ns
t _{TD}	Differential output transition time			8		ns
t _{PZH}	Output enable time to high level	R _L = 110 Ω, C _L = 50 pF, See Figure 4			80	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω, C _L = 50 pF, See Figure 5			30	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω, C _L = 50 pF, See Figure 4			50	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω, C _L = 50 pF, See Figure 5			30	ns

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
t _{DD}	Differential output delay time	'ALS176	3	8	13	ns	
		'ALS176A	4	7	11.5		
		'ALS176B	5	8	10		
t _{sk(p)}	Pulse skew (t _{DDL} - t _{DDH})	R _L = 54 Ω, C _L = 50 pF, See Figure 3		0	2	ns	
t _{TD}	Differential output transition time			8		ns	
t _{PZH}	Output enable time to high level	R _L = 110 Ω, C _L = 50 pF, See Figure 4			23	50	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω, C _L = 50 pF, See Figure 5			14	20	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω, C _L = 50 pF, See Figure 4			20	35	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω, C _L = 50 pF, See Figure 5			8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V _O	V _{oa} , V _{ob}	V _{oa} , V _{ob}
V _{OD1}	V _o	V _o
V _{OD2}	V _t (R _L = 100 Ω)	V _t (R _L = 54 Ω)
V _{OD3}		V _t (Test Termination Measurement 2)
Δ V _{OD}	V _t - V _t	V _t - V _t
V _{OC}	V _{os}	V _{os}
Δ V _{OC}	V _{os} - V _{os}	V _{os} - V _{os}
I _{OS}	I _{sa} , I _{sb}	
I _O	I _{xa} , I _{xb}	I _{ia} , I _{ib}


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SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V _{TH}	Differential-input high-threshold voltage	V _O = 2.7 V, I _O = -0.4 mA			0.2	V	
V _{TL}	Differential-input low-threshold voltage	V _O = 0.5 V, I _O = 8 mA	-0.2‡			V	
V _{hys}	Hysteresis§			60		mV	
V _{IK}	Enable-input clamp voltage	I _I = -18 mA			-1.5	V	
V _{OH}	High-level output voltage	V _{ID} = -200 mV, I _{OH} = -400 µA, See Figure 6	2.7			V	
V _{OL}	Low-level output voltage	V _{ID} = -200 mV, I _{OL} = 8 mA, See Figure 6			0.45	V	
I _{OZ}	High-impedance-state output current	V _O = 0.4 V to 2.4 V			±20	µA	
I _I	Line input current	Other input = 0 V, V _I = 12 V See Note 4, V _I = 7 V			1 -0.8	mA	
I _{IH}	High-level enable-input current	V _{IH} = 2.7 V			20	µA	
I _{IL}	Low-level enable-input current	V _{IL} = 0.4 V			-100	µA	
r _i	Input resistance		12	20		kΩ	
I _{OS}	Short-circuit output current	V _{ID} = 200 mV, V _O = 0	-15		-85	mA	
I _{CC}	Supply current	No load			23 19	30 26	mA
						Outputs enabled Outputs disabled	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{pd}	Propagation time	V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See Figure 7			25	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			0	2	ns
t _{PZH}	Output enable time to high level	C _L = 15 pF, See Figure 8		11	18	ns
t _{PZL}	Output enable time to low level			11	18	ns
t _{PHZ}	Output disable time from high level				50	ns
t _{PLZ}	Output disable time from low level				30	ns

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
t _{pd}	Propagation time	V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See Figure 7	'ALS176	9	14	19	ns
			'ALS176A	10.5	14	18	
			'ALS176B	11.5	13	16.5	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			0	2	ns	
t _{PZH}	Output enable time to high level	C _L = 15 pF, See Figure 8		7	14	ns	
t _{PZL}	Output enable time to low level			20	35	ns	
t _{PHZ}	Output disable time from high level			20	35	ns	
t _{PLZ}	Output disable time from low level			8	17	ns	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.



**SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS**

PARAMETER MEASUREMENT INFORMATION

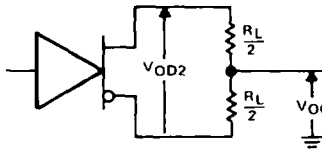


FIGURE 1. DRIVER V_{OD} AND V_{OC}

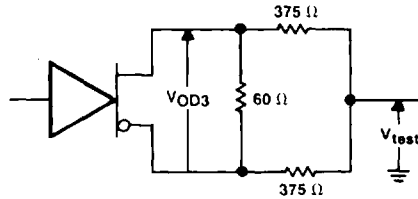
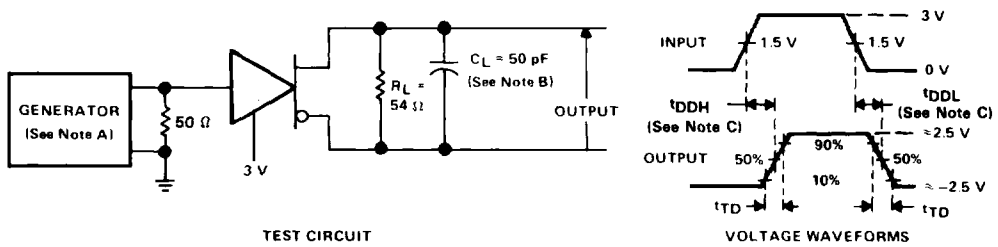


FIGURE 2. DRIVER V_{OD3}



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. $t_{OD} = t_{DDH}$ or t_{DDL}

FIGURE 3. DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

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DIFFERENTIAL BUS TRANSCEIVERS

PARAMETER MEASUREMENT INFORMATION

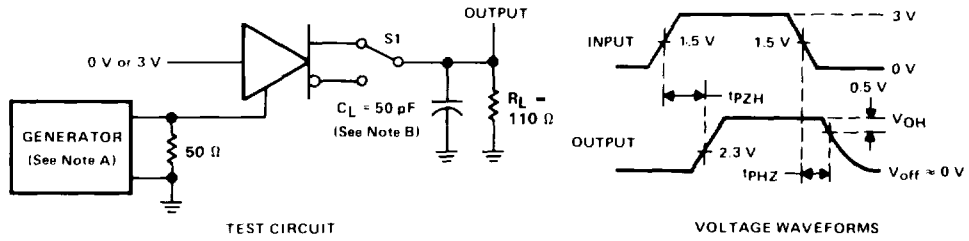


FIGURE 4. DRIVER ENABLE AND DISABLE TIMES

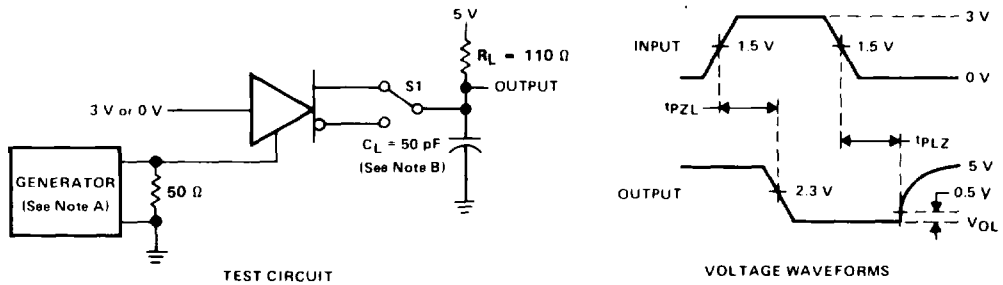


FIGURE 5. DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

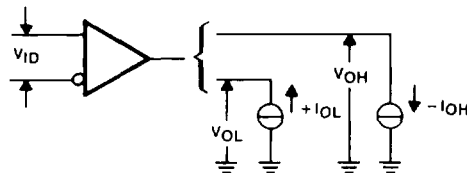
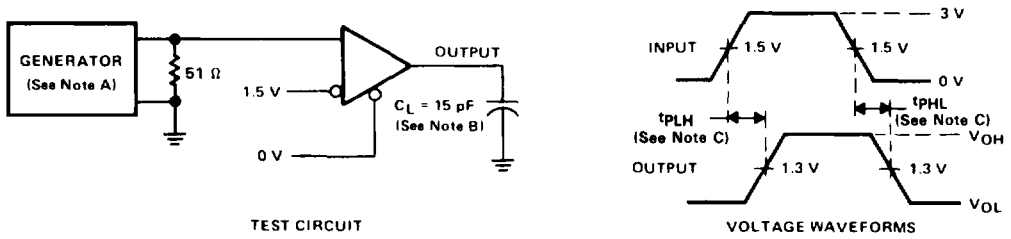


FIGURE 6. RECEIVER V_{OH} AND V_{OL}

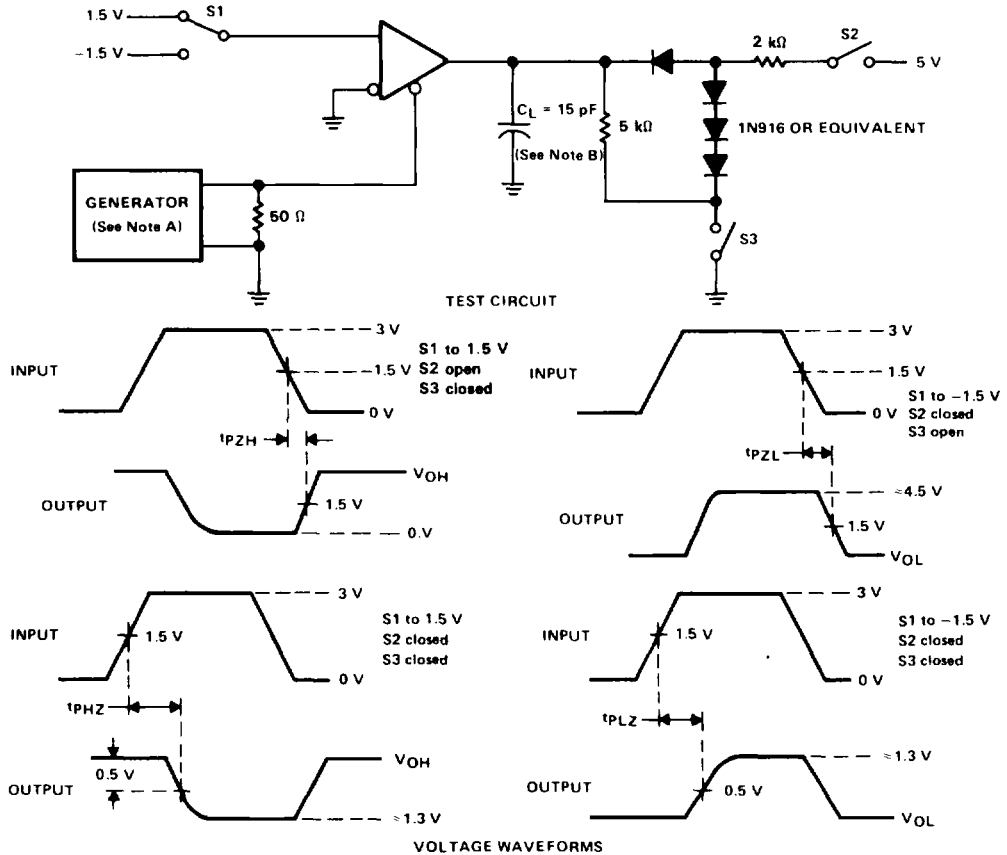
**SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS**

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

FIGURE 7. RECEIVER PROPAGATION DELAY TIMES



TEST CIRCUIT

FIGURE 8. RECEIVER OUTPUT ENABLE AND DISABLE TIMES

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_o = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. $t_{pd} = t_{PLH}$ or t_{PHL}



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS

TYPICAL CHARACTERISTICS

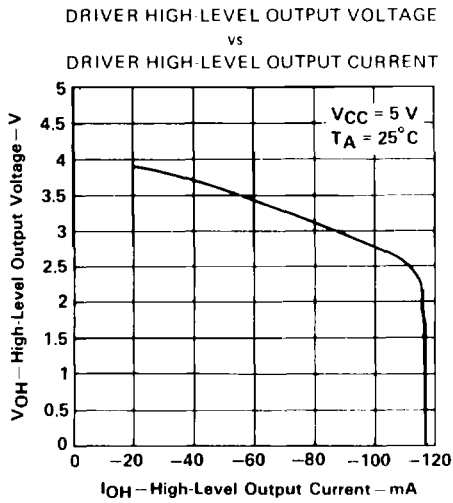


FIGURE 9

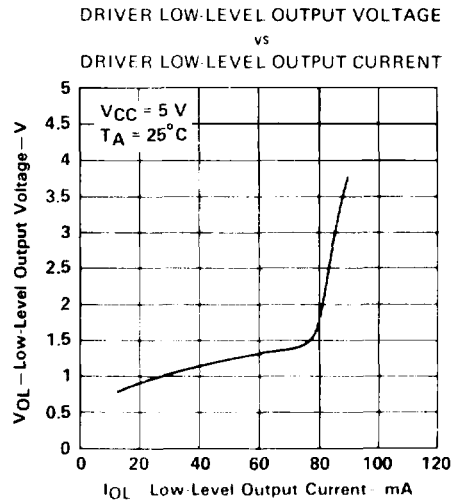


FIGURE 10

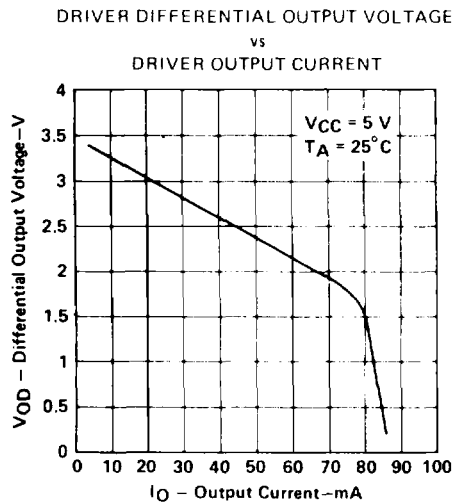


FIGURE 11

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS

TYPICAL CHARACTERISTICS

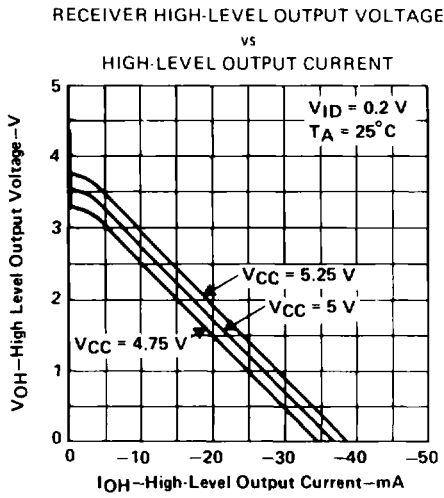


FIGURE 12

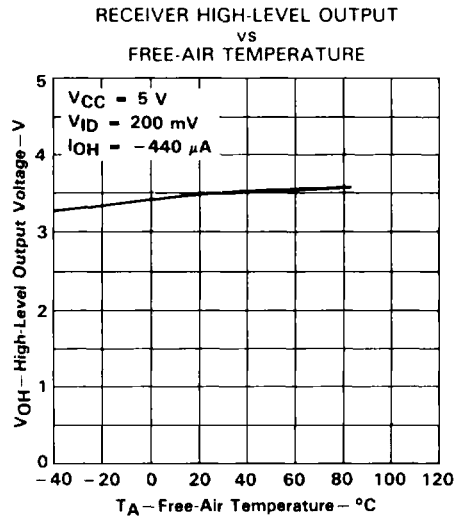


FIGURE 13

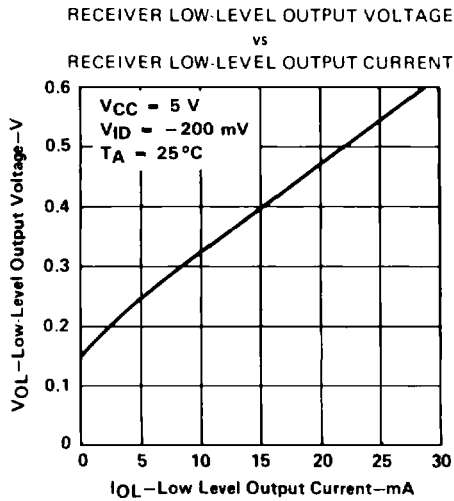


FIGURE 14

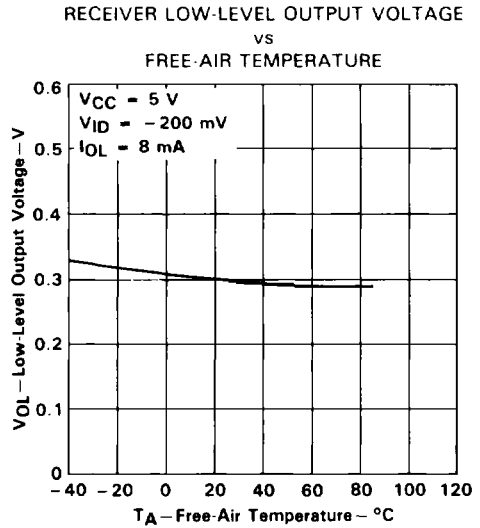


FIGURE 15

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS

TYPICAL CHARACTERISTICS

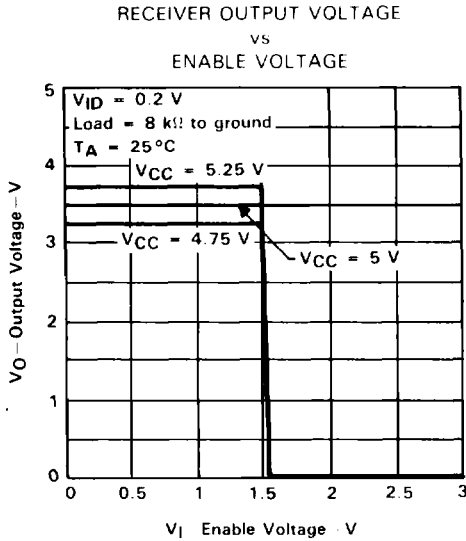


FIGURE 16

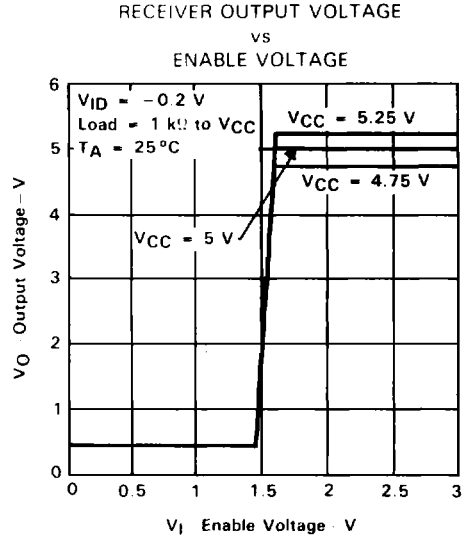


FIGURE 17

APPLICATION INFORMATION

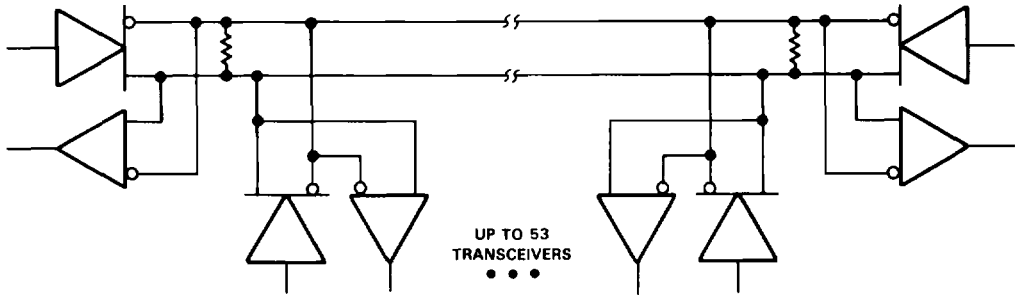


FIGURE 18. TYPICAL APPLICATION CIRCUIT

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.