74AC/ACT11240

Octal Buffer/Line Driver; 3-State; INV

Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffers**
- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11240 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11240 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($\overline{OE}$), each controlling four of the 3-State outputs.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF		5.0	6.3	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	39	47	pF
			Disabled	12	13	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		10	10	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

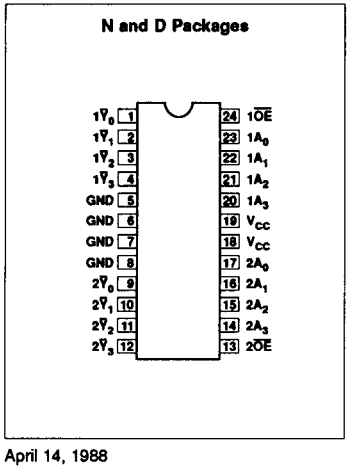
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

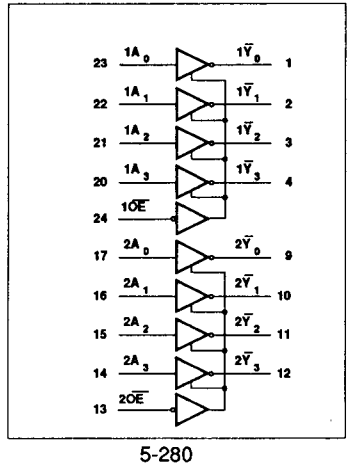
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11240N 74ACT11240N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11240D 74ACT11240D

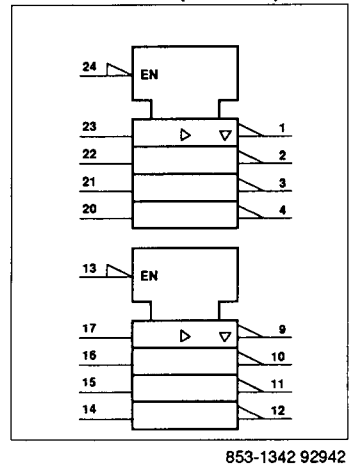
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
23, 22, 21, 20	$1A_0$ - $1A_3$	Data inputs
17, 16, 15, 14	$2A_0$ - $2A_3$	Data inputs
1, 2, 3, 4	$1\overline{Y}_0$ - $1\overline{Y}_3$	Data outputs
9, 10, 11, 12	$2\overline{Y}_0$ - $2\overline{Y}_3$	Data outputs
24, 13	$1\overline{OE}$, $2\overline{OE}$	Output enables
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	$2\overline{OE}$	$2A_n$	$1\overline{Y}_n$	$2\overline{Y}_n$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11240			74ACT11240			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Output enable	0		5	0		10	
T_A	Operating free-air temperature		-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11240				74ACT11240				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	7.6 6.3	10.5 8.6	1.5 1.5	11.7 9.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	8.2 7.6	11.6 10.8	1.5 1.5	12.7 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	5.5 6.7	7.5 9.4	1.5 1.5	7.8 9.8	ns

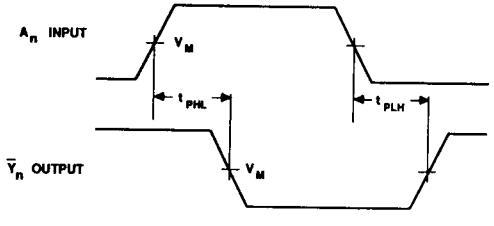
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	5.4 4.6	7.5 6.6	1.5 1.5	8.4 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	5.7 5.3	8.2 7.7	1.5 1.5	9.2 8.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	4.7 5.2	6.3 7.3	1.5 1.5	6.6 7.7	ns

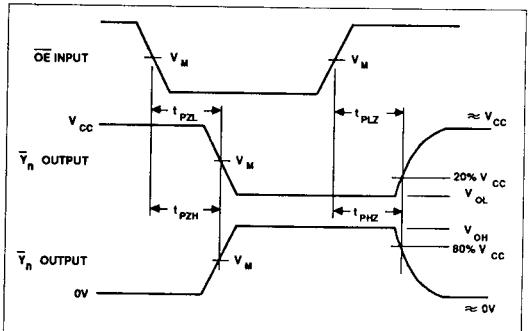
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11240					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	1	1.5 1.5	6.5 6.0	9.9 8.0	1.5 1.5	10.6 8.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low Level	2	1.5 1.5	7.5 7.3	11.7 11.5	1.5 1.5	12.5 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	7.3 7.9	9.4 10.3	1.5 1.5	10.0 10.8	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n) to Output ($\overline{Y}_n$) Propagation Delays

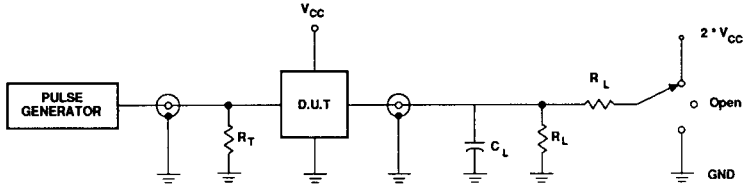


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
$t_{PLZ}t_{PZL}$	2*VCC
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

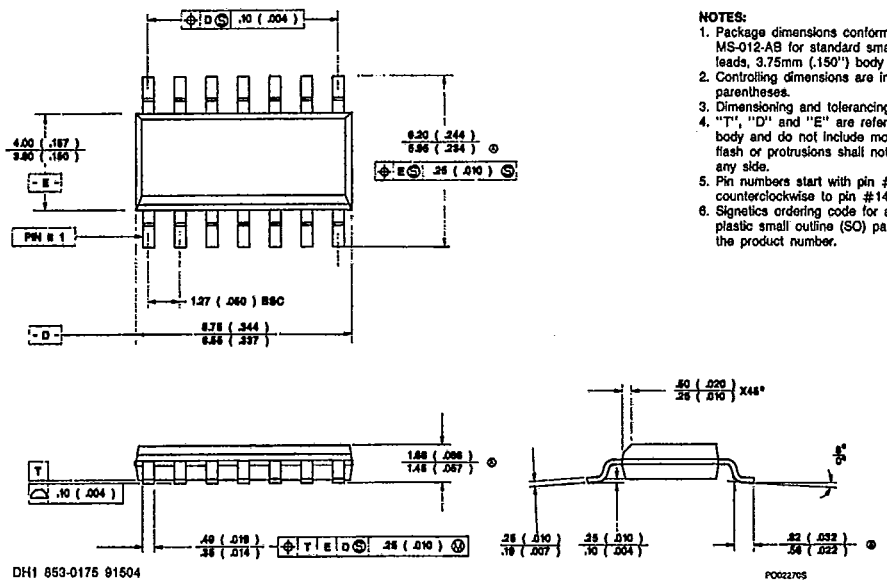
Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Packaging Information

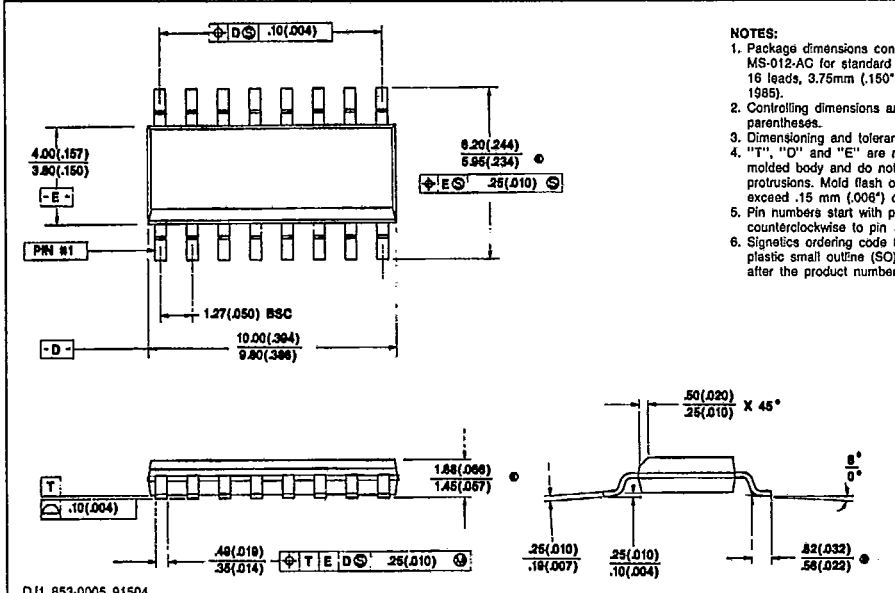
T-90-20

14-PIN PLASTIC SMALL OUTLINE (SO)



NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SMALL OUTLINE (SO)



NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference Datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix "D" after the product number.

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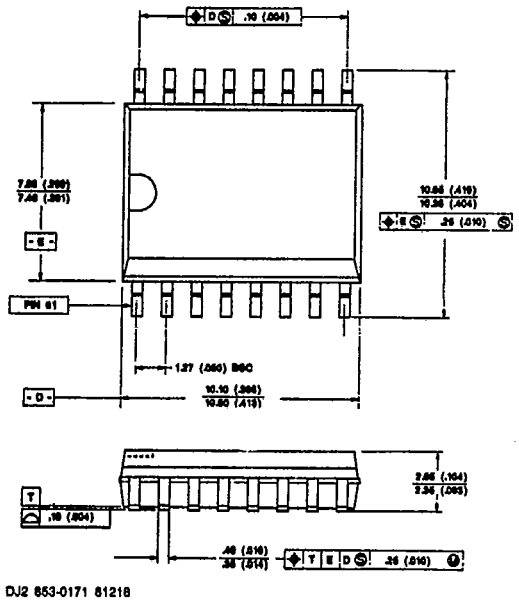
Packaging Information

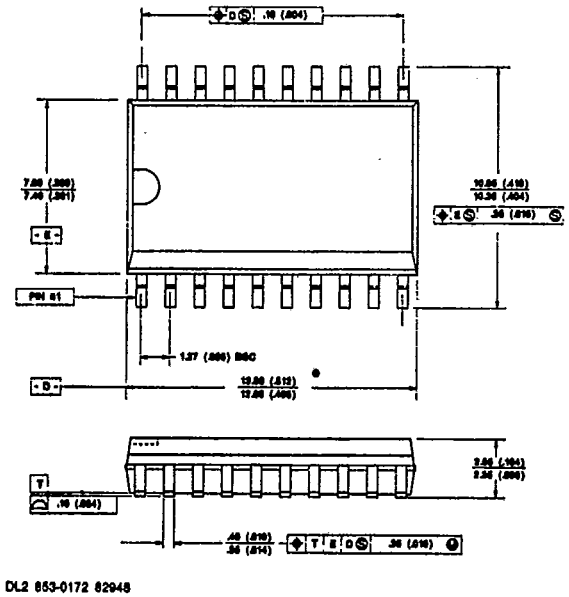
16-PIN PLASTIC SMALL OUTLINE (SOL)



NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (Issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

DJ2 853-0171 81218

20-PIN PLASTIC SMALL OUTLINE (SOL)

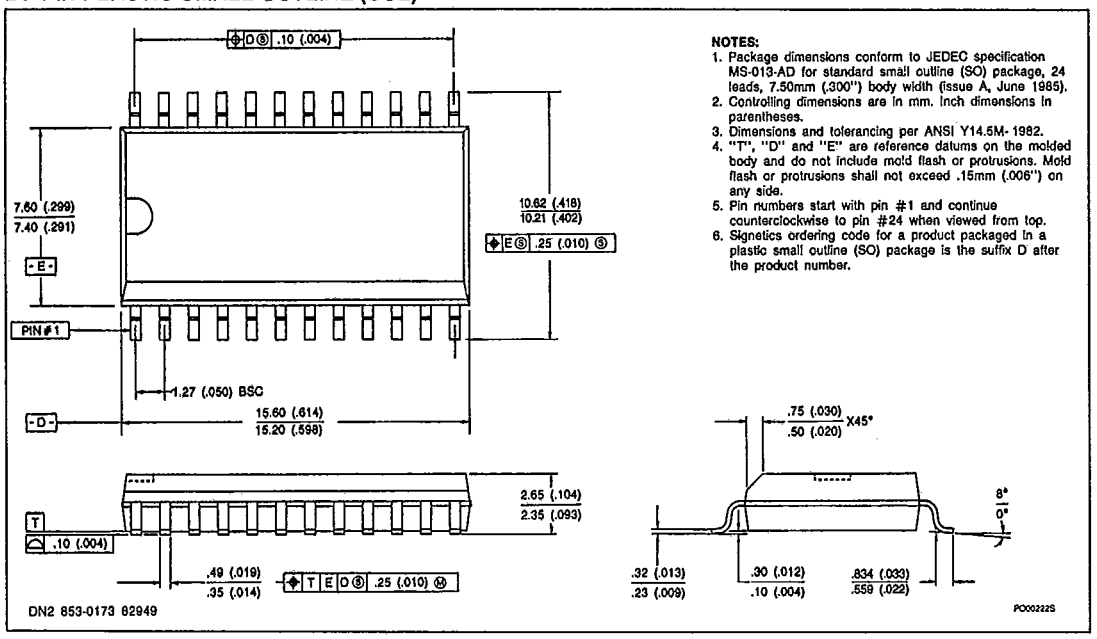


NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (Issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

DL2 853-0172 82948

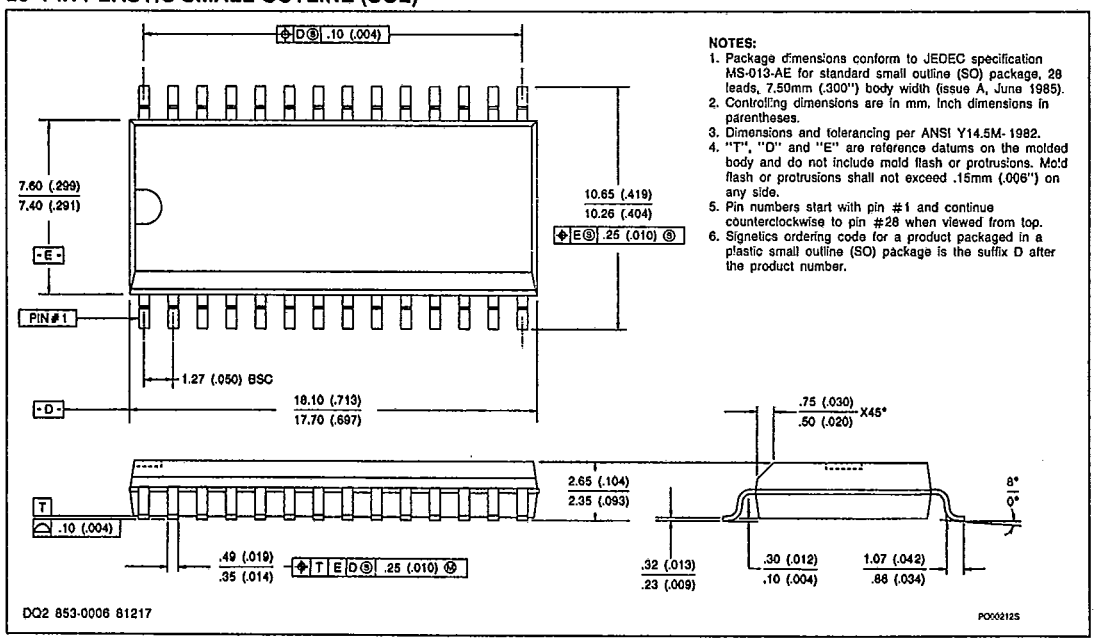
Packaging Information

24–PIN PLASTIC SMALL OUTLINE (SOL)



NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

28–PIN PLASTIC SMALL OUTLINE (SOL)



NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Packaging Information

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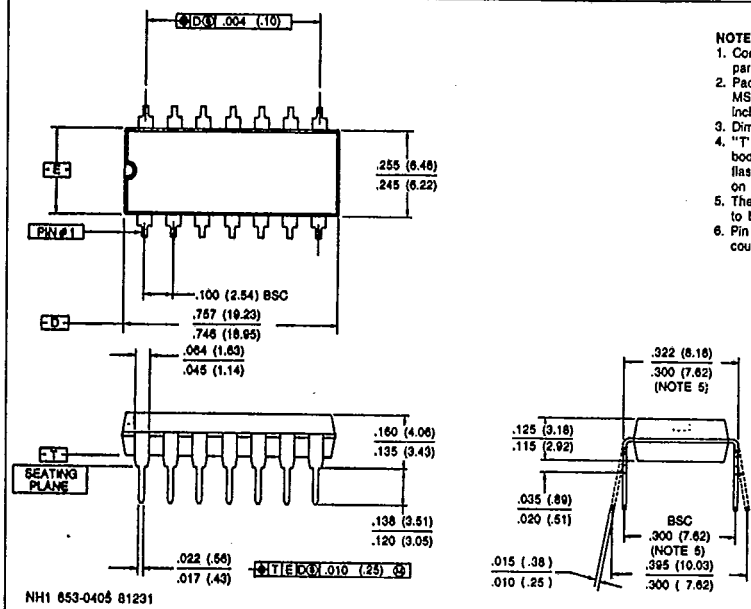
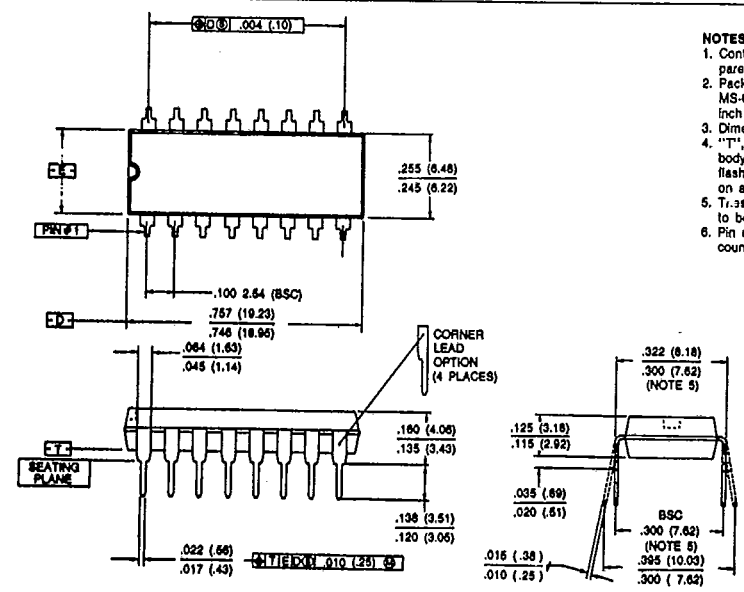
14-PIN PLASTIC DUAL IN-LINE (PDIP)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

16-PIN PLASTIC DUAL IN-LINE (PDIP)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

Packaging Information

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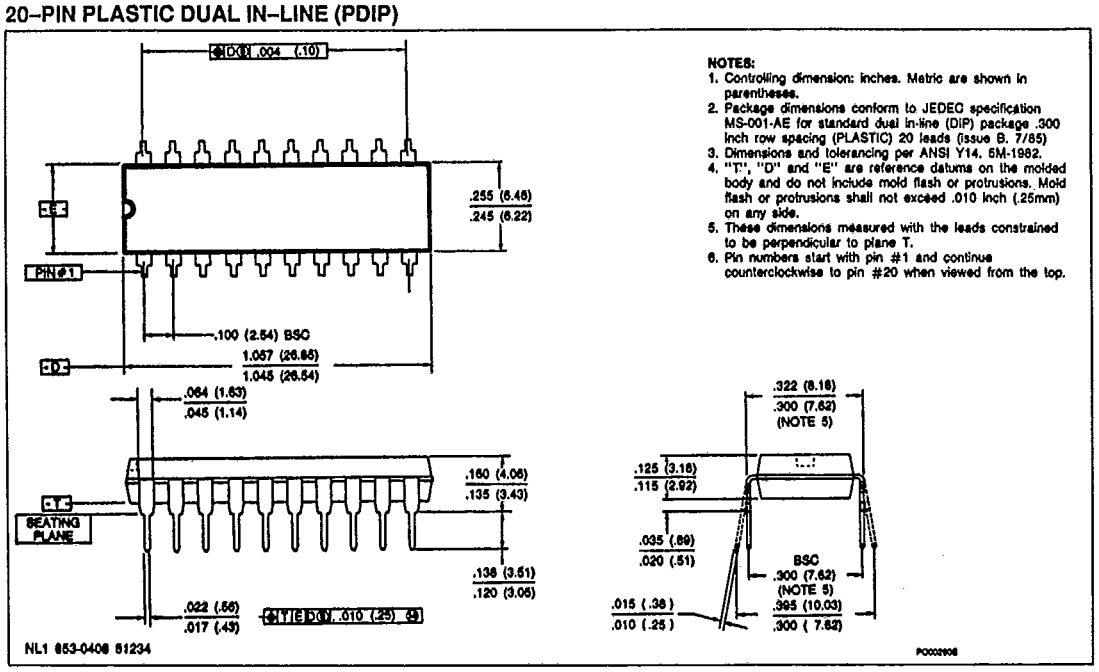
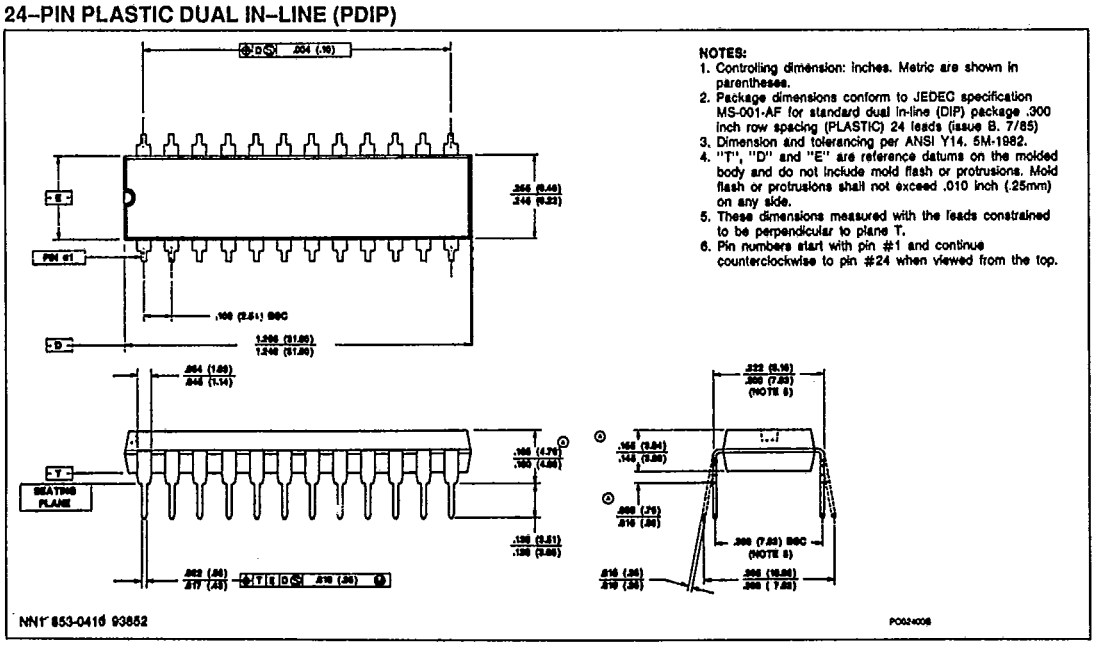
20-PIN PLASTIC DUAL IN-LINE (PDIP)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B, 7/85)
3. Dimensions and toleraricing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

24-PIN PLASTIC DUAL IN-LINE (PDIP)

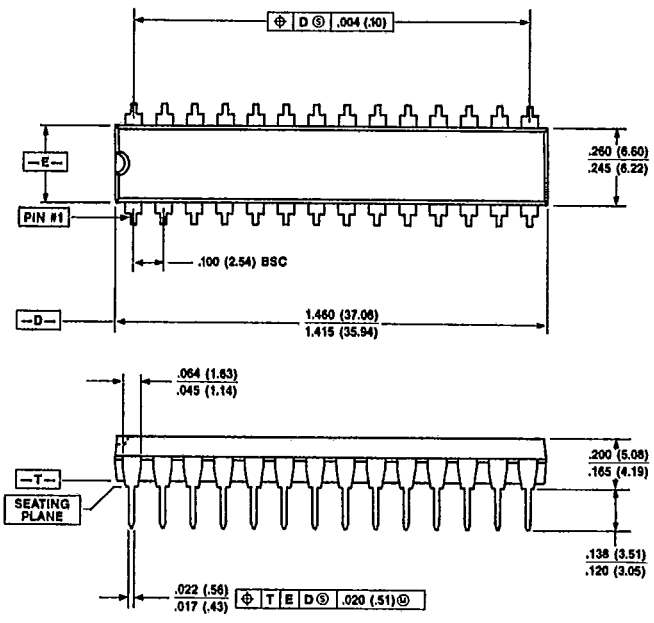


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AF for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B, 7/85)
3. Dimension and toleraricing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

T-90-20

Packaging Information

28-PIN PLASTIC DUAL IN-LINE (PDIP) (300-mil-wide)



NOTES:
1. Controlling dimensions: inches. Metric are shown in parentheses.
2. Dimensions are tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference datums on the molded body and do not include mold-flash or protrusions which shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane "T".
5. Pin numbers start with #1 and continue counterclockwise to pin #28 when viewed from the top.

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