### SN54HC623, SN74HC623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCLS149B – DECEMBER 1982 – REVISED MAY 1997

- Lock Bus-Latch Capability
- True Logic
- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

### description

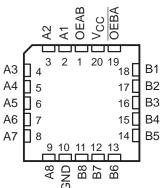
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SN74HC623	DW (TOP VI	-	I PACKAGE
OEAB [ A1 [ A2 [ A3 [ A4 [ A5 [ A6 [ A7 [ A8 [ GND [	3 4 5 6 7 8	20 19 18 17 16 15 14 13 12 11	B2 B3 B4 B5 B6
SN54HC6	623 F (TOP VI		CKAGE
	~	1.4	-

SN54HC623 ... J OR W PACKAGE



The SN54HC623 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC623 is characterized for operation from –40°C to 85°C.

	FUNCTION TABLE						
INP	UTS						
OEBA	OEAB	OPERATION					
L	L	B data to A bus					
н	Н	A data to B bus					
н	L	Isolation					
L	н	B data to A bus, A data to B bus					

FUNCTION TABLE



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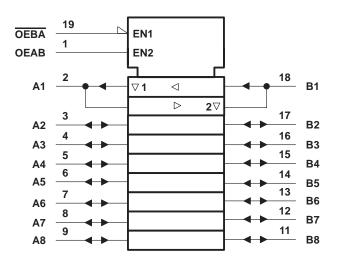


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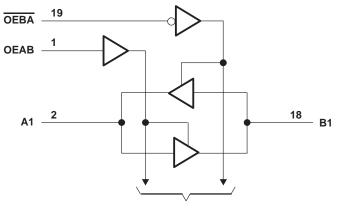
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### logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



**To Seven Other Transceivers** 

### absolute maximum ratings over operating free-air temperature range<sup>‡</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	±35 mA
Continuous current through V <sub>CC</sub> or GND	±70 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DW package	97°C/W
N package	67°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



### recommended operating conditions

			SN	SN54HC623		SN	174HC62	23	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		2	5	6	2	5	6	V
		$V_{CC} = 2 V$	1.5			1.5			
VIH	High-level input voltage	$V_{CC} = 4.5 V$	3.15			3.15			V
		$V_{CC} = 6 V$	4.2		M	4.2			
	Low-level input voltage	$V_{CC} = 2 V$	0	N.	0.5	0		0.5	
VIL		$V_{CC} = 4.5 V$	0	22	1.35	0		1.35	V
		$V_{CC} = 6 V$	0	5	1.8	0		1.8	
VI	Input voltage		0	50	VCC	0		VCC	V
VO	Output voltage		0	)	VCC	0		VCC	V
		$V_{CC} = 2 V$	0		1000	0		1000	
t <sub>t</sub>	Input transition (rise and fall) time	$V_{CC} = 4.5 V$	0		500	0		500	ns
		$V_{CC} = 6 V$	0		400	0		400	
Тд	Operating free-air temperature		-55		125	-40		85	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	AMETER	TEST COL		vcc	Т	A = 25°C	;	SN54H	IC623	SN74H	C623	UNIT
	AWEIER	TEST COL	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9			
			I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
VOH		$V_I = V_{IH} \text{ or } V_{IL}$		6 V	5.9	5.999		5.9		5.9		V
			I <sub>OH</sub> =6 mA	4.5 V	3.98	4.3		3.7		3.84		
			I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8		5.2	ΞW	5.34		
		$V_{I} = V_{IH} \text{ or } V_{IL}$		2 V		0.002	0.1		0.1		0.1	
			I <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1	4	0.1		0.1	
VOL				6 V		0.001	0.1	40	0.1		0.1	V
				$I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26	$n_{Q}$	0.4		0.33
			I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26	b A	0.4		0.33	
ų	OEAB OEBA	$V_I = V_{CC} \text{ or } 0$		6 V		±0.1	±100	Y	±1000		±1000	nA
IOZ	A or B	$V_{O} = V_{CC} \text{ or } 0$		6 V		±0.01	±0.5		±10		±5	μΑ
ICC		$V_I = V_{CC} \text{ or } 0,$	IO = 0	6 V			8		160		80	μA
Ci	OEAB OEBA			2 V to 6 V		3	10		10		10	pF



## SN54HC623, SN74HC623 **OCTAL BUS TRANSCEIVERS** WITH 3-STATE OUTPUTS

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# switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то		T <sub>A</sub> =	T <sub>A</sub> = 25°C			IC623	SN74H	C623	UNIT
PARAMETER	(INPUT)	(OUTPUT)	Vcc	MIN T	ΥP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		29	105		160		130	
<sup>t</sup> pd	A or B	B or A	4.5 V		10	21		32		26	ns
			6 V		8	18		27		22	
			2 V		112	210		315		265	
ten	OEBA	А	4.5 V		27	42		63		53	ns
			6 V		20	36		54		45	
			2 V		40	150		225		190	
<sup>t</sup> dis	OEBA	A	4.5 V		18	30		45		38	ns
			6 V		16	26		<b>2</b> 38		32	
			2 V		112	210	ζ.	315		265	
ten	OEAB	В	4.5 V		27	42	20	63		53	ns
			6 V		20	36	Y.	54		45	
			2 V		40	150		225		190	
<sup>t</sup> dis	OEAB	В	4.5 V		18	30		45		38	ns
			6 V		16	26		38		32	
			2 V		20	60		90		75	
tt		A or B	4.5 V		8	12		18		15	ns
			6 V		6	10		15		13	

# switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	Vaa	Τį	ς = 25°C	;	SN54HC62	23	SN74H	C623	UNIT
PARAMETER	(INPUT)	(OUTPUT)	Vcc	MIN	TYP	MAX	MIN M	AX	MIN	MAX	UNIT
			2 V		44	135	2	200		170	
<sup>t</sup> pd	A or B	B or A	4.5 V		14	27		40		34	ns
			6 V		11	23		34		29	
			2 V		130	270	4	405		335	
	OEBA	A	4.5 V		31	54	1Z	81		67	ns
			6 V		23	46	Q	69		56	
t <sub>en</sub>	OEAB		2 V		130	270	0	405		335	
		В	4.5 V		31	54	200	81		67	ns
			6 V		23	46	40	69		56	
	A or B		2 V		45	210	3	315		265	
tt		A or B	4.5 V		17	42		63		53	ns
			6 V		13	36		53		45	

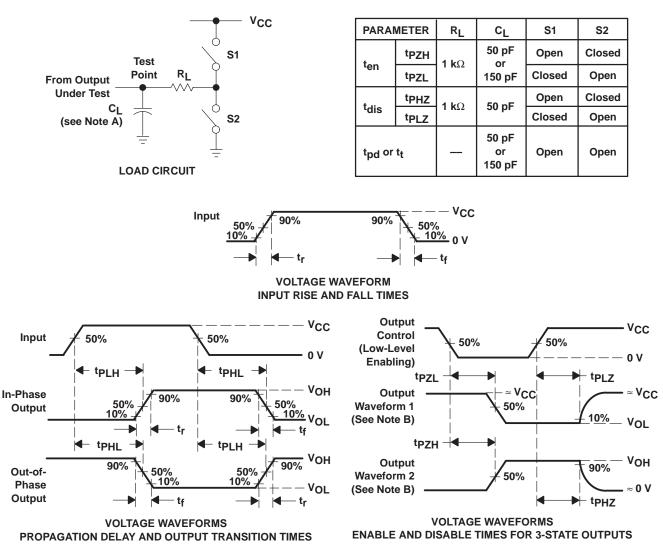
### operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	No load	40	pF

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### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. CL includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>Q</sub> = 50  $\Omega$ , t<sub>f</sub> = 6 ns, t<sub>f</sub> = 6 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

### Figure 1. Load Circuit and Voltage Waveforms



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 | APPLICATION NOTES | RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

#### SN74HC623, Octal Bus Transceivers With 3-State Outputs DEVICE STATUS: ACTIVE

SN74HC623
6, 5, 2
2.0 to 6.0
CMOS
CMOS
-6/6
8
True
0.08
22

#### FEATURES

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- Lock Bus-Latch Capability
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- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads
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DESCRIPTION

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 DATASHEET
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 Full datasheet in Acrobat PDF: sn74hc623.pdf (111 KB,Rev.B) (Updated: 05/01/1997)
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APPLICATION NOTES

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View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 Updated: 10/01/1996)
- LVT-to-LVTH Conversion (SCEA010 Updated: 12/08/1998)
- Live Insertion (SDYA012 Updated: 10/01/1996)
- Logic Solutions For IEEE Std 1284 (SCEA013 Updated: 06/01/1999)
- SN54/74HCT CMOS Logic Family Applications and Restrictions (SCLA011 Updated: 05/01/1996)
- Selecting the Right Texas Instruments Signal Switch (SZZA030 Updated: 09/07/2001)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 Updated: 04/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB Updated: 04/22/2002)

SAMPLES	<u>ABack to Top</u>									
ORDERABLE DEVICE	<u>PACKAGE</u> <u>INDUSTRY (TI)</u>	<u>PINS</u>	<u>TEMP (°C)</u>	<u>STATUS</u>	PRODUCT CONTENT	<u>SAMPLES</u>				
SN74HC623DW	<u>SOP</u> (DW)	20	-40 TO 85	ACTIVE	View Product Content	<u>Request Samples</u>				
SN74HC623N	PDIP (N)	20	-40 TO 85	ACTIVE	View Product Content	<u>Request Samples</u>				

PRICING/AVA	PKG					Back to Top							
DEVICE INFORMATION								TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	<u>STATUS</u>	<u>PACKAGE</u> <u>TYPE PINS</u>	<u>TEMP (°C)</u>	PRODUCT CONTENT	BUDGETARY PRICING QTY   \$US	<u>STD</u> <u>PACK</u> <u>QTY</u>	IN STOCK	<u>IN PROGRESS</u> QTY DATE	<u>LEAD TIME</u>	DISTRIBUTOR COMPANY REGION	<u>IN STOCK</u>	PURCHASE	
SN74HC623DW	ACTIVE	<u>SOP</u> ( <u>DW)</u>   20	-40 TO 85	<u>View Contents</u>	1KU   3.64	25	<u>N/A*</u>	100   03 Oct	2 WKS				
								4984   07 Oct					
								>10k   14 Oct					
SN74HC623DWR	ACTIVE	<u>SOP</u> ( <u>DW)</u>   20	-40 TO 85	<u>View Contents</u>	1KU   3.67	2000	8000	4984   04 Oct	2 WKS				
								>10k   11 Oct					
SN74HC623N	ACTIVE	$\frac{\underline{PDIP}}{\underline{(N)}} \mid 20$	-40 TO 85	<u>View Contents</u>	1KU   3.64	20	2000	640   19 Sep	2 WKS				
								2   25 Sep					
								4969   07 Oct					

							>10k   14 Oct			
							5287   21 Oct			
SN74HC623NSR	ACTIVE	$\frac{\text{SOP}}{(\text{NS})} \mid 20$	View Contents	1KU   3.64	2000	<u>N/A*</u>	4967   07 Oct	3 WKS		
							>10k   14 Oct			

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