2K x 8 Static RAM (Low Power) L6116/L6116L

FEATURES

- 2K x 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 10 ns maximum
- Low Power Operation
  Active:
  250 mW (L6116) typical at 35 ns
  Standby (typical):
  100 µW (L6116)
  50 µW (L6116L)
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT6116, Cypress CY7C128/CY6116
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin CerDIP
  - 24-pin Plastic SOIC
  - 24-pin Plastic SOJ
  - 28-pin Ceramic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The L6116 and L6116L are high-performance, low-power CMOS static RAM. The storage circuitry is organized as 2048 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in six speeds with maximum access times from 10 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L6116 is 250 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) for the L6116 and 60 mW (typical) for the L6116L when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L6116 and L6116L consume only 15 µW and 6 µW (typical) respectively at 3 V, allowing effective battery backup operation.

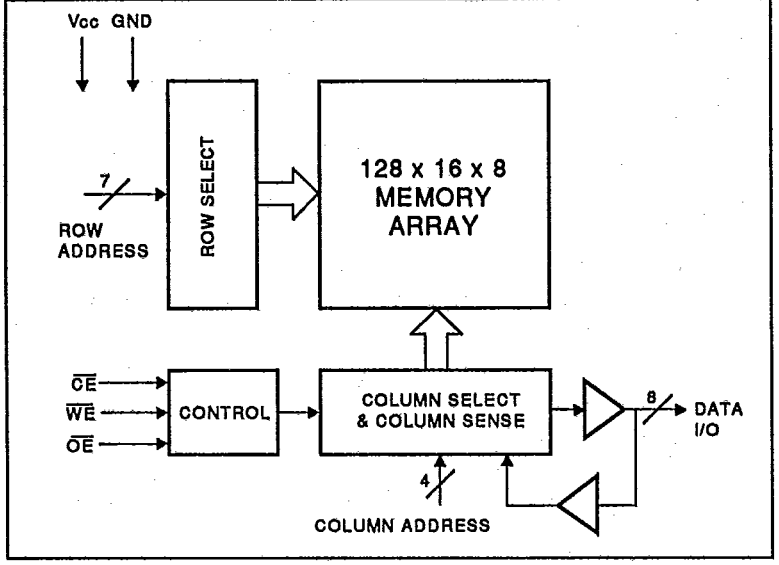
The L6116 and L6116L provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{10}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is high, or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L6116 and L6116L can withstand an injection current of up to 200 mA on any pin without damage.

L6116/L6116L BLOCK DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ Vcc ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ Vcc ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ Vcc ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

			L6116			L6116L			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, Vcc = 4.5 V	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4			0.4	V
V_{IH}	Input High Voltage		2.0		Vcc +0.3	2.0		Vcc +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ Vcc	–10		+10	–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ Vcc, $\overline{CE}$ = Vcc	–10		+10	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, Vcc = Max (Note 4)			–350			–350	mA
I_{CC2}	Vcc Current, TTL Inactive	(Note 7)		15	30		12	20	mA
I_{CC3}	Vcc Current, CMOS Standby	(Note 8)		20	100		10	30	µA
I_{CC4}	Vcc Current, Data Retention	Vcc = 3.0 V (Note 9)		5	50		2	10	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, Vcc = 5.0 V			5			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

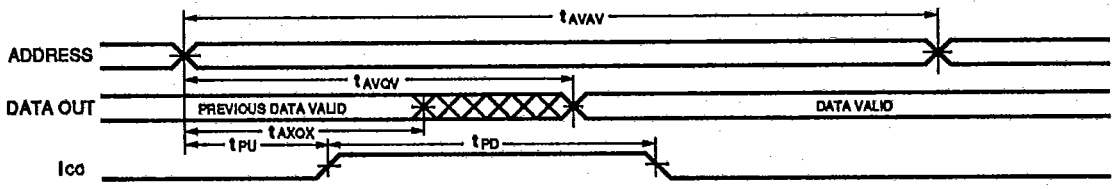
			L6116-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10		Unit
I_{CC1}	Vcc Current, Active	(Note 6)	75	100	125	160	200	220		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

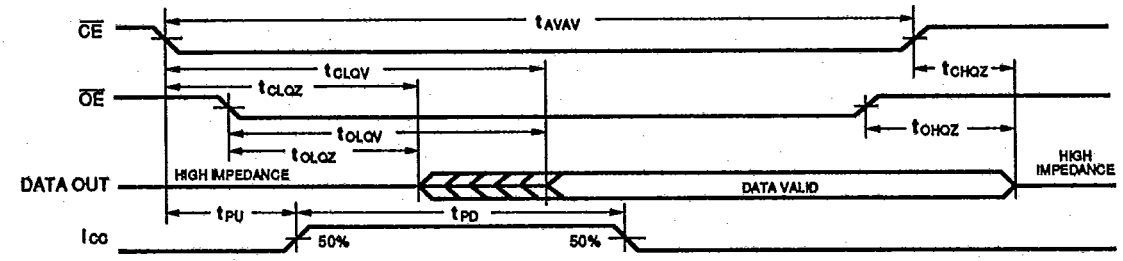
Read Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L6116/L6116L- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
tAVAV	Read Cycle Time	35		25		20		15		12		10			
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		
tAXQX	Address Change to Output Change	3		3		3		3		3		3			
tCLQV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3			
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		
tOLQV	Output Enable Low to Output Valid		15		12		10		8		6		5		
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0			
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0			
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0			

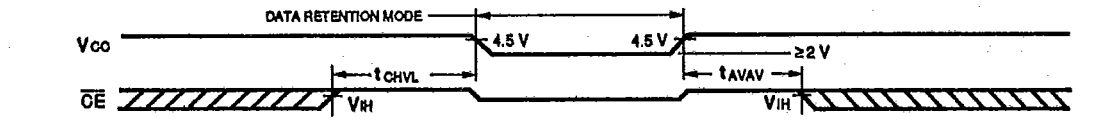
Read Cycle — Address Controlled (Notes 13, 14)



Read Cycle — CE/OE Controlled (Notes 13, 15)



Data Retention



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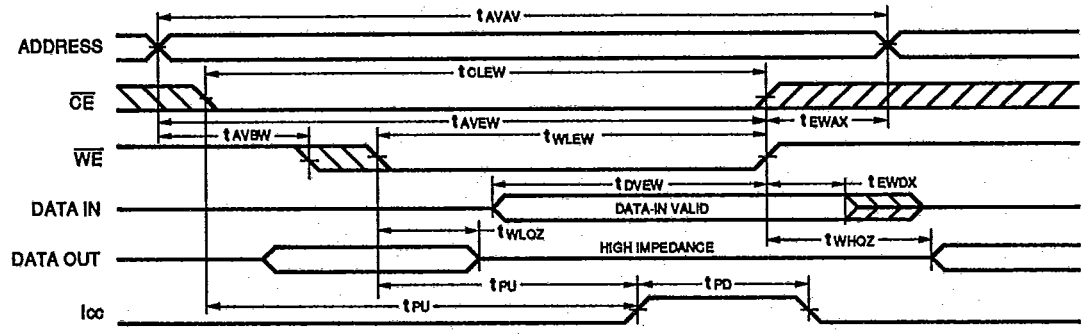
SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

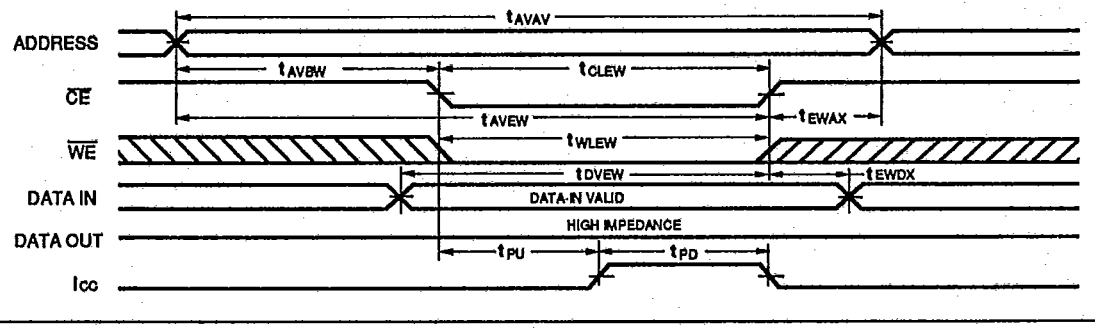
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L6116/L6116L- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12		10			
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8			
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0			
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8			
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0			
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8			
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5			
tEWDX	End of Write Cycle to Data Change	1		1		1		1		1		1			
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0			
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

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FIGURE 1a.

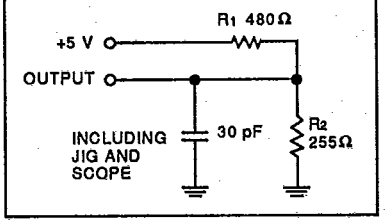


FIGURE 1b.

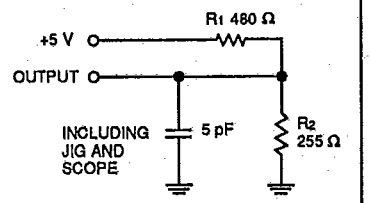
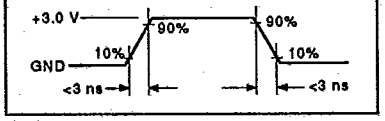
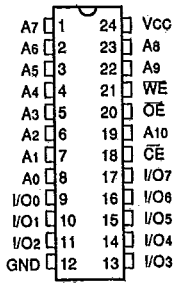


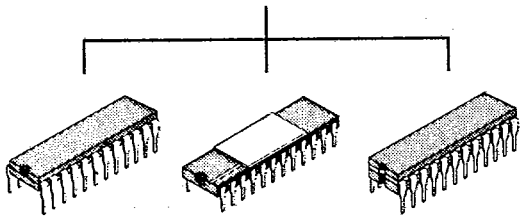
FIGURE 2.



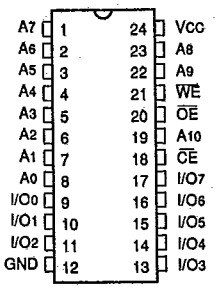
ORDERING INFORMATION

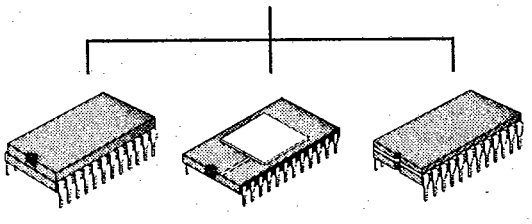
24-pin (0.3" wide)





24-pin (0.6" wide)

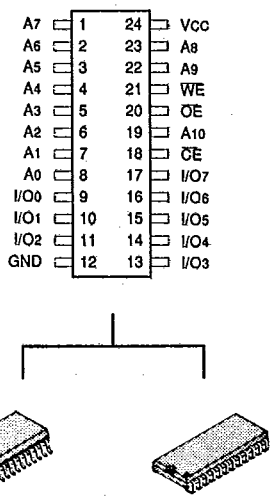




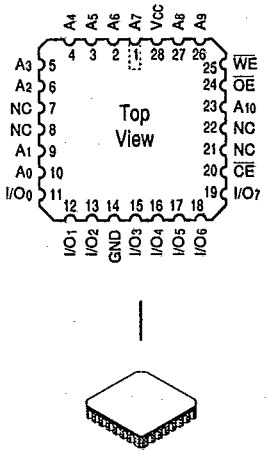
Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic DIP (P1)	Sidebraze Hermetic DIP (D1)	CerDIP (C4)
	0°C to +70°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L6116PC / L6116LPC	L6116DC / L6116LDC	L6116CC / L6116LCC	L6116NC / L6116LNC	L6116HC / L6116LHC	L6116IC / L6116LIC
	–55°C to +125°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L6116DM / L6116LDM	L6116CM / L6116LCM		L6116HM / L6116LHM	L6116IM / L6116LIM
	–55°C to +125°C — Extended Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L6116DME / L6116LDME	L6116CME / L6116LCME		L6116HME / L6116LHME	L6116IME / L6116LIME
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L6116DMB / L6116LDMB	L6116CMB / L6116LCMB		L6116HMB / L6116LHMB	L6116IMB / L6116LIMB

ORDERING INFORMATION

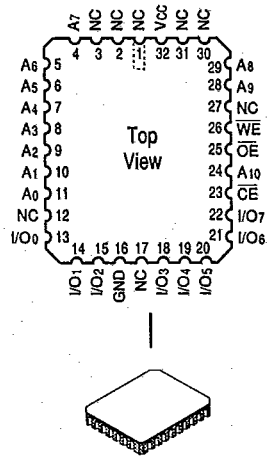
24-pin



28-pin (450 x 450)



32-pin (450 x 550)



Speed	Plastic SOIC (.300"— U1)	Plastic SOJ (.300"— W1)	Ceramic Leadless Chip Carrier (K1)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening			
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L6116UC or L6116LUC 35 25 20 15 12 10	L6116WC or L6116LWC 35 25 20 15 12 10	L6116KC or L6116LKC 35 25 20 15 12 10	L6116TC or L6116LTC 35 25 20 15 12 10
	–55°C to +125°C — Commercial Screening			
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L6116KM or L6116LKM 35 25 20 15 12	L6116TM or L6116LTM 35 25 20 15 12
	–55°C to +125°C — Extended Screening			
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L6116KME or L6116LKME 35 25 20 15 12	L6116TME or L6116LTME 35 25 20 15 12
	–55°C to +125°C — MIL-STD-883 Compliant			
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L6116KMB or L6116LKMB 35 25 20 15 12	L6116TMB or L6116LTMB 35 25 20 15 12