# HARRIS HI-5687V/883

## Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter

May 1988

### Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **DAC 87 Alternate Source**
- **Monolithic Construction (Single Chip)**
- **Fast Settling**
- **Guaranteed Specifications**
- **Wafer Laser Trimmed**
- **Applications Resistors On-Chip**
- **On-Chip Reference**
- **Dielectric Isolation (DI) Processing**
- **±12V Power Supply Operation**

### Applications

- **High Speed A/D Converters**
- **Precision Instrumentation**
- **CRT Display Generation**

### Description

The HI-5687V/883 is a monolithic direct replacement for the popular DAC 87-CBI wide temperature range digital-to-analog converter. Single chip construction, along with several design innovations make the HI-5687/883 the optimum choice for low cost, high reliability applications.

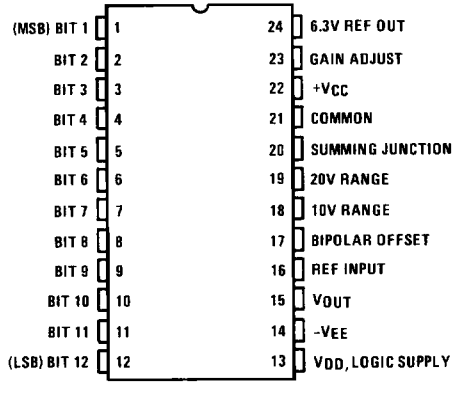
The Harris unique Dielectric Isolation (DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. On-board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-chip op amp.

Internally, the HI-5687V/883 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents, allowing virtually zero variation in current through the package common, pin 21, (25).

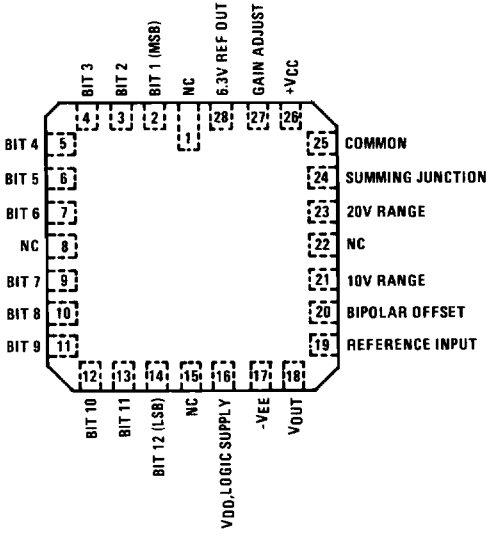
The HI-5687V/883 includes an on-chip output amplifier, a buried zener voltage reference featuring low temperature coefficient, and operates with a +5V logic supply and a $+V_{CC}$, $-V_{EE}$ in the range of ±11.4V to ±16.5V.

### Pinouts

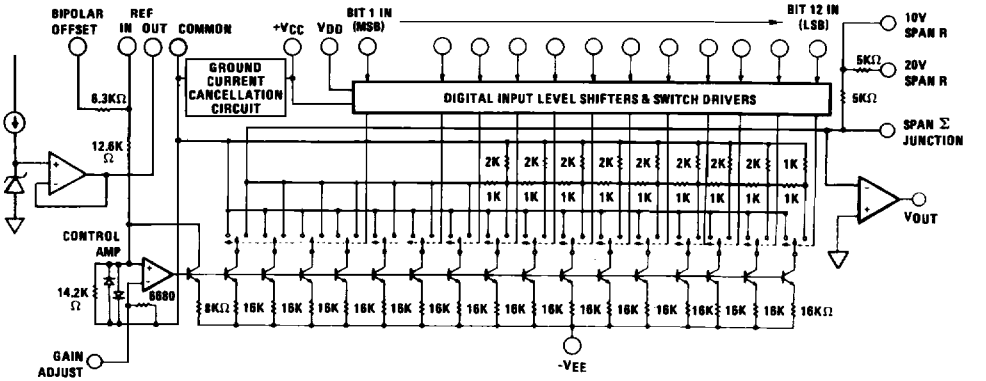
**HI1-5687V/883 (CERAMIC SIDEBRAZE DIP)**
TOP VIEW




**HI4-5687V/883 (CERAMIC LCC)**
TOP VIEW



## Functional Block Diagram



## Absolute Maximum Ratings (Note 1)

All Voltages Referred to Common
Power Supply Inputs
- $+V_{CC}$ ..... +20V
- $-V_{EE}$ ..... -20V
- $V_{DD}$ ..... +20V

Reference
- Input ..... $+V_{CC}$ to $-V_{EE}$
- Output Current ..... 6mA

Digital Inputs
- Bits 1 to 12 ..... -1V to +12V

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... 275°C
Junction Temperature ..... 175°C

## Thermal Information

Thermal Resistance, Junction-to-Case ($\theta_{jc}$)
- Ceramic DIP Package ..... 12°C/W
- Ceramic LCC Package ..... 40°C/W

Thermal Resistance Junction-to-Ambient ($\theta_{ja}$)
- Ceramic DIP Package ..... 49°C/W
- Ceramic LCC Package ..... 81°C/W

Power Dissipation at 75°C
- Ceramic DIP Package ..... 2040mW
- Ceramic LCC Package ..... 1235mW

Power Dissipation Derating Factor (Above +75°C)
- Ceramic DIP Package ..... 20.4mW/°C
- Ceramic LCC Package ..... 12.35mW/°C

## Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage (Note 5);
- $+V_{CC}$ ..... +12V to +15V
- $-V_{EE}$ ..... -12V to -15V
- $+V_{DD}$ ..... +5V

Reference Input Voltage ..... 6.3V
Logic Low Level ..... 0V to 0.8V
Logic High Level ..... 2.0V to 5.5V

### TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, $V_{DD}$ = +5V, Reference Out Connected to Reference In, Pin numbers correspond to DIP package only; Unless Otherwise Specified.

| D.C PARAMETERS | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current From $V_{CC}$ | $I_{CC}$ | All Bits OFF, $V_{IH}$ = 2.0V | 1 | +25°C | — | 11.0 | mA |
| | | | 2, 3 | -55°C, +125°C | — | 13.5 | mA |
| Supply Current From $V_{EE}$ | $I_{EE}$ | All Bits OFF, $V_{IH}$ = 2.0V | 1 | +25°C | -20.0 | — | mA |
| | | | 2, 3 | -55°C, +125°C | -22.5 | — | mA |
| Supply Current From $V_{DD}$ | $I_{DD}$ | All Bits OFF, $V_{IH}$ = 2.0V | 1 | +25°C | — | 8.0 | mA |
| | | | 2, 3 | -55°C, +125°C | — | 9.50 | mA |
| Digital Input Low Current | $I_{IL}$ | Each Bit Tested Separately Input Under Test, $V_{IL}$ = 0V, all other Bits, $V_{IL}$ = 0.8V | 1 | +25°C | -50 | — | μA |
| | | | 2, 3 | -55°C, +125°C | -100 | — | μA |
| Digital Input High Current | $I_{IH}$ | Each Bit Tested Separately Input Under Test, $V_{IH}$ = 5.5V all other Bits, $V_{IL}$ = 0.8V | 1 | +25°C | -0.25 | 0.25 | μA |
| | | | 2, 3 | -55°C, +125°C | -1.0 | 1.0 | μA |
| Reference Voltage Unipolar Bipolar Loaded | $V_{REF(U)}$ $V_{REF(B)}$ $V_{REF(L)}$ | All Bits OFF, $V_{IH}$ = 2.0V Unipolar 10V Range Bipolar 20V Range Bipolar 20V Range 2.5mA Current Source from Pin 24 to Ground | 1 | +25°C | 6.20 | 6.40 | V |
| | | | 2, 3 | -55°C, +125°C | 6.20 | 6.40 | V |
| Unipolar Offset Error | $V_{OS}$ | All Bits OFF, $V_{IH}$ = 2.0V (Note 2) | 1 | +25°C | -0.10 | 0.10 | % FSR |
| | | | 2, 3 | -55°C, +125°C | -0.13 | 0.13 | % FSR |
| Unipolar Gain Error | $A_E$ | All Bits OFF to all Bits ON $V_{IH}$ = 2.0V, $V_{IL}$ = 0.8V (Note 2) | 1 | +25°C | -0.20 | 0.20 | % FSR |
| | | | 2, 3 | -55°C, +125°C | -0.45 | 0.45 | % FSR |
| Unipolar Gain Error, ±5mA Load Current | $A_{EI}$ ± | All Bits OFF to all Bits ON ±5mA Load Current from $V_O$ (Pin 15) to Ground | 1 | +25°C | -0.20 | 0.20 | % FSR |
| | | | 2, 3 | -55°C, +125°C | -0.45 | 0.45 | % FSR |
| Power Supply Sensitivity From $V_{CC}$ | $+P_{SS1}$ | All Bits ON, $V_{IL}$ = 0.8V $V_{CC}$ from 16.5V to 11.4V Bipolar Mode, ±5V Range | 1 | +25°C | -0.002 | 0.002 | $\frac{\Delta \% FSR}{\% \Delta V_{CC}}$ |
| Power Supply Sensitivity From $V_{DD}$ | $+P_{SS2}$ | All Bits ON, $V_{IL}$ = 0.8V $V_{DD}$ from 4.5V to 5.5V Bipolar Mode ±5V Range | 1 | +25°C | -0.002 | 0.002 | $\frac{\Delta \% FSR}{\% \Delta V_{DD}}$ |
| Power Supply Sensitivity From $V_{EE}$ | $-P_{SS1}$ | All Bits ON, $V_{IN}$ = 0.8V $V_{EE}$ from -16.5V to -11.4V Bipolar Mode ±5V Range | 1 | +25°C | -0.002 | 0.002 | $\frac{\Delta \% FSR}{\% \Delta V_{EE}}$ |

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

**TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

Devices Tested at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, $V_{DD}$ = +5V, Reference Out connected to Reference In, Pin numbers correspond to DIP package only, Unless Otherwise Specified.

| D.C. PARAMETERS | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Bipolar Offset Error | $BPO_E$ | All Bits OFF, $V_{IH}$ = 2.0V Bipolar ±10V Range (Note 2) | 1 | +25°C | -0.10 | 0.10 | % FSR |
| | | | 2, 3 | -55°C, +125°C | -0.20 | 0.20 | % FSR |
| Bipolar Zero Error | $BPZ_E$ | MSB ON, $V_{IL}$ = 0.8V; all other Bits OFF, $V_{IH}$ = 2.0V Bipolar ±10V Range | 1 | +25°C | -0.10 | 0.10 | % FSR |
| | | | 2, 3 | -55°C, +125°C | -0.20 | 0.20 | % FSR |
| Bipolar Gain Error | $BPA_E$ | All Bits OFF, to all Bits ON, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V Bipolar ±10V Range (Note 2) | 1 | +25°C | -0.20 | 0.20 | % FSR |
| | | | 2, 3 | -55°C, +125°C | -0.45 | 0.45 | % FSR |
| Integral Linearity Error | $L_E$ | Unipolar Mode 10V Range, Reference Chart B for Codes Tested | 1 | +25°C | -0.375 | 0.375 | LSB |
| | | | 2, 3 | -55°C, +125°C | -0.75 | 0.75 | LSB |
| Differential Linearity Error | $DL_E$ | Unipolar Mode 10V Range Reference Chart C for Codes Tested | 1 | +25°C | -0.50 | 0.50 | LSB |
| | | | 2, 3 | -55°C, +125°C | -1.0 | 1.0 | LSB |
| Gain Adjust | $A_A$ | Unipolar Mode All Bits ON, $V_{IL}$ = 0.8V (Note 6) | 1 | +25°C | ±0.20 | — | % FSR |
| Reference Voltage Drift Unipolar | $\frac{dV_{REF(U)}}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | -20 | 20 | ppm of $V_{REF}$ / °C |
| | | | 1, 3 | +25°C, -55°C | -20 | 20 | |
| Reference Voltage Drift Bipolar | $\frac{dV_{REF(B)}}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | -20 | 20 | ppm of $V_{REF}$ / °C |
| | | | 1, 3 | +25°C, -55°C | -20 | 20 | |
| Unipolar Offset Drift | $\frac{dV_{OS}}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | +3.0 | -3.0 | ppm of FSR / °C |
| | | | 1, 3 | +25°C, -55°C | +3.0 | -3.0 | |
| Unipolar Gain Drift | $\frac{dA_{E1}}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | -25 | +25 | ppm of FSR / °C |
| | | | 1, 3 | +25°C, -55°C | -25 | +25 | |
| Unipolar Gain Drift Exclusive of the Internal Reference | $\frac{dA_{E2}}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | -10 | +10 | ppm of FSR / °C |
| | | | 1, 3 | +25°C, -55°C | -10 | +10 | |
| Total Unipolar Error | $U_{ET}$ | (Note 3) | 1, 2 | +25°C, +125°C | -0.3 | 0.3 | % FSR |
| | | | 1, 3 | +25°C, -55°C | -0.3 | 0.3 | % FSR |
| Bipolar Offset Drift | $\frac{dBPO_E}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | -10 | +10 | ppm of FSR / °C |
| | | | 1, 3 | +25°C, -55°C | -10 | +10 | |
| Bipolar Gain Drift | $\frac{dBPA_{E1}}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | -25 | 25 | ppm of FSR / °C |
| | | | 1, 3 | +25°C, -55°C | -25 | 25 | |
| Bipolar Gain Drift Exclusive of the Internal Reference | $\frac{dBPA_{E2}}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | -10 | 10 | ppm of FSR / °C |
| | | | 1, 3 | +25°C, -55°C | -10 | 10 | |
| Total Bipolar Error | $B_{ET}$ | (Note 3) | 1, 2 | +25°C, +125°C | -0.24 | 0.24 | % FSR |
| | | | 1, 3 | +25°C, -55°C | -0.24 | 0.24 | % FSR |
| Total Bipolar Drift | $\frac{dBP_T}{dT}$ | (Note 3) | 1, 2 | +25°C, +125°C | -30 | 30 | ppm of FSR / °C |
| | | | 1, 3 | +25°C, -55°C | -30 | 30 | |

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is a "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
5. The HI-5687/883 will operate with supply voltage as low as ±11.4V. It is recommended that output voltage ranges -10V to +10V not be used if the supply voltages are less than ±12.5V.
6. Gain Adjust capability is tested by first measuring the full scale output voltage with pin 23 (DIP package) open, positive and negative adjustability are checked by applying ±15V to pin 23 (DIP package) through a 2.8MΩ resistor and measuring the full scale voltage for each condition. A minimum delta of ±20mV with respect to the initial reading guarantees ideal full scale adjustment as the gain error specification at +25°C is ±20mV (0.2% FSR).

**TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Devices Tested at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, $V_{DD}$ = +5V, Reference Out Connected to Reference In, Unless Otherwise Specified

| A.C. PARAMETERS | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMP | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Positive Slew Rate | $S_{R+}$ | All Bits OFF ($V_{IH}$ = 2V) to all Bits ON ($V_{IL}$ = 0.8V). Bipolar ±10V Range. Measurement Points at -6V and +6V. Figure 2. | 4 | +25°C | 11.0 | — | V/μs |
| Negative Slew Rate | $S_{R-}$ | All Bits ON ($V_{IL}$ = 0.8V) to all Bits OFF ($V_{IH}$ = 2.0V). Bipolar ±10V Range. Measurement Points at +6V and -6V. Figure 2. | 4 | +25°C | 11.0 | — | V/μs |

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Characterized at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, $V_{DD}$ = +5V, Reference Out Connected to Reference In, Unless Otherwise Specified

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMP | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Settling Time | $t_S$ | To ±0.5LSB for Full Scale Transition Unipolar 10V Range, $R_L$ = 5kΩ Figures 3 & 4 | 3, 7 | +25°C | — | 2.0 | μs |

NOTES: 7. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

**TABLE 4. ELECTRICAL TEST REQUIREMENTS**

| MIL-STD-883 TEST REQUIREMENTS | SUBGROUPS (SEE TABLES 1, 2 & 3) |
|---|---|
| Interim Electrical Parameters (Pre Burn-In) | 1 |
| Final Electrical Test Parameters | 1*, 2, 3, 4 |
| Group A Test Requirements | 1, 2, 3, 4 |
| Groups C & D Endpoints | 1 |

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

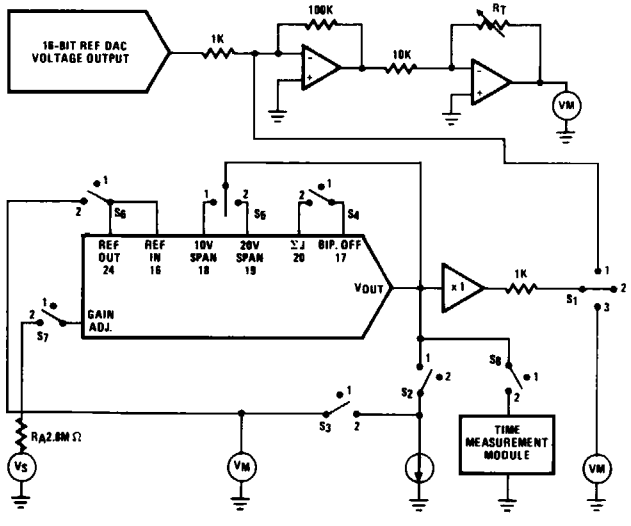



**FIGURE 1. TEST CIRCUIT**

**CHART A. GROUP A TEST CONDITIONS**

Pin 24 Tied to Pin 16, and Pin 23 Open Unless Otherwise Noted, All Pin Number's Listed Refer to the 24 Lead DIP Package.

| TEST | SYMBOL | CONDITIONS | PIN13 | PIN14 | PIN15 | PIN17 | PIN18 | PIN19 | PIN20 | PIN22 | SWITCH POSITION | | | | | | | | MEASURE | | EQUATIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ | $V_{EE}$ | $V_{OUT}$ | B.P. $R_{OUT}$ | 10V SPAN | 20V SPAN | $\Sigma_J$ | $V_{CC}$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | VALUE | UNIT | |
| Supply Current From $V_{CC}$ | $I_{CC}$ | All Bits OFF, $V_{IH}$ = 2.0V | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C. | O.C. | 15V | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | — | mA | |
| Supply Current From $V_{EE}$ | $I_{EE}$ | All Bits OFF, $V_{IH}$ = 2.0V | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C | O.C. | 15V | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | — | mA | |
| Supply Current From $V_{DD}$ | $I_{DD}$ | All Bits OFF, $V_{IH}$ = 2.0V | 5V | -15V | Pin 18 | O.C | Pin 15 | O.C. | O.C. | 15V | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | — | mA | |
| Digital Input Low Current | $I_{IL}$ | Each Bit Test Separately Bit Input Under Test. $V_{IL}$ = 0V, All Other Bits, $V_{IH}$ = 0.8V | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C. | O.C. | 15V | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | — | μA | |
| Digital Input High Current | $I_{IH}$ | Each Bit Test Separately Bit Input Under Test. $V_{IH}$ = 5.5V, All Other Bits, $V_{IL}$ = 0.8V | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C. | O.C. | 15V | 2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | — | μA | |

## CHART A. GROUP A TEST CONDITIONS (Continued)

Pin 24 Tied to Pin 16, and Pin 23 Open Unless Otherwise Noted, All Pin Number's Listed Refer to the 24 Lead DIP Package.

| TEST | SYMBOL | CONDITIONS | PIN13 $V_{DD}$ | PIN14 $V_{EE}$ | PIN15 $V_{OUT}$ | PIN17 B.P. $R_{OUT}$ | PIN18 10V SPAN | PIN19 20V SPAN | PIN20 $\Sigma_J$ | PIN22 $V_{CC}$ | SWITCH POSITION $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | MEASURE VALUE | UNIT | EQUATIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reference Voltage Loaded | $V_{REF(L)}$ | All Bits OFF ($V_{IH}$ = 2V) 2.5mA Current Source From Pin 24 to GND. Bipolar Mode **±10V Range** | 5V | -15V | Pin 19 | Pin 20 | O.C | Pin 15 | Pin 17 | 15V | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | $E_{1R}$ $E_{1H}$ $E_{1L}$ | V | |
| Reference Voltage Unipolar Mode | $V_{REF(U)}$ | All Bits OFF ($V_{IH}$ = 2V) | 5V | -15V | Pin 18 | O.C | Pin 15 | O.C | O.C. | 15V | 2 | 2 | 1 | 1 | 1 | 2 | 1 | 1 | $E_{2R}$ $E_{2H}$ $E_{2L}$ | V | |
| Reference Voltage Bipolar Mode | $V_{REF(B)}$ | All Bits OFF ($V_{IH}$ = 2V) Bipolar Mode ±10V Range | 5V | -15V | Pin 19 | Pin 20 | O.C | Pin 15 | Pin 17 | 15V | 2 | 2 | 1 | 2 | 2 | 2 | 1 | 1 | $E_{3R}$ $E_{3H}$ $E_{3L}$ | V | |
| Unipolar Offset | $V_{OS}$ | All Bits OFF ($V_{IH}$ = 2V) | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C | O.C. | 15V | 3 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | $E_{4R}$ $E_{4H}$ $E_{4L}$ | V | $\frac{E_4}{10} \times 100 = \%\ FSR$ |
| Unipolar Gain Error | $A_{E1}$ | All Bits OFF to All Bits ON, ($V_{IH}$ = 2V, $V_{IL}$ = 0.8V) | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C | O.C. | 15V | 3 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | $E_{5R}$ $E_{5H}$ $E_{5L}$ | V | $\frac{\lvert(E_5-E_4)-9.99756\rvert}{10} \times 100 = \%\ FSR$ |
| Unipolar Gain Error Output Loaded | $A_{E2}$ | All Bits OFF to All Bits ON, ($V_{IH}$ = 2V, $V_{IL}$ = 0.8V) +5mA Current Source From $V_{OUT}$ to GND | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C | O.C. | 15V | 3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $E_{6R}$ $E_{6H}$ $E_{6L}$ | V | Calculation Same as Above |
| Unipolar Gain Error Output Loaded | $A_{E3}$ | All Bits OFF to All Bits ON, $V_{IL}$ = 0.8V -5mA Current Source From $V_{OUT}$ to GND | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C. | O.C. | 15V | 3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $E_{7R}$ $E_{7H}$ $E_{7L}$ | V | Calculation Same as Above |
| Power Supply Sensitivity From $V_{CC}$ | $+P_{SS1}$ | All Bits ON, $V_{IL}$ = 0.8V $V_{CC}$ = 16.5/11.4V Bipolar ±5V Range | 5V | -15V | Pin 18 | Pin 20 | Pin 15 | O.C. | Pin 17 | 16.5V 11.4V | 3 | 2 | 1 | 2 | 1 | 1 | 1 | 1 | $E_{8A}$ $E_{8B}$ | V | $\frac{E_{8A}-E_{8B}}{(10)(34\%)} \times 100 = \frac{\Delta\ \%\ FSR}{\%\ \Delta\ V_{CC}}$ |
| Power Supply Sensitivity From $V_{DD}$ | $+P_{SS2}$ | All Bits ON, $V_{IL}$ = 0.8V $V_{DD}$ = 5.5V/4.5V Bipolar ±5V Range | 5.5V 4.5V | -15V | Pin 18 | Pin 20 | Pin 15 | O.C. | Pin 17 | 15V | 3 | 2 | 1 | 2 | 1 | 1 | 1 | 1 | $E_{9A}$ $E_{9B}$ | V | $\frac{E_{9A}-E_{9B}}{(10)(34\%)} \times 100 = \frac{\Delta\ \%\ FSR}{\%\ \Delta\ V_{CC}}$ |
| Power Supply Sensitivity From $V_{EE}$ | $-P_{SS1}$ | All Bits ON, $V_{IL}$ = 0.8V $V_{EE}$ = -16.5/-11.4V Bipolar ±5V Range | 5V | -16.5V -11.4V | Pin 18 | Pin 20 | Pin 15 | O.C. | Pin 17 | 15V | 3 | 2 | 1 | 2 | 1 | 1 | 1 | 1 | $E_{10A}$ $E_{10B}$ | V | $\frac{E_{10A}-E_{10B}}{(10)(34\%)} \times 100 = \frac{\Delta\ \%\ FSR}{\%\ \Delta\ V_{EE}}$ |
| Bipolar Offset Error | $BP_{OE}$ | All Bits OFF, $V_{IH}$ = 2V ±10V Range | 5V | -15V | Pin 19 | Pin 20 | O.C. | Pin 15 | Pin 17 | 15V | 3 | 2 | 1 | 2 | 2 | 1 | 1 | 1 | $E_{11R}$ $E_{11H}$ $E_{11L}$ | V | $\frac{E_{11}*10}{20} \times 100 = \%\ FSR$ |

## CHART A. GROUP A TEST CONDITIONS (Continued)

Pin 24 Tied to Pin 16, and Pin 23 Open Unless Otherwise Noted. All Pin Number's Listed Refer to the 24 Lead DIP Package.

| TEST | SYMBOL | CONDITIONS | PIN13 $V_{DD}$ | PIN14 $V_{EE}$ | PIN15 $V_{OUT}$ | PIN17 B.P. ROUT | PIN18 10V SPAN | PIN19 20V SPAN | PIN20 $\Sigma_J$ | PIN22 $V_{CC}$ | SWITCH POSITION $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ | MEASURE VALUE | UNIT | EQUATIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bipolar Zero Error | $BP_{ZE}$ | MSB ON, $V_{IL}$ = 0.8V All Other Bits OFF, $V_{IH}$ = 2.0V ±10V Range | 5V | -15V | Pin 19 | Pin 20 | O.C. | Pin 15 | Pin 17 | 15V | 3 | 2 | 1 | 2 | 2 | 1 | 1 | 1 | $E_{12R}$ $E_{12H}$ $E_{12L}$ | V | $\frac{E_{12}}{20} \times 100 = \%$ FSR |
| Bipolar Gain Error | $BP_{AE}$ | All Bits OFF ($V_{IH}$ = 2V) to All Bits ON ($V_{IL}$ = 0.8V) ±10V Range | 5V | -15V | Pin 19 | Pin 20 | O.C. | Pin 15 | Pin 17 | 15V | 3 | 2 | 1 | 2 | 2 | 1 | 1 | 1 | $E_{13R}$ $E_{13H}$ $E_{13L}$ | V | $\left[\frac{(E_{13}-E_{11})-19.995}{20}\right] \times 100 = \%$ FSR |
| Integral Linearity Error | $L_E$ | Unipolar Mode 0 to 10V Range $V_{IL}$ = 0.8V, $V_{IH}$ = 2.0V | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C. | O.C. | 15V | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | $E_{LR}$ $E_{LH}$ $E_{LL}$ | V | $E_L$(1LSB) = LSBs of Error |
| Differential Linearity Error | $D_{LE}$ | Unipolar Mode 0 to 10V Range $V_{IL}$ = 0.8V, $V_{IH}$ = 2.0V | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C. | O.C. | 15V | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | $E_{DLR}$ $E_{DLH}$ $E_{DLL}$ | V | $E_{DL}$(1LSB) = LSBs of Error |
| Gain Adjust | $A_A$ | $V_S$ = 15V, RA = 2.8MΩ $V_S$ = -15V, RA = 2.8MΩ | 5V | -15V | Pin 18 | O.C. | Pin 15 | O.C. | O.C. | 15V | 3 | 2 | 1 | 1 | 1 | 1 | 2 | 1 | $E_{14}$ $E_{15}$ | V | $\frac{E_{14}-E_{5R}}{10} \times 100 = \%$FSR $\frac{E_{5R}-E_{15}}{10} \times 100 = \%$FSR |
| Positive Slew Rate | +SR | All Bits OFF ($V_{IH}$ = 2V) to All Bits ON ($V_{IL}$ = 0.8V) Bipolar ±10V Range | 5V | -15V | Pin 19 | Pin 20 | O.C. | Pin 15 | Pin 17 | 15V | 2 | 2 | 1 | 2 | 2 | 1 | 1 | 2 | $T_1$ $T_2$ | µs | $\frac{12V}{T_2-T_1} = \frac{V}{\mu s}$ |
| Negative Slew Rate | -SR | All Bits ON ($V_{IL}$ = 0.8V) to All Bits OFF ($V_{IH}$ = 2V) Bipolar ±10V Range | 5V | -15V | Pin 19 | Pin 20 | O.C. | Pin 15 | Pin 17 | 15V | 2 | 2 | 1 | 2 | 2 | 1 | 1 | 2 | $T_3$ $T_4$ | µs | $\frac{12V}{T_3-T_4} = \frac{V}{\mu s}$ |

| TEST | SYMBOL | CONDITIONS | TEMPERATURE | EQUATIONS |
|---|---|---|---|---|
| Reference Voltage Drift Unipolar Mode | $\frac{dV_{REF(U)}}{dT}$ | Calculations Made From Tests Previously Defined in this Chart | +25°C to +125°C | $\frac{(E_{2H}-E_{2R})10^6}{E_{2R}\ (100^oC)} = \frac{\text{PPM of } V_{REF}}{^oC}$ |
| | | | -55°C to +25°C | $\frac{(E_{2R}-E_{2L})10^6}{E_{2R}\ (80^oC)} = \frac{\text{PPM of } V_{REF}}{^oC}$ |
| Reference Voltage Drift Bipolar Mode | $\frac{dV_{REF(B)}}{dT}$ | Calculations Made From Tests Previously Defined in this Chart | +25°C to +125°C | $\frac{(E_{3H}-E_{3R})10^6}{E_{3R}\ (100^oC)} = \frac{\text{PPM of } V_{REF}}{^oC}$ |
| | | | -55°C to +25°C | $\frac{(E_{3R}-E_{3L})10^6}{E_{3R}\ (80^oC)} = \frac{\text{PPM of } V_{REF}}{^oC}$ |
| Unipolar Offset Drift | $\frac{dV_{OS}}{dT}$ | Calculations Made From Tests Previously Defined in this Chart | +25°C to +125°C | $\frac{(E_{4H}-E_{4R})10^6}{10\ (100^oC)} = \frac{\text{PPM of FSR}}{^oC}$ |
| | | | -55°C to +25°C | $\frac{(E_{4R}-E_{4L})10^6}{10\ (80^oC)} - \frac{\text{PPM of FSR}}{^oC}$ |

## CHART A. GROUP A TEST CONDITIONS (Continued)

Pin 24 Tied to Pin 16, and Pin 23 Open Unless Otherwise Noted. All Pin Number's Listed Refer to the 24 Lead DIP Package.

| TEST | SYMBOL | CONDITIONS | TEMPERATURE | EQUATIONS |
|---|---|---|---|---|
| Unipolar Gain Drift | $\frac{dA_{E1}}{dT}$ | Calculations Made From Tests Previously Defined in this Chart | +25°C to +125°C | $\left[\frac{(E_{5H}-E_{4H})-(E_{5R}-E_{4R})}{10\ (100^{\circ}C)}\right]10^6 = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| | | | -55°C to +25°C | $\left[\frac{(E_{5R}-E_{4R})-(E_{5L}-E_{4L})}{10\ (80^{\circ}C)}\right]10^6 = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| Unipolar Gain Drift Exclusive of the Internal Reference | $\frac{dA_{E2}}{dT}$ | Calculations Made From Tests Previously Defined in this Chart | +25°C to +125°C | $\left[\frac{(E_{5H}-E_{4H})-(E_{5R}-E_{4R})}{10} - \frac{(E_{2H}-E_{2R})}{6.3}\right]\frac{10^6}{100^{\circ}C} = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| | | | -55°C to +25°C | $\left[\frac{(E_{5R}-E_{4R})-(E_{5L}-E_{4L})}{10} - \frac{(E_{2R}-E_{2L})}{6.3}\right]\frac{10^6}{80^{\circ}C} = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| Total Unipolar Error | $U_{ET}$ | Calculations Made From Tests Previously Defined in This Chart | +25°C to +125°C | $\frac{(E_{5H}-E_{5R})}{10}\ (100) = \%\ \text{FSR}$ |
| | | | -55°C to +25°C | $\frac{(E_{5R}-E_{5L})}{10}\ (100) = \%\ \text{FSR}$ |
| Bipolar Offset Drift | $\frac{dBP_{OE}}{dT}$ | Calculations Made From Tests Previously Defined in This Chart | +25°C to +125°C | $\frac{(E_{11H}-E_{11R})\ 10^6}{20\ (100^{\circ}C)} = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| | | | -55°C to +25°C | $\frac{(E_{11R}-E_{11L})\ 10^6}{20\ (80^{\circ}C)} = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| Bipolar Gain Drift | $\frac{dBP_{AE1}}{dT}$ | Calculations Made From Tests Previously Defined in This Chart | +25°C to +125°C | $\left[\frac{(E_{13H}-E_{11H})-(E_{13R}-E_{11R})}{20\ (100^{\circ}C)}\right]10^6 = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| | | | -55°C to +25°C | $\left[\frac{(E_{13R}-E_{11R})-(E_{13L}-E_{11L})}{20\ (80^{\circ}C)}\right]10^6 = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| Bipolar Gain Drift Exclusive of the Internal Reference | $\frac{dBA_{E2}}{dT}$ | Calculations Made From Tests Previously Defined in This Chart | +25°C to +125°C | $\left[\frac{(E_{13H}-E_{11H})-(E_{13R}-E_{11R})}{20} - \frac{(E_{3H}-E_{3R})}{6.3}\right]\frac{10^6}{100^{\circ}C} = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| | | | -55°C to +25°C | $\left[\frac{(E_{13R}-E_{11R})-(E_{13L}-E_{11L})}{20} - \frac{(E_{3R}-E_{3L})}{6.3}\right]\frac{10^6}{80^{\circ}C} = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| Total Bipolar Error | $B_{ET}$ | Calculations Made From Tests Previously Defined in This Chart | +25°C to +125°C | $\frac{(E_{13H}-E_{13R})}{20}\ (100) = \%\ \text{FSR}$ |
| | | | -55°C to +25°C | $\frac{(E_{13R}-E_{13L})}{20}\ (100) = \%\ \text{FSR}$ |
| Total Bipolar Drift | $\frac{dBp}{dT}$ | Calculations Made From Tests Previously Defined in This Chart | +25°C to +125°C | $\frac{(E_{13H}-E_{13R})\ 10^6}{20\ (100^{\circ}C)} = \frac{\text{PPM of FSR}}{^{\circ}C}$ |
| | | Includes Gain, Offset and Linearity Drift | -55°C to +25°C | $\frac{(E_{13R}-E_{13L})\ 10^6}{20\ (80^{\circ}C)} = \frac{\text{PPM of FSR}}{^{\circ}C}$ |

## Waveforms

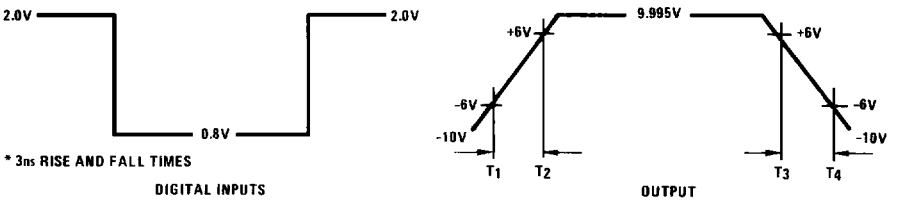



FIGURE 2. SLEW RATE WAVEFORMS

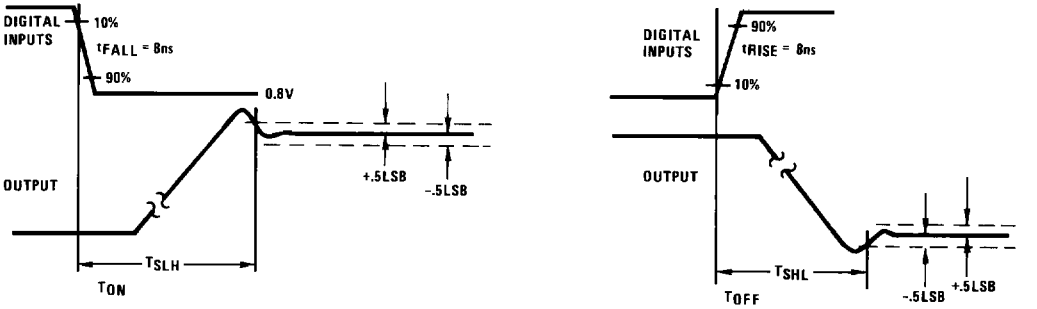



FIGURE 3. SETTLING TIME WAVEFORMS

## Test Circuit

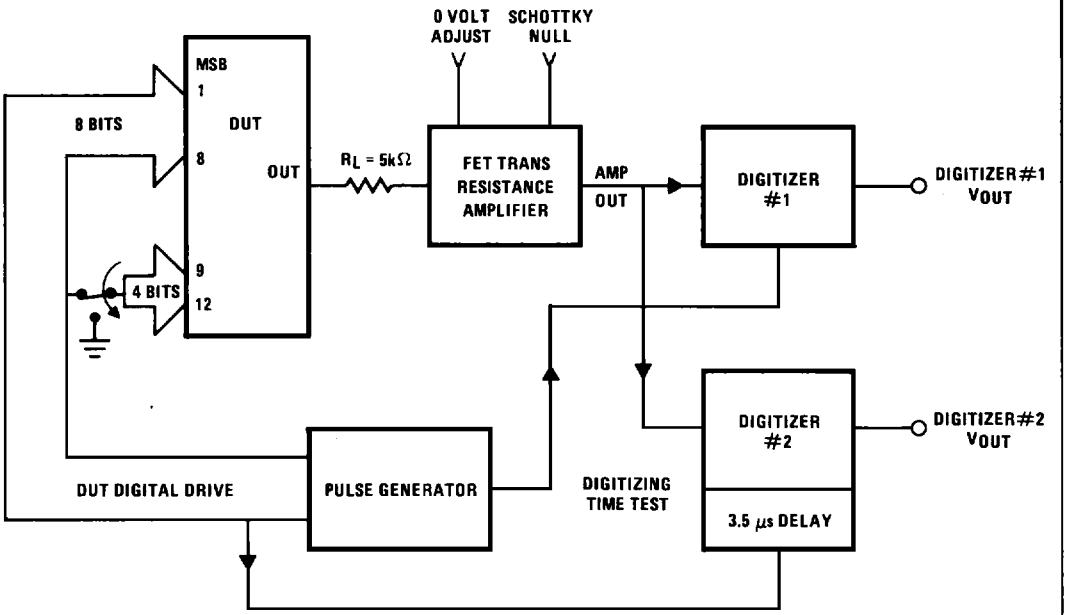



FIGURE 4. SETTLING TIME TEST FIXTURE

CHART B.

| DIGITAL CODE (MSB ——— LSB) | NOTE | DIGITAL CODE (MSB ——— LSB) | NOTE |
|---|---|---|---|
| 1 1 1 1 1 1 1 1 1 1 1 0 | | 1 0 0 1 X X X X X X X X | 9 |
| 1 1 1 1 1 1 1 1 1 1 0 1 | | 1 0 0 0 X X X X X X X X | 8 |
| 1 1 1 1 1 1 1 1 1 0 1 1 | | 1 0 0 0 X X X X X X X X | 9 |
| 1 1 1 1 1 1 1 1 0 1 1 1 | | 0 1 1 1 X X X X X X X X | 8 |
| 1 1 1 1 1 1 1 0 1 1 1 1 | | 0 1 1 1 X X X X X X X X | 9 |
| 1 1 1 1 1 1 0 1 1 1 1 1 | | 0 1 1 0 X X X X X X X X | 8 |
| 1 1 1 1 1 0 1 1 1 1 1 1 | | 0 1 1 0 X X X X X X X X | 9 |
| 1 1 1 1 0 1 1 1 1 1 1 1 | | 0 1 0 1 X X X X X X X X | 8 |
| 1 1 1 0 1 1 1 1 1 1 1 1 | | 0 1 0 1 X X X X X X X X | 9 |
| 1 1 0 1 1 1 1 1 1 1 1 1 | | 0 1 0 0 X X X X X X X X | 8 |
| 1 0 1 1 1 1 1 1 1 1 1 1 | | 0 1 0 0 X X X X X X X X | 9 |
| 0 1 1 1 1 1 1 1 1 1 1 1 | | 0 0 1 1 X X X X X X X X | 8 |
| 1 1 1 0 X X X X X X X X | 8 | 0 0 1 1 X X X X X X X X | 9 |
| 1 1 1 0 X X X X X X X X | 9 | 0 0 1 0 X X X X X X X X | 8 |
| 1 1 0 1 X X X X X X X X | 8 | 0 0 1 0 X X X X X X X X | 9 |
| 1 1 0 1 X X X X X X X X | 9 | 0 0 0 1 X X X X X X X X | 8 |
| 1 1 0 0 X X X X X X X X | 8 | 0 0 0 1 X X X X X X X X | 9 |
| 1 1 0 0 X X X X X X X X | 9 | 0 0 0 0 X X X X X X X X | 8 |
| 1 0 1 1 X X X X X X X X | 8 | 0 0 0 0 X X X X X X X X | 9 |
| 1 0 1 1 X X X X X X X X | 9 | X X X X X X X X X X X X | 8 |
| 1 0 1 0 X X X X X X X X | 8 | X X X X X X X X X X X X | 9 |
| 1 0 1 0 X X X X X X X X | 9 | | |
| 1 0 0 1 X X X X X X X X | 8 | | |

NOTES: 8. X = 0 ($V_{IL}$ = 0.8V) if the linearity error for that bit was measured as a positive error. X = 1 ($V_{IH}$ = 2.0V) if the linearity error for that bit was measured as a negative error.

9. X = 0 ($V_{IL}$ = 0.8V) if the linearity error for that bit was measured as a negative error. X = 1 ($V_{IH}$ = 2.0V) if the linearity error for that bit was measured as a positive error.

**Integral Linearity Error Measurements**

The transfer characteristics of the DUT are first determined by measuring its end points (all bits OFF, all bits ON). The end points of the reference DAC are then matched to the DUTs through software and hardware adjustments, to establish an ideal transfer characteristic for the DUT. The reference DAC then supplies one 12-bit LSB (DUT, all Bits OFF) to the input of the error amplifier and $R_T$ is adjusted to obtain an output of 1V. The integral linearity error, measured at the output of the error amplifier is the difference between the ideal voltage supplied by the reference DAC and the output voltage of the DUT for the code under test

$$\text{LSB's of Error} = (\text{Ideal voltage} - \text{measured voltage}) \times \frac{\text{LSB's}}{\text{Volt}}$$

CHART C.

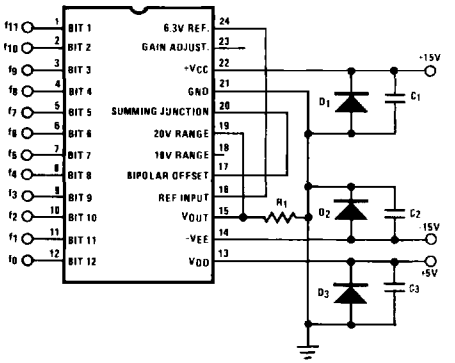
| TO CODE | | | | | | | | | | | | FROM CODE | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | | | | | LSB | MSB | | | | | | | | | | | LSB |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Differential Linearity Error Measurements**

The DUT and the reference DAC supply the code under test to the input of the error amplifier, and the resulting output error is measured ($E_1$). The digital code of the DUT is then increased by 1LSB and the output error is measured a second time ($E_2$). The differential linearity error is calculated as, $\frac{(E_2 - E_1)}{\text{Volts/LSB}}$ - 1LSB = LSB's of error.

## Burn-In Circuits

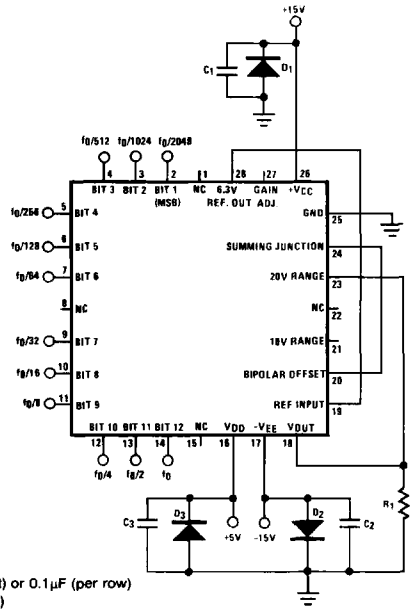
### HI-5687V/883 (CERAMIC SIDEBRAZE DIP)




NOTES:
$R_1$ = 2.0kΩ, ± 5%, 1/2 or 1/4 Watt
$C_1$ - $C_3$ = 0.01µF (one each per socket) or 0.1µF (per row)
$D_1$ - $D_3$ = 1N4003 (one each per board)

| | | | |
|---|---|---|---|
| $f_0$ = 100kHz | TTL Logic Levels | $f_6 = f_0/64$ | TTL Logic Levels |
| $f_1 = f_0/2$ | 50% Duty Cycle | $f_7 = f_0/128$ | 50% Duty Cycle |
| $f_2 = f_0/4$ | | $f_8 = f_0/256$ | |
| $f_3 = f_0/8$ | | $f_9 = f_0/512$ | |
| $f_4 = f_0/16$ | | $f_{10} = f_0/1024$ | |
| $f_5 = f_0/32$ | | $f_{11} = f_0/2048$ | |

### HI-5687V/883 (CERAMIC LCC)




NOTES:
$R_1$ = 2.0kΩ, ± 5%, 1/2 or 1/4 Watt
$C_1$ - $C_3$ = 0.01µF (one each per socket) or 0.1µF (per row)
$D_1$ - $D_3$ = IN4002 (one each per board)
$F_0$ = 100kHz (TTL Logic Level), 50% Duty Cycle

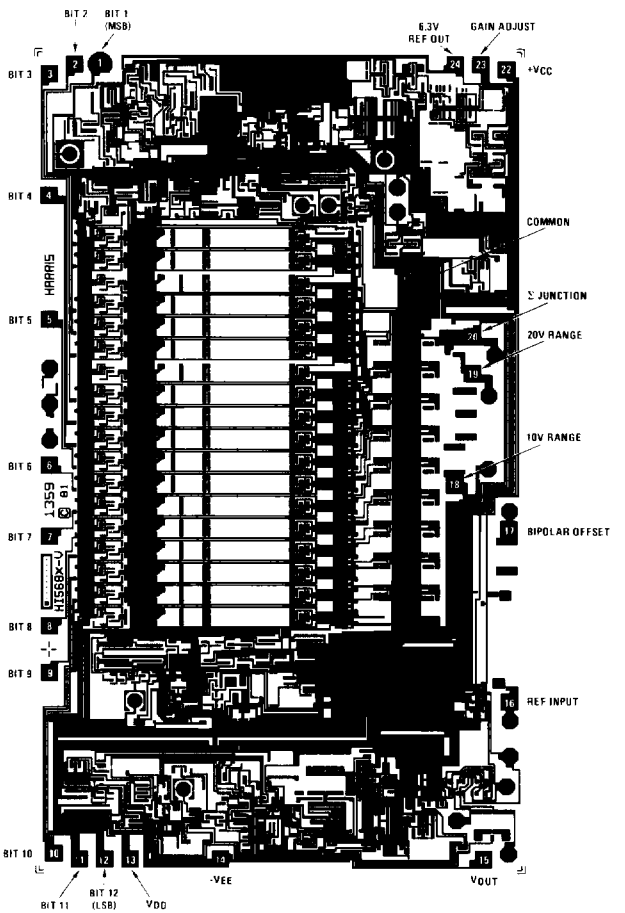
## Die Characteristics

**DIE DIMENSIONS:** 125 x 210 x 19 mils
**METALLIZATION:**
Type: Al
Thickness: 16kÅ ± 2kÅ
**GLASSIVATION:**
Type: Silox
Thickness: 14kÅ ± 2.0kÅ
**WORST CASE CURRENT DENSITY:** $2.26 \times 10^5 A/cm^2$
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

**TRANSISTOR COUNT:** 259
**PROCESS:** Bipolar-DI
**DIE ATTACH:**
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)
Ceramic LCC - 420°C (Max)

## Metallization Mask Layout

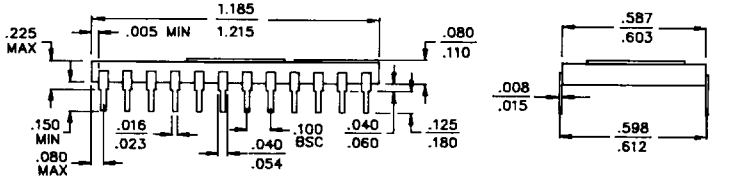
**HI-5687V/883**




NOTE: Pad Numbers Correspond to DIP Package Only.

## Packaging †

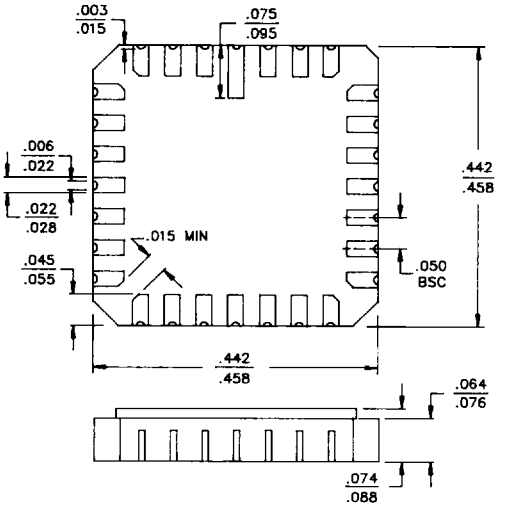
### 24 PIN CERAMIC SIDEBRAZE DIP




**LEAD MATERIAL:** Type B
**LEAD FINISH:** Type C
**PACKAGE MATERIAL:** Multilayer Ceramic, 90% Alumina
**PACKAGE SEAL:**
Material: Gold/Tin (80/20)
Temperature: 450°C ±10°C
Method: Furnace Seal

**INTERNAL LEAD WIRE:**
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
**COMPLIANT OUTLINE:** 38510 D-3

### 28 PAD CERAMIC LCC




**PAD MATERIAL:** Type C
**PAD FINISH:** Type A
**FINISH DIMENSION:** Type A
**PACKAGE MATERIAL:** Multilayer Ceramic, 90% Alumina
**PACKAGE SEAL:**
Material: Gold/Tin (80/20)
Temperature: 320°C ±10°C
Method: Furnace Braze

**INTERNAL LEAD WIRE:**
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
**COMPLIANT OUTLINE:** 38510 C-4

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

## DESIGN INFORMATION

# Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter

*The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.*

## *Definitions of Specifications*

### Digital Inputs

The HI-5687V accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

| DIGITAL INPUT | ANALOG OUTPUT | | |
|---|---|---|---|
| | COMPLEMENTARY BINARY | COMPLEMENTARY OFFSET BINARY | COMPLEMENTARY TWO's COMPLEMENT* |
| MSB LSB | | | |
| 000 . . . 000 | +Full Scale | +Full Scale | -LSB |
| 100 . . . 000 | Mid Scale -1 LSB | -1 LSB | +Full Scale |
| 111 . . . 111 | Zero | -Full Scale | Zero |
| 011 . . . 111 | +1/2 Full Scale | Zero | -Full Scale |

*Invert MSB with external inverter to obtain CTC Coding

### Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 10% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12 bit system ±1/2 LSB = ±0.012% of FSR.

### Thermal Drift

Thermal drift is based on measurements at +25°C, +125°C ($T_H$) and -55°C ($T_L$). Drift calculations are made for the high (+125°C, +25°C) and low (+25°C, -55°C) ranges, and the larger of the two values is given as a specification representing worstcase drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta \text{ FSR}/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta \text{ Offset}/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta V_{REF}/\Delta^{\circ}\text{C}}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{\Delta V_O/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage - Zero Scale Output Voltage

Δ FSR = FSR (+125°C) - FSR (+25°C)

or FSR (+25°C) - FSR (-55°C)

$V_O$ = Steady-state response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code.

### Accuracy

LINEARITY ERROR—(Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".)- The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL LINEARITY ERROR—The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY—The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

TOTAL ERROR—The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

### Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in $+V_{CC}$, $V_{DD}$ or $-V_{EE}$ supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

# DESIGN INFORMATION (Continued)

*The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied. Pin numbers correspond to DIP package only.*

$$P.S.S. = \frac{\frac{\Delta \text{ Full Scale Range} \times 100}{\text{Full Scale Range (Nominal)}}}{\frac{\Delta V \times 100}{V \text{ (Nominal)}}}$$

### Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale, i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

### Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 5 should be used. Decoupling capacitors should be connected close to the HI-5687V (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

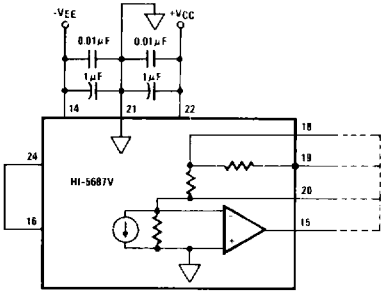



FIGURE 5.

### Reference Supply

An internal 6.3 Volt reference is provided on board the HI-5687V models. This voltage reference (pin 24) must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5687V. All gain adjustments should be made under constant load conditions.

### Output Voltage Ranges

HI-5687V

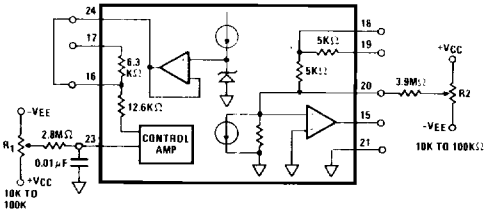



FIGURE 6.

RANGE CONNECTIONS

| | RANGE | CONNECT PIN 15 | CONNECT PIN 17 | CONNECT PIN 19 |
|---|---|---|---|---|
| Unipolar | 0 to +5V | 18 | N.C. | 20 |
| | 0 to +10V | 18 | N.C. | N.C. |
| Bipolar | -2.5V | 18 | 20 | 20 |
| | ±5.0V | 18 | 20 | N.C. |
| | ±10V | 19 | 20 | 15 |

### Gain and Offset Calibration

**UNIPOLAR CALIBRATION**

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust $R_2$ for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust $R_1$ for FS-1LSB

That is:
4.9988 for 0 to +5V range
9.9976 for 0 to +10V range

**BIPOLAR CALIBRATION**

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R2 for Negative FS

That Is:
-10V for ±10V range
-5V for ±5V range
-2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R1 for positive FS-1LSB

That is:
+9.9951V for ±10V range
+4.9976V for ±5V range
+2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

## DESIGN INFORMATION (Continued)

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### TYPICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMP | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| Output Impedance | $Z_O$ | Closed Loop, DC | 10 | +25°C | — | 0.05 | — | Ω |
| Internal Reference Output Impedance | $REF_{OUT}$ | DC | 10 | +25°C | — | 1.5 | — | Ω |
| Output Short Circuit to GND | $I_{SC}$ | Pin 15 to GND, Unipolar 10V Range, All Bits ON | 10, 11 | +25°C | — | 40 | — | mA |

NOTES: 10. The parameters listed in this Table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

11. Under short circuit conditions, the amplifier will current limit. The duty cycle must not exceed 2.7% to maintain an acceptable current density level.