

# NEC

## DATA SHEET

# MOS INTEGRATED CIRCUIT

# $\mu$ PD464318L, 464336L

### 4M-BIT Bi-CMOS SYNCHRONOUS FAST STATIC RAM

### 256K-WORD BY 18-BIT / 128K-WORD BY 36-BIT

### HSTL INTERFACE

#### Description

The  $\mu$ PD464318L is a 262,144 words by 18 bits, and the  $\mu$ PD464336L is a 131,072 words by 36 bits synchronous static RAM fabricated with advanced Bi-CMOS technology using N-channel memory cell.

This technology and unique peripheral circuits make the  $\mu$ PD464318L and  $\mu$ PD464336L a high-speed device. The  $\mu$ PD464318L and  $\mu$ PD464336L are suitable for applications which require high-speed, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

These are packaged in a 119-pin plastic BGA (Ball Grid Array).

#### Features

- Fully synchronous operation
- Fast clock access time : 2.6 ns / 200 MHz, 3.0 ns / 167 MHz, 3.5 ns / 154 MHz
- Single Differential Single clock, Registered Input / Registered Output
- Asynchronous output enable control : /G
- Byte write control : /SBa (DQa1-9), /SBb (DQb1-9), /SBc (DQc1-9), /SBd (DQd1-9)
- Common I/O using three-state outputs
- Internally self-timed write cycle
- Late write with 1 dead cycle between Read-Write
- User-configurable outputs :  
Controlled impedance outputs or push-pull outputs
- Boundary scan (JTAG) IEEE 1149.1 compatible
- 3.3 V (Chip) / 1.5V (I/O) supply

#### Ordering Information

| Part number           | Access time | Clock frequency | Package             |
|-----------------------|-------------|-----------------|---------------------|
| $\mu$ PD464318LS1-A5  | 2.6 ns      | 200 MHz         | 119-pin plastic BGA |
| $\mu$ PD464318LS1-A6  | 3.0 ns      | 167 MHz         |                     |
| $\mu$ PD464318LS1-A65 | 3.5 ns      | 154 MHz         |                     |
| $\mu$ PD464336LS1-A5  | 2.6 ns      | 200 MHz         |                     |
| $\mu$ PD464336LS1-A6  | 3.0 ns      | 167 MHz         |                     |
| $\mu$ PD464336LS1-A65 | 3.5 ns      | 154 MHz         |                     |

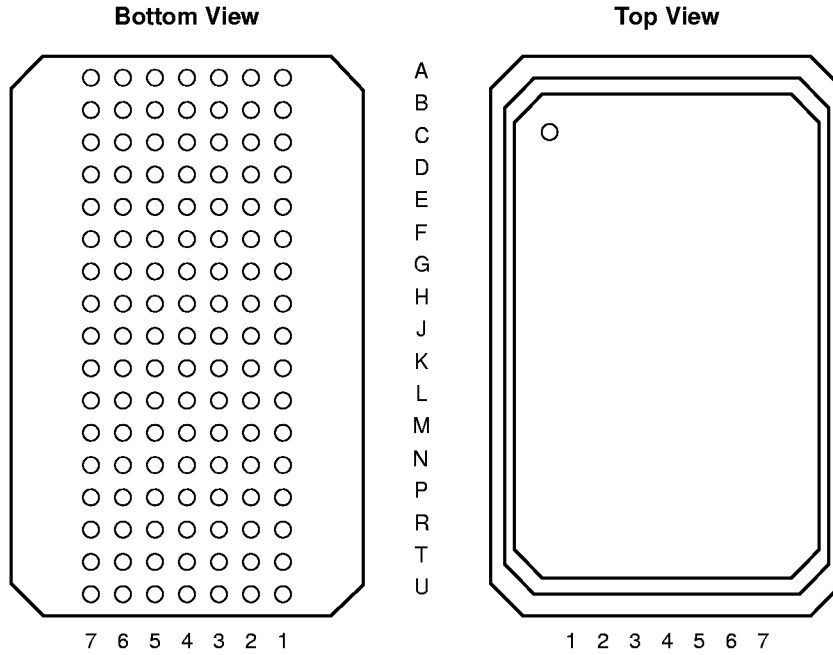
The information in this document is subject to change without notice.

**Pin Configurations**

/xxx indicates active low signal.

**119-pin Plastic BGA (256K Words by 18 Bits Pin Assignment)**

[ μPD464318LS1 ]



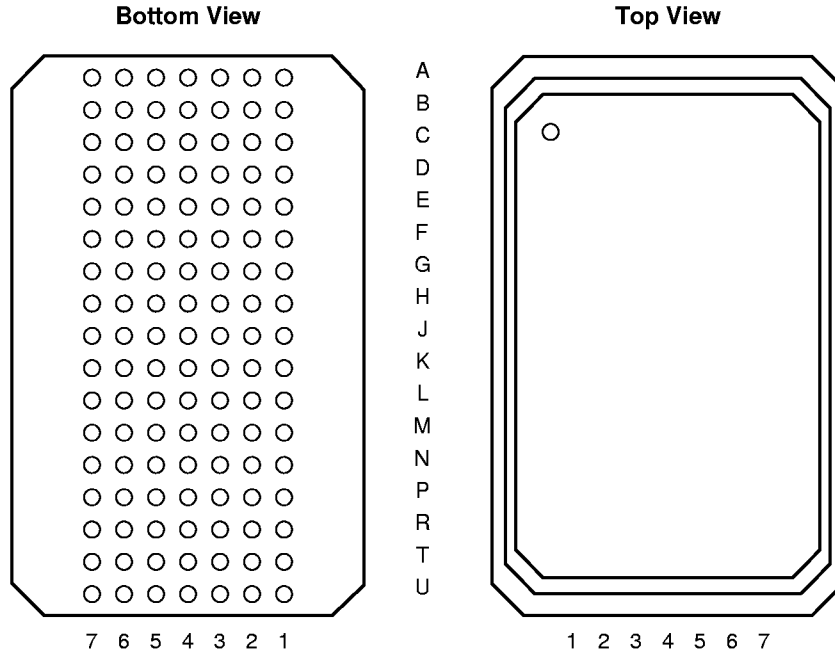
|   | 7       |                  | 6       |                 | 5       |                  | 4       |                 | 3       |                  | 2       |                 | 1       |                  |
|---|---------|------------------|---------|-----------------|---------|------------------|---------|-----------------|---------|------------------|---------|-----------------|---------|------------------|
|   | Pin No. | Func.            | Pin No. | Func.           | Pin No. | Func.            | Pin No. | Func.           | Pin No. | Func.            | Pin No. | Func.           | Pin No. | Func.            |
| A | A7      | V <sub>DDQ</sub> | A6      | SA2             | A5      | SA6              | A4      | NC              | A3      | SA9              | A2      | SA12            | A1      | V <sub>DDQ</sub> |
| B | B7      | NC               | B6      | NC              | B5      | SA16             | B4      | NC              | B3      | SA17             | B2      | NC              | B1      | NC               |
| C | C7      | NC               | C6      | SA3             | C5      | SA7              | C4      | V <sub>DD</sub> | C3      | SA10             | C2      | SA13            | C1      | NC               |
| D | D7      | NC               | D6      | DQa9            | D5      | V <sub>SS</sub>  | D4      | ZQ              | D3      | V <sub>SS</sub>  | D2      | NC              | D1      | DQb1             |
| E | E7      | DQa8             | E6      | NC              | E5      | V <sub>SS</sub>  | E4      | /SS             | E3      | V <sub>SS</sub>  | E2      | DQb2            | E1      | NC               |
| F | F7      | V <sub>DDQ</sub> | F6      | DQa7            | F5      | V <sub>SS</sub>  | F4      | /G              | F3      | V <sub>SS</sub>  | F2      | NC              | F1      | V <sub>DDQ</sub> |
| G | G7      | DQa6             | G6      | NC              | G5      | V <sub>SS</sub>  | G4      | NC              | G3      | /SBb             | G2      | DQb3            | G1      | NC               |
| H | H7      | NC               | H6      | DQa5            | H5      | V <sub>SS</sub>  | H4      | NC              | H3      | V <sub>SS</sub>  | H2      | NC              | H1      | DQb4             |
| J | J7      | V <sub>DDQ</sub> | J6      | V <sub>DD</sub> | J5      | V <sub>REF</sub> | J4      | V <sub>DD</sub> | J3      | V <sub>REF</sub> | J2      | V <sub>DD</sub> | J1      | V <sub>DDQ</sub> |
| K | K7      | DQa4             | K6      | NC              | K5      | V <sub>SS</sub>  | K4      | K               | K3      | V <sub>SS</sub>  | K2      | DQb5            | K1      | NC               |
| L | L7      | NC               | L6      | DQa3            | L5      | /SBa             | L4      | /K              | L3      | V <sub>SS</sub>  | L2      | NC              | L1      | DQb6             |
| M | M7      | V <sub>DDQ</sub> | M6      | NC              | M5      | V <sub>SS</sub>  | M4      | /SW             | M3      | V <sub>SS</sub>  | M2      | DQb7            | M1      | V <sub>DDQ</sub> |
| N | N7      | NC               | N6      | DQa2            | N5      | V <sub>SS</sub>  | N4      | SA1             | N3      | V <sub>SS</sub>  | N2      | NC              | N1      | DQb8             |
| P | P7      | DQa1             | P6      | NC              | P5      | V <sub>SS</sub>  | P4      | SA0             | P3      | V <sub>SS</sub>  | P2      | DQb9            | P1      | NC               |
| R | R7      | NC               | R6      | SA4             | R5      | V <sub>DD</sub>  | R4      | V <sub>DD</sub> | R3      | V <sub>SS</sub>  | R2      | SA14            | R1      | NC               |
| T | T7      | NC               | T6      | SA5             | T5      | SA8              | T4      | NC              | T3      | SA11             | T2      | SA15            | T1      | NC               |
| U | U7      | V <sub>DDQ</sub> | U6      | NC              | U5      | TDO              | U4      | TCK             | U3      | TDI              | U2      | TMS             | U1      | V <sub>DDQ</sub> |

**Pin Name and Functions**

| Pin name     | Description                       | Function                          |
|--------------|-----------------------------------|-----------------------------------|
| VDD          | Core Power Supply                 | Supplies power for RAM core       |
| VSS          | Ground                            |                                   |
| VDDQ         | Output Power Supply               | Supplies power for output buffers |
| VREF         | Input Reference                   |                                   |
| K, /K        | Main Clock Input                  |                                   |
| SA0 to SA17  | Synchronous Address Input         |                                   |
| DQa1 to DQb9 | Synchronous Data Input / Output   |                                   |
| /SS          | Synchronous Chip Select           | Logically selects SRAM            |
| /SW          | Synchronous Byte Write Enable     |                                   |
| /SBa         | Synchronous Byte "a" Write Enable | Write DQa1 to DQa9                |
| /SBb         | Synchronous Byte "b" Write Enable | Write DQb1 to DQb9                |
| /G           | Asynchronous Output Enable        | Asynchronous input                |
| ZQ           | Output Impedance Control          |                                   |
| NC           | No Connection                     |                                   |
| TMS          | Test Mode Select (JTAG)           |                                   |
| TDI          | Test Data Input (JTAG)            |                                   |
| TCK          | Test Clock Input (JTAG)           |                                   |
| TDO          | Test Data Output (JTAG)           |                                   |

119-pin plastic BGA (128K Words by 36 Bits Pin Assignment)

[ μPD464336LS1 ]

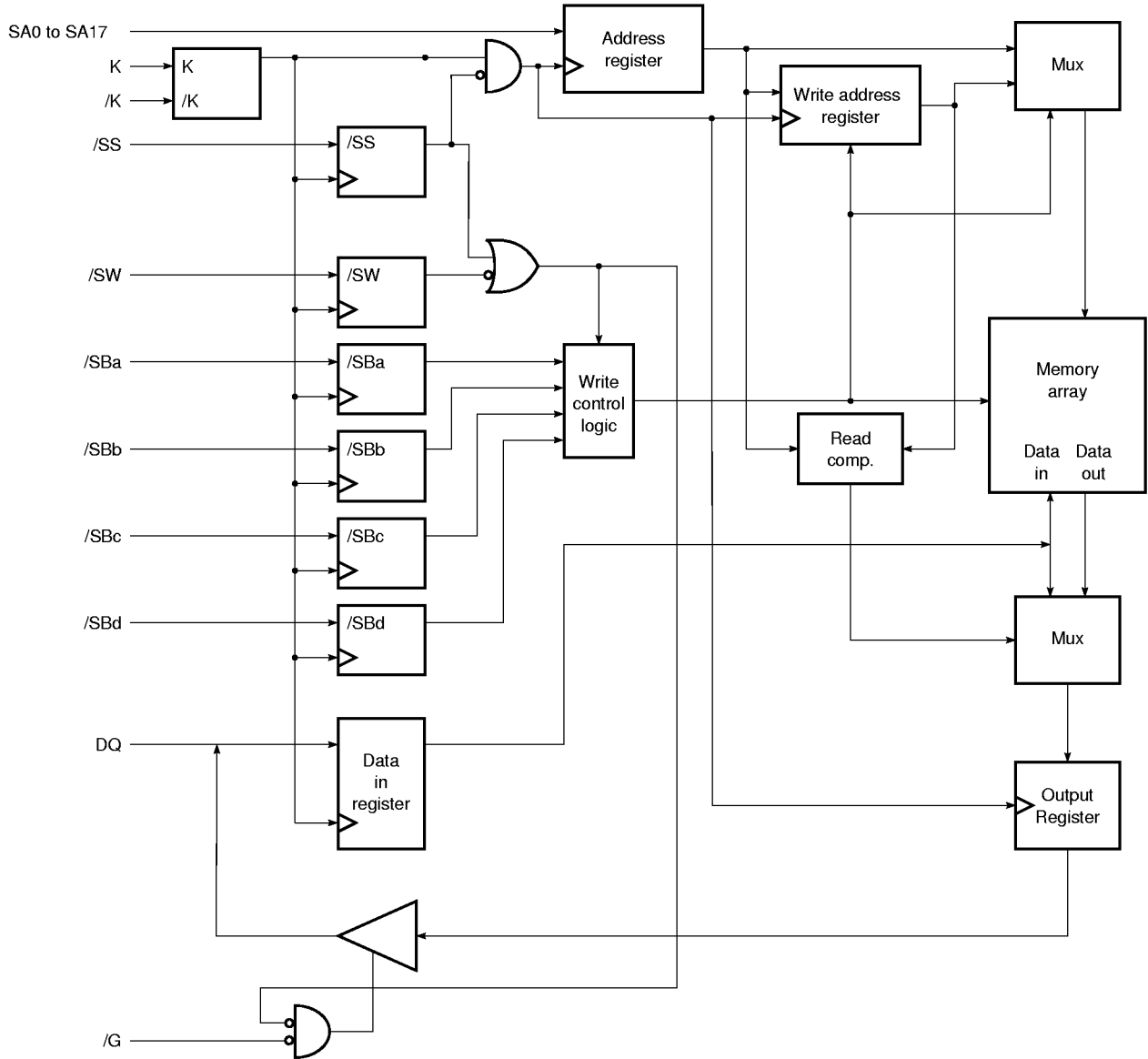


|   | 7       |                  | 6       |                 | 5       |                  | 4       |                 | 3       |                  | 2       |                 | 1       |                  |
|---|---------|------------------|---------|-----------------|---------|------------------|---------|-----------------|---------|------------------|---------|-----------------|---------|------------------|
|   | Pin No. | Func.            | Pin No. | Func.           | Pin No. | Func.            | Pin No. | Func.           | Pin No. | Func.            | Pin No. | Func.           | Pin No. | Func.            |
| A | A7      | V <sub>DDQ</sub> | A6      | SA2             | A5      | SA5              | A4      | NC              | A3      | SA9              | A2      | SA12            | A1      | V <sub>DDQ</sub> |
| B | B7      | NC               | B6      | NC              | B5      | SA15             | B4      | NC              | B3      | SA16             | B2      | NC              | B1      | NC               |
| C | C7      | NC               | C6      | SA3             | C5      | SA6              | C4      | V <sub>DD</sub> | C3      | SA10             | C2      | SA13            | C1      | NC               |
| D | D7      | DQb8             | D6      | DQb9            | D5      | V <sub>SS</sub>  | D4      | ZQ              | D3      | V <sub>SS</sub>  | D2      | DQc9            | D1      | DQc8             |
| E | E7      | DQb6             | E6      | DQb7            | E5      | V <sub>SS</sub>  | E4      | /SS             | E3      | V <sub>SS</sub>  | E2      | DQc7            | E1      | DQc6             |
| F | F7      | V <sub>DDQ</sub> | F6      | DQb5            | F5      | V <sub>SS</sub>  | F4      | /G              | F3      | V <sub>SS</sub>  | F2      | DQc5            | F1      | V <sub>DDQ</sub> |
| G | G7      | DQb3             | G6      | DQb4            | G5      | /SBb             | G4      | NC              | G3      | /SBc             | G2      | DQc4            | G1      | DQc3             |
| H | H7      | DQb1             | H6      | DQb2            | H5      | V <sub>SS</sub>  | H4      | NC              | H3      | V <sub>SS</sub>  | H2      | DQc2            | H1      | DQc1             |
| J | J7      | V <sub>DDQ</sub> | J6      | V <sub>DD</sub> | J5      | V <sub>REF</sub> | J4      | V <sub>DD</sub> | J3      | V <sub>REF</sub> | J2      | V <sub>DD</sub> | J1      | V <sub>DDQ</sub> |
| K | K7      | DQa1             | K6      | DQa2            | K5      | V <sub>SS</sub>  | K4      | K               | K3      | V <sub>SS</sub>  | K2      | DQd2            | K1      | DQd1             |
| L | L7      | DQa3             | L6      | DQa4            | L5      | /SBa             | L4      | /K              | L3      | /SBd             | L2      | DQd4            | L1      | DQd3             |
| M | M7      | V <sub>DDQ</sub> | M6      | DQa5            | M5      | V <sub>SS</sub>  | M4      | /SW             | M3      | V <sub>SS</sub>  | M2      | DQd5            | M1      | V <sub>DDQ</sub> |
| N | N7      | DQa6             | N6      | DQa7            | N5      | V <sub>SS</sub>  | N4      | SA1             | N3      | V <sub>SS</sub>  | N2      | DQd7            | N1      | DQd6             |
| P | P7      | DQa8             | P6      | DQa9            | P5      | V <sub>SS</sub>  | P4      | SA0             | P3      | V <sub>SS</sub>  | P2      | DQd9            | P1      | DQd8             |
| R | R7      | NC               | R6      | SA4             | R5      | V <sub>DD</sub>  | R4      | V <sub>DD</sub> | R3      | V <sub>SS</sub>  | R2      | SA14            | R1      | NC               |
| T | T7      | NC               | T6      | NC              | T5      | SA7              | T4      | SA8             | T3      | SA11             | T2      | NC              | T1      | NC               |
| U | U7      | V <sub>DDQ</sub> | U6      | NC              | U5      | TDO              | U4      | TCK             | U3      | TDI              | U2      | TMS             | U1      | V <sub>DDQ</sub> |

**Pin Name and Functions**

| Pin name     | Description                       | Function                          |
|--------------|-----------------------------------|-----------------------------------|
| VDD          | Core Power Supply                 | Supplies power for RAM core       |
| VSS          | Ground                            |                                   |
| VDDQ         | Output Power Supply               | Supplies power for output buffers |
| VREF         | Input Reference                   |                                   |
| K, /K        | Main Clock                        |                                   |
| SA0 to SA16  | Synchronous Address Input         |                                   |
| DQa1 to DQd9 | Synchronous Data Input / Output   |                                   |
| /SS          | Synchronous Chip Select           | Logically selects SRAM            |
| /SW          | Synchronous Byte Write Enable     |                                   |
| /SBa         | Synchronous Byte "a" Write Enable | Write DQa1 to DQa9                |
| /SBb         | Synchronous Byte "b" Write Enable | Write DQb1 to DQb9                |
| /SBc         | Synchronous Byte "c" Write Enable | Write DQc1 to DQc9                |
| /SBd         | Synchronous Byte "d" Write Enable | Write DQd1 to DQd9                |
| /G           | Asynchronous Output Enable        | Asynchronous input                |
| ZQ           | Output Impedance Control          |                                   |
| NC           | No Connection                     |                                   |
| TMS          | Test Mode Select (JTAG)           |                                   |
| TDI          | Test Data Input (JTAG)            |                                   |
| TCK          | Test Clock Input (JTAG)           |                                   |
| TDO          | Test Data Output (JTAG)           |                                   |

★ Late Write Block Diagram



**Synchronous Truth Table**

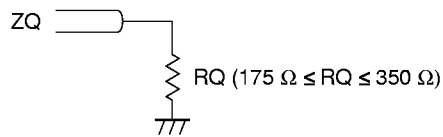
| /SS | /SW | /SBa | /SBb | /SBc | /SBd | Mode         | DQa1-9 | DQb1-9 | DQc1-9 | DQd1-9 | Power  |
|-----|-----|------|------|------|------|--------------|--------|--------|--------|--------|--------|
| H   | x   | x    | x    | x    | x    | Not selected | Hi-Z   | Hi-Z   | Hi-Z   | Hi-Z   | Active |
| L   | H   | x    | x    | x    | x    | Read         | Dout   | Dout   | Dout   | Dout   | Active |
| L   | L   | L    | L    | L    | L    | Write        | Din    | Din    | Din    | Din    | Active |
| L   | L   | L    | H    | H    | H    | Write        | Din    | Hi-Z   | Hi-Z   | Hi-Z   | Active |
| L   | L   | H    | L    | L    | L    | Write        | Hi-Z   | Din    | Din    | Din    | Active |

**Remark** x : Don't care

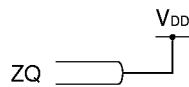
**Mode Select (Output Buffer)**

| ZQ       | Mode  | Notes |
|----------|---|-------|
| IZQ × RQ | Controlled impedance push-pull output buffer mode | 1     |
| VDD      | Push-Pull output buffer mode                      | 2     |

**Notes** 1. See figure.



2. See figure.



**Electrical Specifications**

**Absolute Maximum Ratings**

| Parameter              | Symbol           | Condition | MIN. | TYP. | MAX.                   | Unit | Note |
|------------------------|------------------|-----------|------|------|------------------------|------|------|
| Supply voltage         | V <sub>DD</sub>  |           | -0.5 |      | +4                     | V    | 1    |
| Output supply voltage  | V <sub>DDQ</sub> |           | -0.5 |      | +4                     | V    | 1    |
| Input voltage          | V <sub>IN</sub>  |           | -0.5 |      | V <sub>DD</sub> + 0.3  | V    | 1    |
| Input / Output voltage | V <sub>I/O</sub> |           | -0.5 |      | V <sub>DDQ</sub> + 0.3 | V    | 1    |
| Operating temperature  | T <sub>J</sub>   |           | 20   |      | 110                    | °C   | 2    |
| Storage temperature    | T <sub>stg</sub> |           | -55  |      | +125                   | °C   |      |

**Notes** 1. -0.5 V MIN. (Pulse width 10% T<sub>cyc</sub>)

2. T<sub>J</sub> = Junction temperature

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended DC Operating Conditions (T<sub>J</sub> = 20 to 110 °C)**

| Parameter                    | Symbol           | Conditions | MIN.                  | TYP. | MAX.                  | Unit |
|------------------------------|------------------|------------|-----------------------|------|-----------------------|------|
| Core supply voltage          | V <sub>DD</sub>  |            | 3.15                  | 3.3  | 3.45                  | V    |
| Output buffer supply voltage | V <sub>DDQ</sub> |            | 1.4                   | 1.5  | 1.6                   | V    |
| Input reference voltage      | V <sub>REF</sub> |            | 0.6                   | 0.95 | 1.3                   | V    |
| Low level input voltage      | V <sub>IL</sub>  |            | -0.3 <sup>Note</sup>  |      | V <sub>REF</sub> -0.1 | V    |
| High level input voltage     | V <sub>IH</sub>  |            | V <sub>REF</sub> +0.1 |      | V <sub>DDQ</sub> +0.3 | V    |

**Note** -0.5 V MIN. (Pulse width 10% T<sub>cyc</sub>)

**Recommended AC Operating Conditions (T<sub>J</sub> = 20 to 110 °C) <sup>Note</sup>**

| Parameter                | Symbol                 | Conditions | MIN.                  | TYP. | MAX.                  | Unit |
|--------------------------|------------------------|------------|-----------------------|------|-----------------------|------|
| Input reference voltage  | V <sub>REF (RMS)</sub> |            | -5%                   |      | +5%                   | V    |
| Low level input voltage  | V <sub>IL</sub>        |            | -0.3                  |      | V <sub>REF</sub> -0.2 | V    |
| High level input voltage | V <sub>IH</sub>        |            | V <sub>REF</sub> +0.2 |      | V <sub>DDQ</sub> +0.3 | V    |

**Note** T<sub>J</sub> = 20 to 110 °C : μPD464318L-A6/ -A65, 464336L-A6/ -A65

T<sub>J</sub> = 20 to 100 °C : μPD464318L-A5, 464336L-A5

**Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

| Parameter <sup>Note</sup>           | Symbol           | Test conditions        | MAX. | Unit |
|-------------------------------------|------------------|------------------------|------|------|
| Input capacitance                   | C <sub>IN</sub>  | V <sub>IN</sub> = 0 V  | 5    | pF   |
| Input / Output capacitance          | C <sub>I/O</sub> | V <sub>I/O</sub> = 0 V | 7    | pF   |
| Clock pin (K, /K) input capacitance | C <sub>CLK</sub> | V <sub>CLK</sub> = 0 V | 7    | pF   |

**Note** These parameters are sampled and not 100% tested.



**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

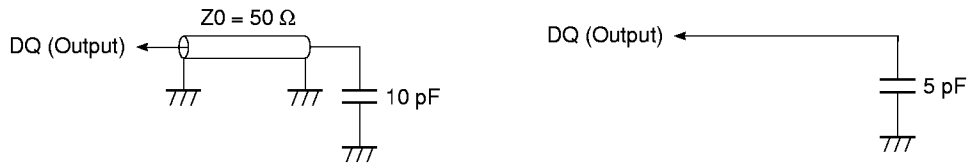
| Parameter                          | Symbol          | Conditions                                    | MIN.       | TYP. | MAX. | Unit |
|------------------------------------|-----------------|---|------------|------|------|------|
| Input leakage current              | I <sub>LI</sub> | V <sub>IN</sub> = 0 to V <sub>DD</sub>        | -5         |      | +5   | μA   |
| DQ leakage current <sup>Note</sup> | I <sub>LO</sub> | V <sub>I/O</sub> = 0 to V <sub>DDQ</sub>      | -5         |      | +5   | μA   |
| Operating supply current           | I <sub>CC</sub> | /SS = V <sub>IL</sub> , IDQ = 0 mA<br>200 MHz | μPD464318L |      | 600  | mA   |
|                                    |                 |   | μPD464336L |      | 700  |      |

**Note** /SS = V<sub>IH</sub> or /G = V<sub>IH</sub>

**Output Voltage on Controlled Impedance Push-Pull Output Buffer Mode (V<sub>ZQ</sub> = I<sub>ZQ</sub> × R<sub>Q</sub>)**

| Parameter                 | Symbol          | Conditions   | MIN.                  | TYP. | MAX.             | Unit |
|---------------------------|-----------------|--|-----------------------|------|------------------|------|
| Low level output voltage  | V <sub>OL</sub> | I <sub>OL</sub>   ≤ 10 μA, I <sub>OL</sub> = 2.5V <sub>DDQ</sub> / R <sub>Q</sub> ± 10%<br>V <sub>OL</sub> = V <sub>DDQ</sub> / 2 (175 Ω < R <sub>Q</sub> < 350 Ω) | V <sub>SS</sub>       |      | 0.1              | V    |
| High level output voltage | V <sub>OH</sub> | I <sub>OH</sub>   ≤ 10 μA, I <sub>OH</sub> = 2.5V <sub>DDQ</sub> / R <sub>Q</sub> ± 10%<br>V <sub>OH</sub> = V <sub>DDQ</sub> / 2 (175 Ω < R <sub>Q</sub> < 350 Ω) | V <sub>DDQ</sub> -0.1 |      | V <sub>DDQ</sub> | V    |

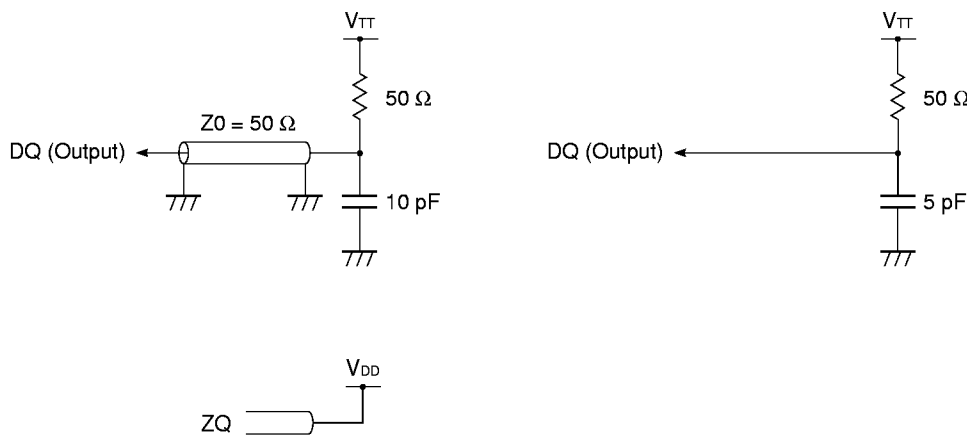
**Remark** See figure.



**Output Voltage on Push-Pull Output Buffer Mode (V<sub>ZQ</sub> = V<sub>DD</sub>)**

| Parameter                 | Symbol          | Conditions              | MIN.                  | TYP. | MAX. | Unit |
|---------------------------|-----------------|-------------------------|-----------------------|------|------|------|
| Low level output voltage  | V <sub>OL</sub> | I <sub>OL</sub> = +4 mA | -                     |      | 0.3  | V    |
| High level output voltage | V <sub>OH</sub> | I <sub>OH</sub> = -4 mA | V <sub>DDQ</sub> -0.3 |      | -    | V    |

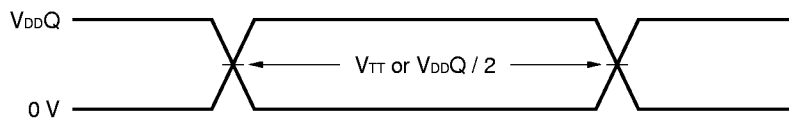
**Remark** See figure (V<sub>TT</sub> = 0.75 V).



**AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

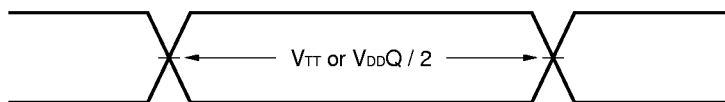
**AC Characteristics Test Conditions**

**Input waveform (rise and fall time = 0.5 ns (20 to 80%))**



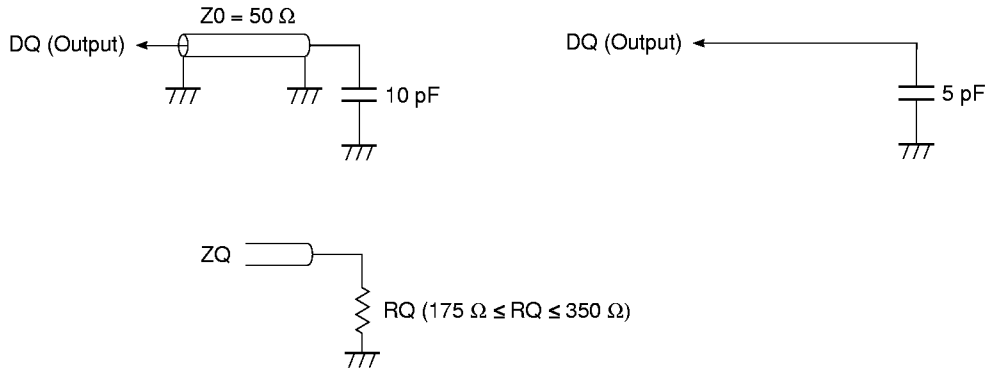
★ **Remark** Clock input differential voltage

**Output waveform**

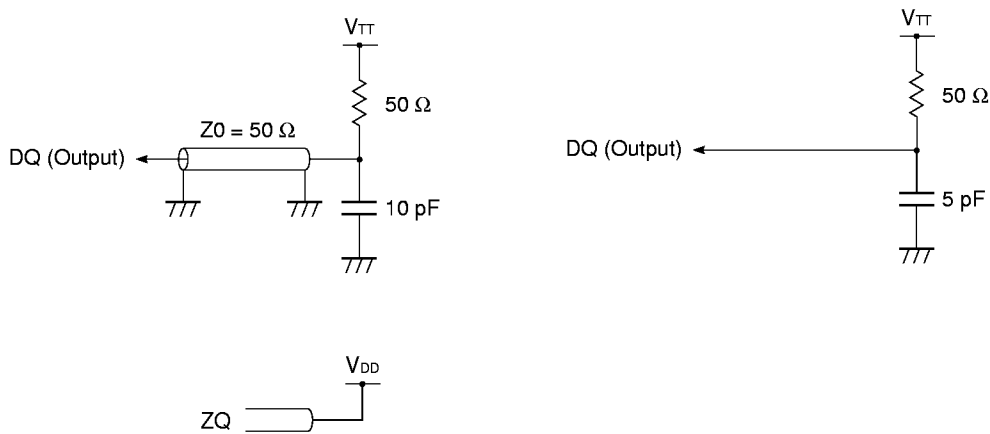


Output load

(1) Controlled impedance push-pull output buffer mode



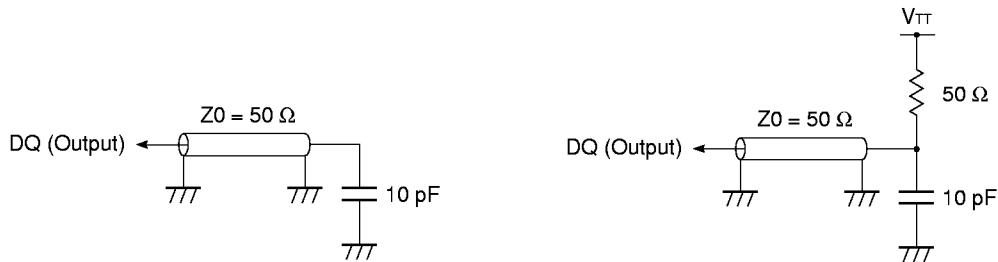
(2) Push-Pull output buffer mode ( $V_{TT}=0.75 \text{ V}$ )



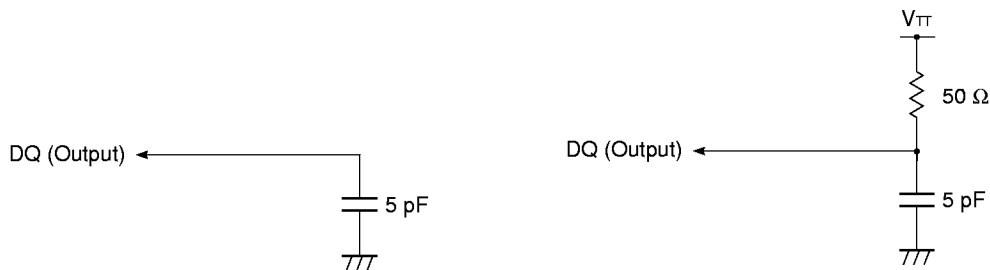
Single Differential Clock, Registered Input / Registered Output Mode

| Parameter              |              | Symbol        | -A5 (200 MHz) |      | -A6 (167 MHz) |      | -A65 (154 MHz) |      | Unit | Notes |
|------------------------|--------------|---------------|---------------|------|---------------|------|----------------|------|------|-------|
|                        |              |               | MIN.          | MAX. | MIN.          | MAX. | MIN.           | MAX. |      |       |
| Clock cycle time       |              | TKHKH         | 5.0           | –    | 6.0           | –    | 6.5            | –    | ns   |       |
| Clock phase time       |              | TKHKL / TKLKH | 2.4           | –    | 2.5           | –    | 3.0            | –    | ns   |       |
| Setup times            | Address      | TAVKH         | 0.5           | –    | 0.5           | –    | 0.5            | –    | ns   |       |
|                        | Write data   | TDVKH         |               |      |               |      |                |      |      |       |
|                        | Write enable | TWVKH         |               |      |               |      |                |      |      |       |
|                        | Chip select  | TSVKH         |               |      |               |      |                |      |      |       |
| Hold times             | Address      | TKHAX         | 1.0           | –    | 1.0           | –    | 1.0            | –    | ns   |       |
|                        | Write data   | TKHDX         |               |      |               |      |                |      |      |       |
|                        | Write enable | TKHWX         |               |      |               |      |                |      |      |       |
|                        | Chip select  | TKHSX         |               |      |               |      |                |      |      |       |
| Clock access time      |              | TKHQV         | –             | 2.6  | –             | 3.0  | –              | 3.5  | ns   | 1     |
| K high to Q change     |              | TKHQX         | 1.0           | –    | 1.0           | –    | 1.0            | –    | ns   | 2     |
| /G low to Q valid      |              | TGLQV         | –             | 2.5  | –             | 3.0  | –              | 3.5  | ns   | 1     |
| /G low to Q change     |              | TGLQX         | 1.0           | –    | 1.0           | –    | 1.0            | –    | ns   | 2     |
| /G high to Q Hi-Z      |              | TGHQZ         | 1.0           | 2.5  | 1.0           | 3.0  | 1.0            | 3.5  | ns   | 2     |
| K high to Q Hi-Z (/SW) |              | TKHQZ         | 1.0           | 3.5  | 1.0           | 3.5  | 1.0            | 4.0  | ns   | 2     |
| K high to Q Hi-Z (/SS) |              | TKHQZ2        | 1.0           | 3.5  | 1.0           | 3.5  | 1.0            | 4.0  | ns   | 2     |
| K high to Q Lo-Z       |              | TKHQX2        | 1.0           | –    | 1.0           | –    | 1.0            | –    | ns   |       |
| /G high Pulse width    |              | TGHGL         | 5.0           | –    | 6.0           | –    | 6.5            | –    | ns   | 3     |
| /G high to K high      |              | TGHKH         | 1.0           | –    | 1.0           | –    | 1.0            | –    | ns   | 3     |
| K high to /G low       |              | TKHGL         | 2.5           | –    | 2.5           | –    | 2.5            | –    | ns   | 3     |

Notes 1. See figure.

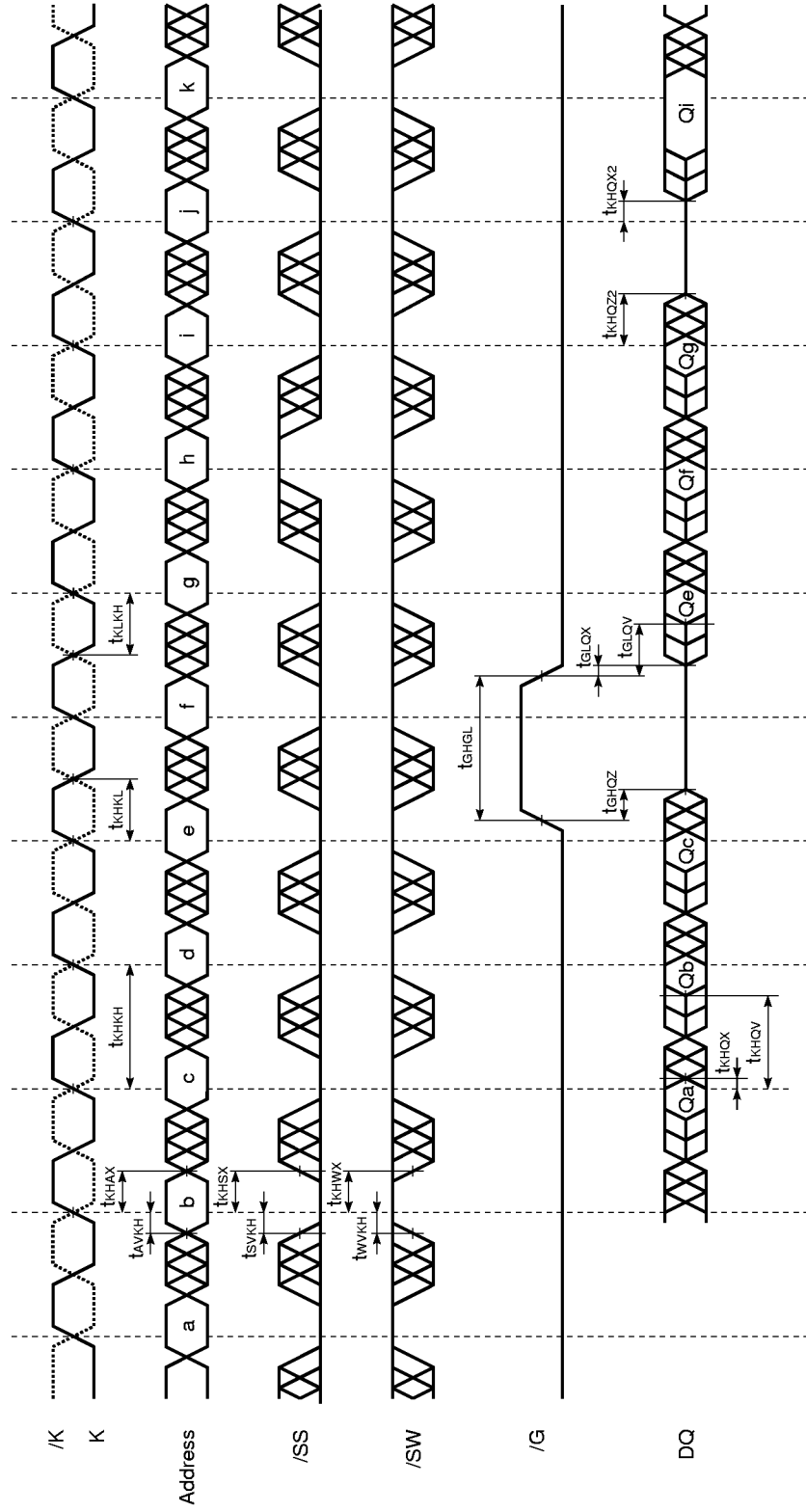


2. See figure.

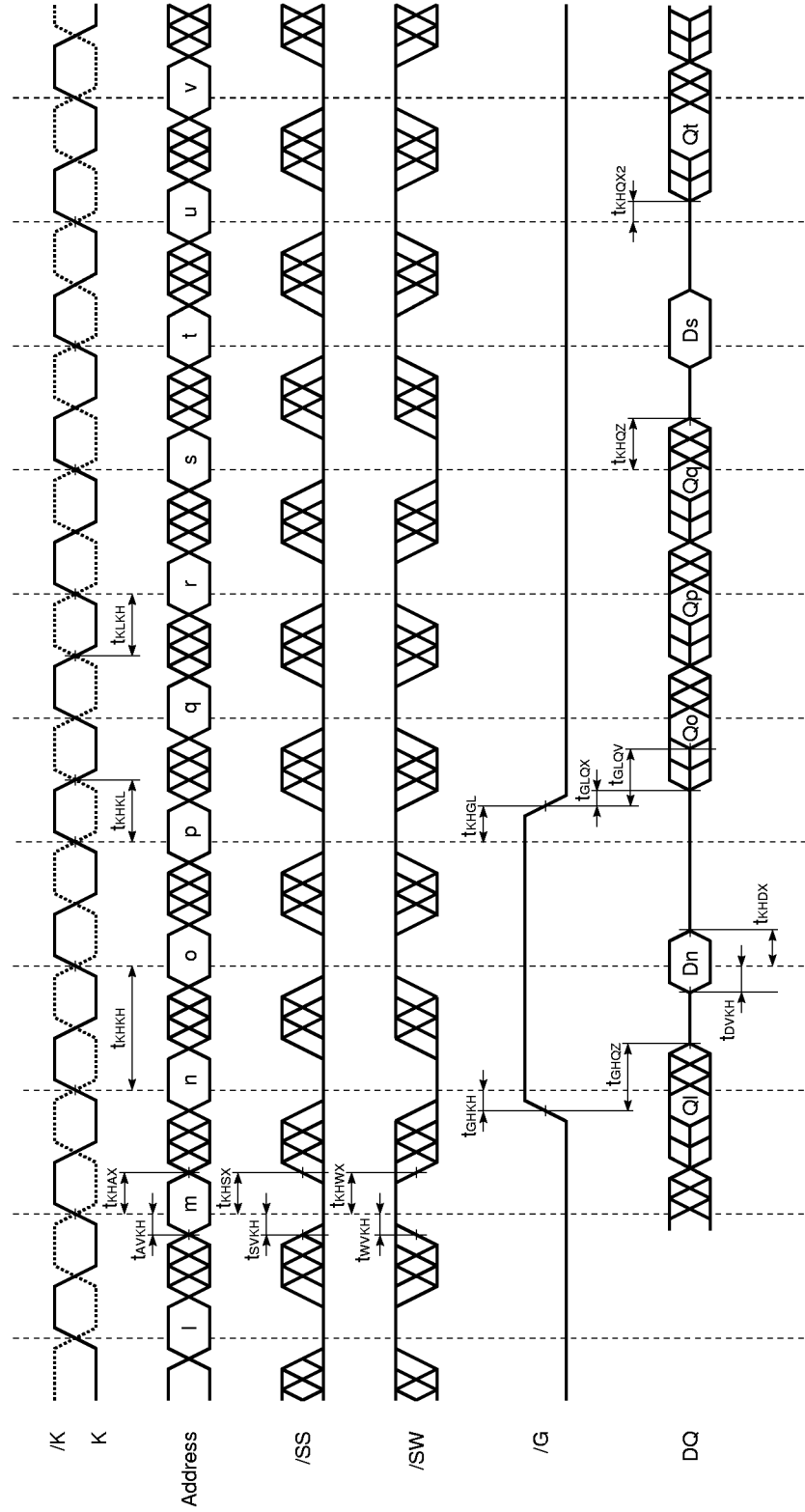


3. Controlled impedance push-pull output buffer mode only.

Single Differential Clock, Registered Input / Registered Output Mode (Read Operation)



Single Differential Clock, Registered Input / Registered Output Mode (Write Operation)



### JTAG Specifications

The μPD464318L and μPD464336L support a limited set of JTAG functions as in IEEE standard 1149.1.

#### Test Access Port (TAP) Pins

| Pin Name | Description      | Pin Assignments |
|----------|------------------|-----------------|
| TCK      | Test Clock Input | 4 U             |
| TMS      | Test Mode Select | 2 U             |
| TDI      | Test Data Input  | 3 U             |
| TDO      | Test Data Output | 5 U             |

**Remark** The device does not have TRST (TAP reset). The TAP controller state is reset into TEST-LOGIC-RESET on the SRAM POWER-UP.

#### JTAG DC Characteristics (T<sub>j</sub> = 20 to 110 °C)

| Parameter                | Symbol          | Conditions | MIN. | TYP. | MAX.                 | Unit | Notes |
|--------------------------|-----------------|------------|------|------|----------------------|------|-------|
| JTAG input high voltage  | V <sub>IH</sub> |            | 2.2  |      | V <sub>DD</sub> +0.3 | V    |       |
| JTAG input low voltage   | V <sub>IL</sub> |            | -0.3 |      | +0.8                 | V    |       |
| JTAG output high voltage | V <sub>OH</sub> |            | 2.4  |      | -                    | V    | 1     |
| JTAG output low voltage  | V <sub>OL</sub> |            | -    |      | 0.4                  | V    | 2     |

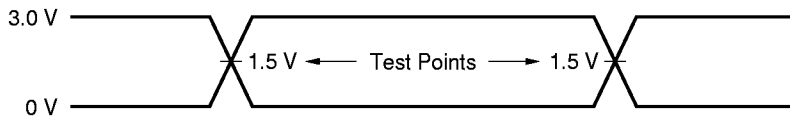
- Notes**
1. I<sub>OH</sub> = -8 mA
  2. I<sub>OL</sub> = 8 mA

#### JTAG AC Characteristics (T<sub>j</sub> = 20 to 110 °C)

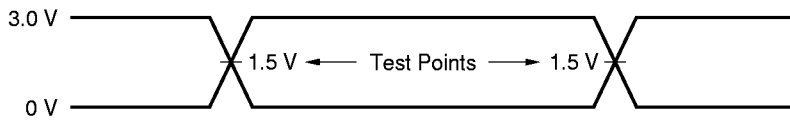
| Parameter                  | Symbol                                | Conditions | MIN. | TYP. | MAX. | Unit | Note |
|----------------------------|---------------------------------------|------------|------|------|------|------|------|
| Clock Cycle Time (TCK)     | t <sub>THH</sub>                      |            | 100  |      | -    | ns   |      |
| Clock Phase Time (TCK)     | t <sub>HTL</sub> / t <sub>LTH</sub>   |            | 40   |      | -    | ns   |      |
| Setup Time (TMS / TDI)     | t <sub>MVTH</sub> / t <sub>DVTH</sub> |            | 10   |      | -    | ns   |      |
| Hold Time (TMS / TDI)      | t <sub>HMX</sub> / t <sub>HDX</sub>   |            | 10   |      | -    | ns   |      |
| TCK Low to TDO Valid (TDO) | t <sub>TLQV</sub>                     |            | -    |      | 20   | ns   |      |

**JTAG AC Test Conditions ( $T_j = 20$  to  $110$  °C)**

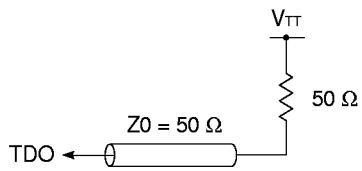
**Input waveform (rise / fall time = 1 ns (20 to 50 %))**



**Output waveform**

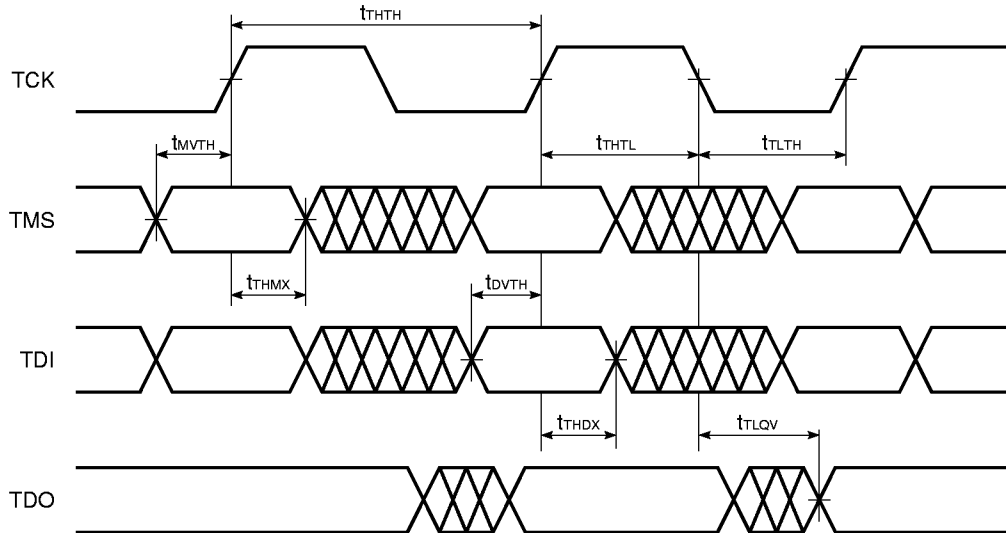


**Output load ( $V_{TT}=1.5$  V)**





JTAG Timing Diagram



Scan Register Definition

| Register name        | 256K x 18 | 128K x 36 | Unit |
|----------------------|-----------|-----------|------|
| Instruction register | 3         | 3         | bit  |
| Bypass register      | 1         | 1         | bit  |
| ID register          | 32        | 32        | bit  |
| Boundary register    | 51        | 70        | bit  |

ID Register Definition

| Organization | ID [31:28] vendor revision no. | ID [27:12] part no. | ID [11:1] vendor ID no. | ID [0] fix bit |
|--------------|--------------------------------|---------------------|-------------------------|----------------|
| 256K x 18    | XXXX                           | 0111001011 000000   | 00010010000             | 1              |
| 128K x 36    | XXXX                           | 0110101100 000000   | 00010010000             | 1              |

JTAG Instruction Cording

| IR2 | IR1 | IR0 | Instruction | Note |
|-----|-----|-----|-------------|------|
| 0   | 0   | 0   | EXTEST      | 1    |
| 0   | 0   | 1   | IDCODE      |      |
| 0   | 1   | 0   | SAMPLE-Z    | 1    |
| 0   | 1   | 1   | BYPASS      |      |
| 1   | 0   | 0   | SAMPLE      |      |
| 1   | 0   | 1   | BYPASS      |      |
| 1   | 1   | 0   | BYPASS      |      |
| 1   | 1   | 1   | BYPASS      |      |

Note 1. TRISTATE all data drivers and CAPTURE the pad values into a SERIAL SCAN LATCH.

SCAN Exit Order

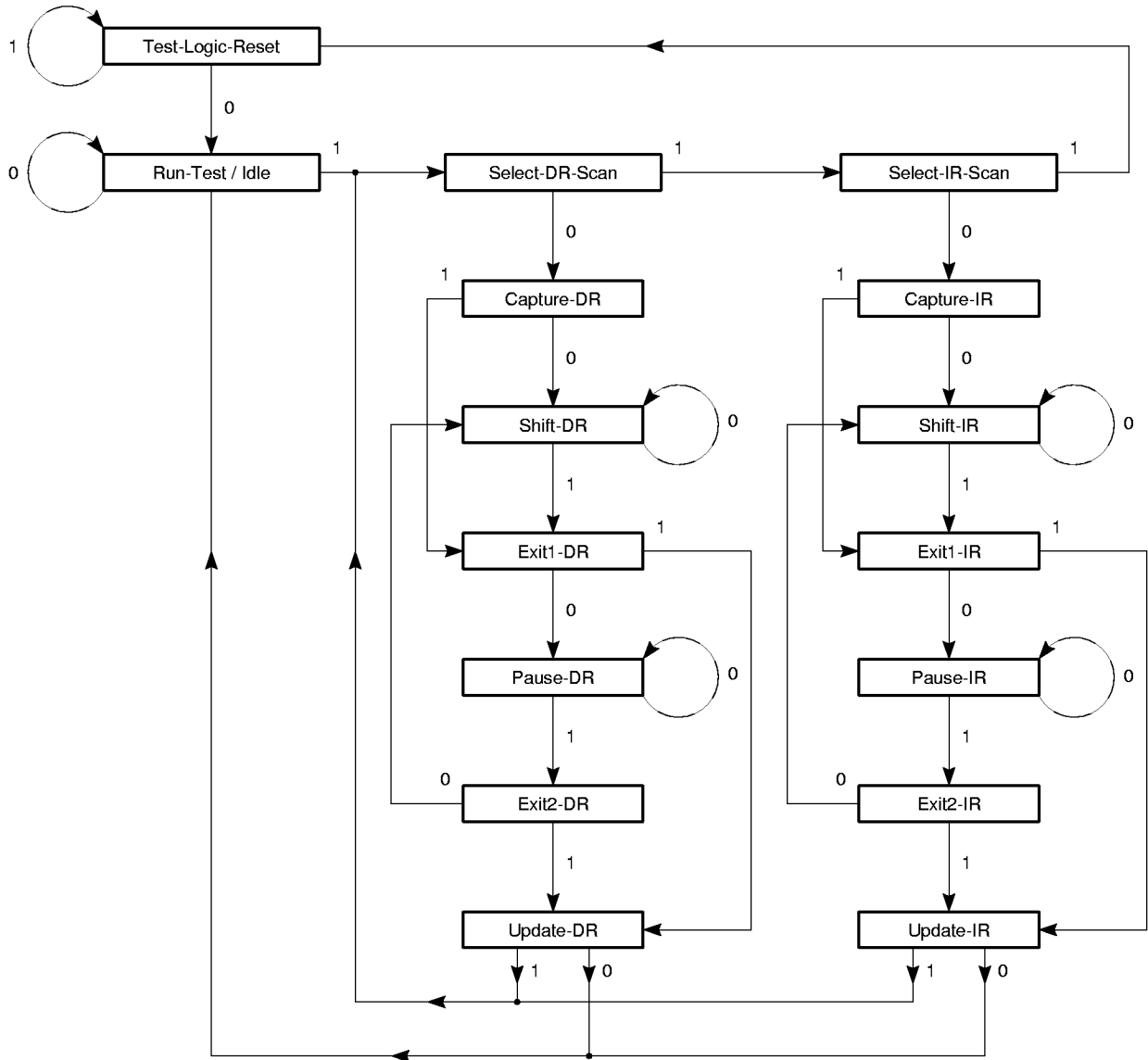
[ μPD464318L (256K words by 18 bits) ]

| Bit no. | Signal name | Bump ID | Bit no. | Signal name | Bump ID |
|---------|-------------|---------|---------|-------------|---------|
| 1       | M2          | 5R      | 26      | SA17        | 3B      |
| 2       | SA5         | 6T      | 27      | NC          | 2B      |
| 3       | SA0         | 4P      | 28      | SA9         | 3A      |
|         |             |         | 29      | SA10        | 3C      |
| 4       | SA4         | 6R      | 30      | SA13        | 2C      |
| 5       | SA8         | 5T      | 31      | SA12        | 2A      |
| 6       | NC          | 7T      |         |             |         |
|         |             |         | 32      | DQb1        | 1D      |
| 7       | DQa1        | 7P      | 33      | DQb2        | 2E      |
| 8       | DQa2        | 6N      |         |             |         |
|         |             |         |         |             |         |
|         |             |         | 34      | DQb3        | 2G      |
| 9       | DQa3        | 6L      |         |             |         |
|         |             |         |         |             |         |
|         |             |         | 35      | DQb4        | 1H      |
| 10      | DQa4        | 7K      | 36      | /SBb        | 3G      |
| 11      | /SBa        | 5L      | 37      | ZQ          | 4D      |
| 12      | /K          | 4L      | 38      | /SS         | 4E      |
| 13      | K           | 4K      | 39      | NC          | 4G      |
| 14      | /G          | 4F      | 40      | NC          | 4H      |
|         |             |         | 41      | /SW         | 4M      |
|         |             |         |         |             |         |
|         |             |         |         |             |         |
| 15      | DQa5        | 6H      |         |             |         |
| 16      | DQa6        | 7G      | 42      | DQb5        | 2K      |
|         |             |         | 43      | DQb6        | 1L      |
|         |             |         |         |             |         |
| 17      | DQa7        | 6F      |         |             |         |
| 18      | DQa8        | 7E      | 44      | DQb7        | 2M      |
|         |             |         | 45      | DQb8        | 1N      |
|         |             |         |         |             |         |
|         |             |         |         |             |         |
| 19      | DQa9        | 6D      |         |             |         |
| 20      | SA2         | 6A      | 46      | DQb9        | 2P      |
| 21      | SA3         | 6C      | 47      | SA11        | 3T      |
| 22      | SA7         | 5C      | 48      | SA14        | 2R      |
| 23      | SA6         | 5A      | 49      | SA1         | 4N      |
| 24      | NC          | 6B      | 50      | SA15        | 2T      |
| 25      | SA16        | 5B      | 51      | M1          | 3R      |

[ μPD464336L (128K words by 36 bits) ]

| Bit no. | Signal name | Bump ID | Bit no. | Signal name | Bump ID |
|---------|-------------|---------|---------|-------------|---------|
| 1       | M2          | 5R      | 36      | SA16        | 3B      |
|         |             |         | 37      | NC          | 2B      |
| 2       | SA0         | 4P      | 38      | SA9         | 3A      |
| 3       | SA8         | 4T      | 39      | SA10        | 3C      |
| 4       | SA4         | 6R      | 40      | SA13        | 2C      |
| 5       | SA7         | 5T      | 41      | SA12        | 2A      |
| 6       | NC          | 7T      | 42      | DQc9        | 2D      |
| 7       | DQa9        | 6P      | 43      | DQc8        | 1D      |
| 8       | DQa8        | 7P      | 44      | DQc7        | 2E      |
| 9       | DQa7        | 6N      | 45      | DQc6        | 1E      |
| 10      | DQa6        | 7N      | 46      | DQc5        | 2F      |
| 11      | DQa5        | 6M      | 47      | DQc4        | 2G      |
| 12      | DQa4        | 6L      | 48      | DQc3        | 1G      |
| 13      | DQa3        | 7L      | 49      | DQc2        | 2H      |
| 14      | DQa2        | 6K      | 50      | DQc1        | 1H      |
| 15      | DQa1        | 7K      | 51      | /SBc        | 3G      |
| 16      | /SBa        | 5L      | 52      | ZQ          | 4D      |
| 17      | /K          | 4L      | 53      | /SS         | 4E      |
| 18      | K           | 4K      | 54      | /C          | 4G      |
| 19      | /G          | 4F      | 55      | C           | 4H      |
| 20      | /SBb        | 5G      | 56      | /SW         | 4M      |
| 21      | DQb1        | 7H      | 57      | /SBd        | 3L      |
| 22      | DQb2        | 6H      | 58      | DQd1        | 1K      |
| 23      | DQb3        | 7G      | 59      | DQd2        | 2K      |
| 24      | DQb4        | 6G      | 60      | DQd3        | 1L      |
| 25      | DQb5        | 6F      | 61      | DQd4        | 2L      |
| 26      | DQb6        | 7E      | 62      | DQd5        | 2M      |
| 27      | DQb7        | 6E      | 63      | DQd6        | 1N      |
| 28      | DQb8        | 7D      | 64      | DQd7        | 2N      |
| 29      | DQb9        | 6D      | 65      | DQd8        | 1P      |
|         |             |         | 66      | DQd9        | 2P      |
| 30      | SA2         | 6A      | 67      | SA11        | 3T      |
| 31      | SA3         | 6C      | 68      | SA14        | 2R      |
| 32      | SA6         | 5C      | 69      | SA1         | 4N      |
| 33      | SA5         | 5A      |         |             |         |
| 34      | NC          | 6B      |         |             |         |
| 35      | SA15        | 5B      | 70      | M1          | 3R      |

TAP Controller State Diagram



**Disabling The Test Access Port**

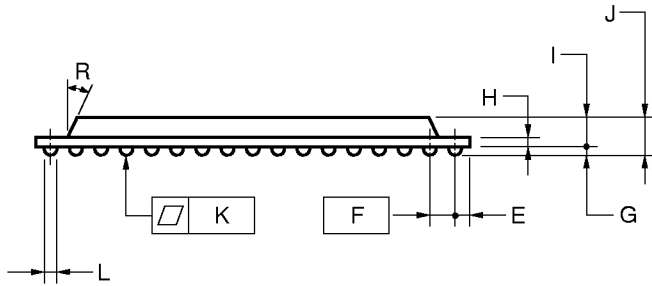
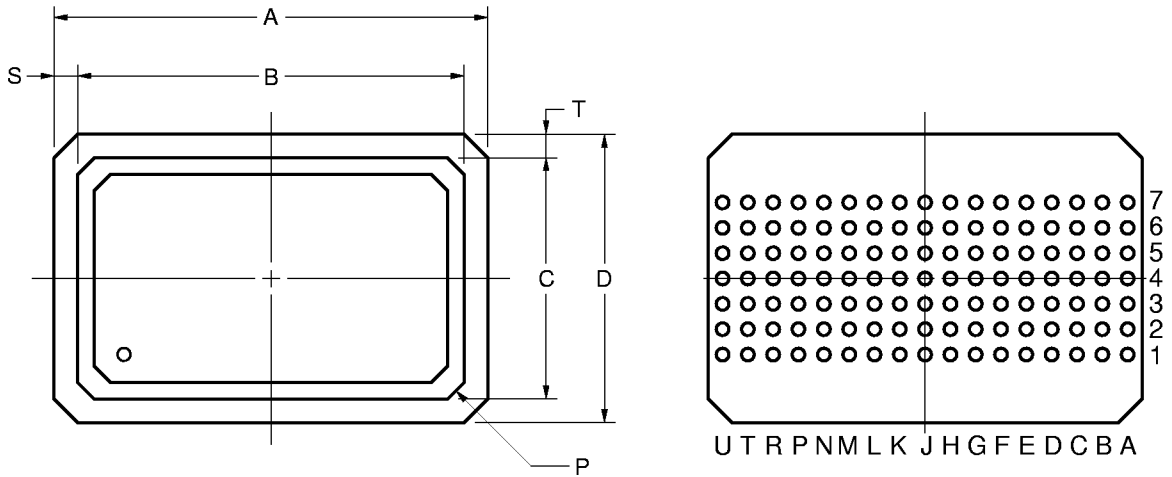
It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to Vss to preclude mid level inputs.

TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a 1 k resistor.

TDO should be left unconnected.

Package Drawing

119 PIN PLASTIC BGA



| ITEM | MILLIMETERS | INCHES                                     |
|------|-------------|--|
| A    | 22.0±0.2    | 0.866±0.008                                |
| B    | 19.5        | 0.768                                      |
| C    | 12.0        | 0.472                                      |
| D    | 14.0±0.2    | 0.551±0.008                                |
| E    | 0.84        | 0.033                                      |
| F    | 1.27 (T.P.) | 0.05 (T.P.)                                |
| G    | 0.6±0.1     | 0.024 <sup>+0.004</sup> <sub>-0.005</sub>  |
| H    | 0.56        | 0.022                                      |
| I    | 1.46±0.1    | 0.057 <sup>+0.005</sup> <sub>-0.004</sub>  |
| J    | 2.30 MAX.   | 0.091                                      |
| K    | 0.15        | 0.006                                      |
| L    | φ0.78±0.1   | φ0.031 <sup>+0.004</sup> <sub>-0.005</sub> |
| P    | C0.7        | C0.028                                     |
| R    | 25°         | 25°  |
| S    | 1.25        | 0.049                                      |
| T    | 1.0         | 0.039                                      |

P119S1-R4

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD464318L and  $\mu$ PD464336L.

**Type of Surface Mount Device**

$\mu$ PD464318LS1: 119-pin plastic BGA

$\mu$ PD464336LS1: 119-pin plastic BGA

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.