K7P403611M
K7P401811M
# 128Kx36 & 256Kx18 SRAM

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## Document Title

**128Kx36 & 256Kx18 Synchronous Pipelined SRAM**

## Revision History

| Rev. No. | History | Draft Date | Remark |
|---|---|---|---|
| Rev. 0.0 | - Preliminary specification release | | Preliminary |
| Rev. 0.1 | - Change specification format.<br>  No change was made in parameters. | April, 1997 | Preliminary |
| Rev. 0.2 | - Added 4.4ns part(Part Number, $I_{DD}$, AC Characteristics).<br> Updated $I_{DD}$, $I_{SB}$ and Input High Level.<br> Updated $t_{KHKL}$, $t_{KLKH}$, $t_{KHQX}$, $t_{KHQX1}$ and AC Test Conditions.<br> For JTAG, updated Vendor Definition and added $t_{SVCH}/t_{CHSX}$. | Dec. 1997 | Preliminary |
| Rev. 1.0 | - Deleted 4.4ns part(Part Number,Idd,AC Characteristics)<br>- Final specification release | Dec.  1998 | Final |

## 128Kx36 & 256Kx18 Synchronous Pipelined SRAM

### FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core/1.5V Output Power Supply.
- HSTL Input and Output Levels.
- Differential, HSTL Clock Inputs K, $\overline{K}$.
- Synchronous Read and Write Operation
- Registered Input and Registered Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- Programmable Impedance Output Drivers.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17)Pin Ball Grid Array Package(14mmx22mm).

| Organization | Part Number | Cycle Time | Access Time |
|---|---|---|---|
| 128Kx36 | K7P403611M-H20 | 5 | 2.5 |
|  | K7P403611M-H16 | 6 | 3.0 |
| 256Kx18 | K7P401811M-H20 | 5 | 2.5 |
|  | K7P401811M-H16 | 6 | 3.0 |

### FUNCTIONAL BLOCK DIAGRAM
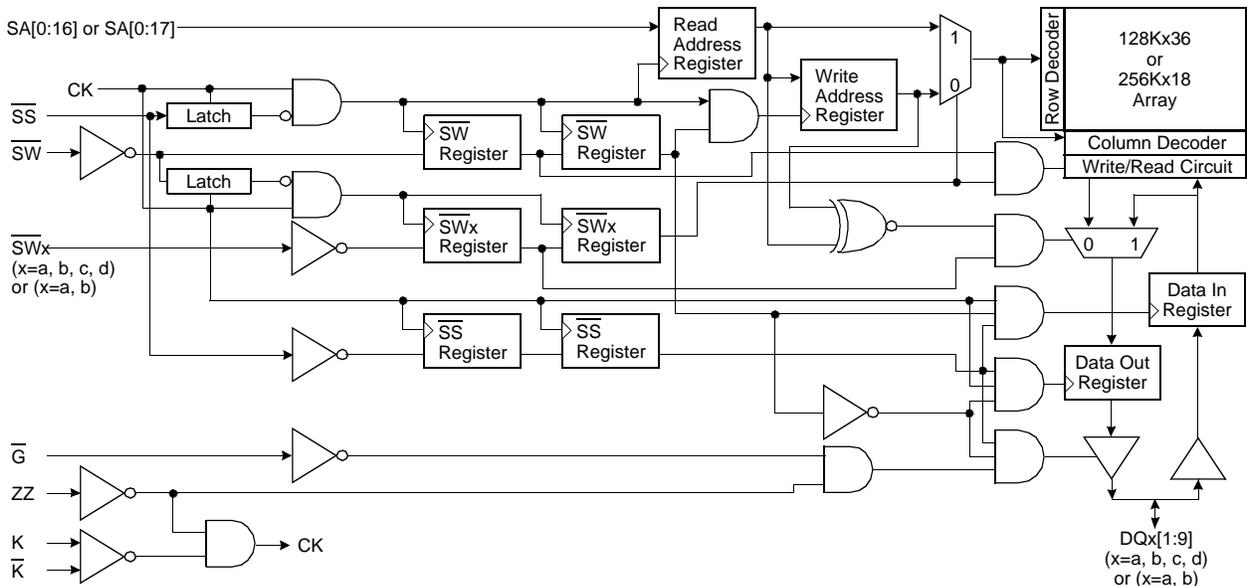


### PIN DESCRIPTION

| Pin Name | Pin Description | Pin Name | Pin Description |
|---|---|---|---|
| K, $\overline{K}$ | Differential Clocks | $V_{REF}$ | HSTL Input Reference Voltage |
| SAn | Synchronous Address Input | $M_1$, $M_2$ | Read Protocol Mode Pins ( $M_1=V_{SS}$, $M_2=V_{DD}$ ) |
| DQn | Bi-directional Data Bus | $\overline{G}$ | Asynchronous Output Enable |
| $\overline{SW}$ | Synchronous Global Write Enable | $\overline{SS}$ | Synchronous Select |
| $\overline{SWa}$ | Synchronous Byte a Write Enable | TCK | JTAG Test Clock |
| $\overline{SWb}$ | Synchronous Byte b Write Enable | TMS | JTAG Test Mode Select |
| $\overline{SWc}$ | Synchronous Byte c Write Enable | TDI | JTAG Test Data Input |
| $\overline{SWd}$ | Synchronous Byte d Write Enable | TDO | JTAG Test Data Output |
| ZZ | Asynchronous Power Down | ZQ | Output Driver Impedance Control |
| $V_{DD}$ | Core Power Supply | $V_{SS}$ | GND |
| $V_{DDQ}$ | Output Power Supply | NC | No Connection |

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## PACKAGE PIN CONFIGURATIONS(TOP VIEW)

### K7P403611M(128Kx36)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | $SA_{13}$ | $SA_{10}$ | NC | $SA_7$ | $SA_4$ | $V_{DDQ}$ |
| B | NC | NC | $SA_9$ | NC | $SA_8$ | NC | NC |
| C | NC | $SA_{12}$ | $SA_{11}$ | $V_{DD}$ | $SA_6$ | $SA_5$ | NC |
| D | $DQc_8$ | $DQc_9$ | $V_{SS}$ | ZQ | $V_{SS}$ | $DQb_9$ | $DQb_8$ |
| E | $DQc_6$ | $DQc_7$ | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | $DQb_7$ | $DQb_6$ |
| F | $V_{DDQ}$ | $DQc_5$ | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | $DQb_5$ | $V_{DDQ}$ |
| G | $DQc_3$ | $DQc_4$ | $\overline{SWc}$ | NC | $\overline{SWb}$ | $DQb_4$ | $DQb_3$ |
| H | $DQc_1$ | $DQc_2$ | $V_{SS}$ | NC | $V_{SS}$ | $DQb_2$ | $DQb_1$ |
| J | $V_{DDQ}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{DDQ}$ |
| K | $DQd_1$ | $DQd_2$ | $V_{SS}$ | K | $V_{SS}$ | $DQa_2$ | $DQa_1$ |
| L | $DQd_3$ | $DQd_4$ | $\overline{SWd}$ | $\overline{K}$ | $\overline{SWa}$ | $DQa_4$ | $DQa_3$ |
| M | $V_{DDQ}$ | $DQd_5$ | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | $DQa_5$ | $V_{DDQ}$ |
| N | $DQd_6$ | $DQd_7$ | $V_{SS}$ | $SA_{16}$ | $V_{SS}$ | $DQa_7$ | $DQa_6$ |
| P | $DQd_8$ | $DQd_9$ | $V_{SS}$ | $SA_0$ | $V_{SS}$ | $DQa_9$ | $DQa_8$ |
| R | NC | $SA_{15}$ | $M_1$ | $V_{DD}$ | $M_2$ | $SA_2$ | NC |
| T | NC | NC | $SA_{14}$ | $SA_1$ | $SA_3$ | NC | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

### K7P401811M(256Kx18)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | $SA_{13}$ | $SA_{10}$ | NC | $SA_7$ | $SA_4$ | $V_{DDQ}$ |
| B | NC | NC | $SA_9$ | NC | $SA_8$ | NC | NC |
| C | NC | $SA_{12}$ | $SA_{11}$ | $V_{DD}$ | $SA_6$ | $SA_5$ | NC |
| D | $DQb_1$ | NC | $V_{SS}$ | ZQ | $V_{SS}$ | $DQa_9$ | NC |
| E | NC | $DQb_2$ | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | NC | $DQa_8$ |
| F | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | $DQa_7$ | $V_{DDQ}$ |
| G | NC | $DQb_3$ | $\overline{SWb}$ | NC | NC | NC | $DQa_6$ |
| H | $DQb_4$ | NC | $V_{SS}$ | NC | $V_{SS}$ | $DQa_5$ | NC |
| J | $V_{DDQ}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{DDQ}$ |
| K | NC | $DQb_5$ | $V_{SS}$ | K | $V_{SS}$ | NC | $DQa_4$ |
| L | $DQb_6$ | NC | NC | $\overline{K}$ | $\overline{SWa}$ | $DQa_3$ | NC |
| M | $V_{DDQ}$ | $DQb_7$ | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| N | $DQb_8$ | NC | $V_{SS}$ | $SA_{16}$ | $V_{SS}$ | $DQa_2$ | NC |
| P | NC | $DQb_9$ | $V_{SS}$ | $SA_1$ | $V_{SS}$ | NC | $DQa_1$ |
| R | NC | $SA_{15}$ | $M_1$ | $V_{DD}$ | $M_2$ | $SA_2$ | NC |
| T | NC | $SA_{17}$ | $SA_{14}$ | NC | $SA_3$ | $SA_0$ | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

# K7P403611M
# K7P401811M
<div align="right">

## 128Kx36 & 256Kx18 SRAM
</div>

## FUNCTION DESCRIPTION

The K7P403611M and K7P401811M are 4,718,592 bit Synchronous Pipeline Mode SRAM. It is organized as 131,072words of 36 bits(or 262, 144 words of 18 bits)and is implemented in SAMSUNG's advanced CMOS technology.

Single differential HSTL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, All addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers edge of the next rising edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

## Read Operation

During reads, the address is registered during the frist clock edge, the internal array is read between this first edge and the second edge, and data is captured in the output register and driven to the CPU during the second clock edge. $\overline{SS}$ is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

## Write(Store) Operation

All addresses and $\overline{SW}$ are sampled on the clock rising edge. $\overline{SW}$ is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and $\overline{SW}$ have been sampled by the SRAM. $\overline{SS}$ will be driven low during the same cycle that the Address, $\overline{SW}$ and $\overline{SW}$[a:d] are valid to signal that a valid operation is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}$[a:d] signal which 9-bit bytes will be writen. Timing of $\overline{SW}$[a:d] is the same as the $\overline{SW}$ signal.

## Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

## Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time($t_{ZZR}$) is required before the SRAM resumes to normal operation.

## TRUTH TABLE

| K | ZZ | $\overline{G}$ | $\overline{SS}$ | $\overline{SW}$ | $\overline{SWa}$ | $\overline{SWb}$ | $\overline{SWc}$ | $\overline{SWd}$ | DQa | DQb | DQc | DQd | Operation |
|---|----|----|----|----|----|----|----|----|------|------|------|------|-----------|
| X | H | X | X | X | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Power Down Mode. No Operation |
| X | L | H | X | X | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Output Disabled. |
| ↑ | L | L | H | X | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Output Disabled. No Operation |
| ↑ | L | L | L | H | X | X | X | X | D$_{OUT}$ | D$_{OUT}$ | D$_{OUT}$ | D$_{OUT}$ | Read Cycle |
| ↑ | L | X | L | L | H | H | H | H | Hi-Z | Hi-Z | Hi-Z | Hi-Z | No Bytes Written |
| ↑ | L | X | L | L | L | H | H | H | D$_{IN}$ | Hi-Z | Hi-Z | Hi-Z | Write first byte |
| ↑ | L | X | L | L | H | L | H | H | Hi-Z | D$_{IN}$ | Hi-Z | Hi-Z | Write second byte |
| ↑ | L | X | L | L | H | H | L | H | Hi-Z | Hi-Z | D$_{IN}$ | Hi-Z | Write third byte |
| ↑ | L | X | L | L | H | H | H | L | Hi-Z | Hi-Z | Hi-Z | D$_{IN}$ | Write fourth byte |
| ↑ | L | X | L | L | L | L | L | L | D$_{IN}$ | D$_{IN}$ | D$_{IN}$ | D$_{IN}$ | Write all byte |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Core Supply Voltage Relative to $V_{SS}$ | $V_{DD}$ | -0.5 to 3.9 | V | |
| Output Supply Voltage Relative to $V_{SS}$ | $V_{DDQ}$ | $V_{DD}$ | V | |
| Voltage on any I/O pin Relative to $V_{SS}$ | $V_{TERM}$ | -0.5 to $V_{DD}$+0.5 | V | |
| Maximum Power Dissipation | $P_D$ | 3 | W | |
| Output Short-Circuit Current | $I_{OUT}$ | 25 | mA | |
| Operating Temperature | $T_{OPR}$ | 0 to 70 | °C | |
| Storage Temperature | $T_{STG}$ | -55 to 125 | °C | |

**NOTE** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Core Power Supply Voltage | $V_{DD}$ | 3.15 | 3.3 | 3.45 | V | |
| Output Power Supply Voltage | $V_{DDQ}$ | 1.4 | 1.5 | 1.6 | V | |
| Input High Level | $V_{IH}$ | $V_{REF}$+0.1 | - | $V_{DD}$+0.3 | V | |
| Input Low Level | $V_{IL}$ | -0.3 | - | $V_{REF}$ - 0.1 | V | |
| Input Reference Voltage | $V_{REF}$ | $V_{DDQ}$/2 | - | $2V_{DDQ}$/3 | V | |
| Clock Input Signal Voltage | $V_{IN}$-CLK | -0.3 | - | $V_{DDQ}$+0.3 | V | |
| Clock Input Differential Voltage | $V_{DIF}$-CLK | 0.1 | - | $V_{DDQ}$+0.6 | V | |
| Clock Input Common Mode Voltage | $V_{CM}$-CLK | $V_{DDQ}$/2 | - | $2V_{DDQ}$/3 | V | |
| Operating Junction Temperature | $T_J$ | 10 | - | 110 | °C | |

## DC CHARACTERISTICS

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Average Power Supply Operating Current-x36 ($V_{IN}=V_{IH}$ or $V_{IL}$, ZZ & $\overline{SS}=V_{IL}$) | $I_{DD5}$ $I_{DD6}$ | - | 650 600 | mA | 1, 2 |
| Average Power Supply Operating Current-x18 ($V_{IN}=V_{IH}$ or $V_{IL}$, ZZ & $\overline{SS}=V_{IL}$) | $I_{DD5}$ $I_{DD6}$ | - | 600 550 | mA | 1, 2 |
| Power Supply Standby Current ($V_{IN}=V_{IH}$ or $V_{IL}$, ZZ=$V_{IH}$) | $I_{SB}$ | - | 60 | mA | 1 |
| Input Leakage Current ($V_{IN}=V_{SS}$ or $V_{DD}$) | $I_{LI}$ | -1 | 1 | µA | |
| Output Leakage Current ($V_{OUT}=V_{SS}$ or $V_{DDQ}$, ZZ=$V_{IH}$, $\overline{G}=V_{IH}$) | $I_{LO}$ | -1 | 1 | µA | |
| Output High Voltage($I_{OH}$=-2mA) | $V_{OH}$ | $V_{DDQ}$/2+0.3 | $V_{DDQ}$ | V | |
| Output Low Voltage($I_{OL}$=2mA) | $V_{OL}$ | $V_{SS}$ | $V_{DDQ}$/2-0.3 | V | |

**NOTE** : 1. Minimum cycle. $I_{OUT}$=0mA.
       2. 50% read cycles.

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## PIN CAPACITANCE

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | 4 | 5 | pF |
| Output Capacitance | $C_{OUT}$ | 7 | 8 | pF |

**NOTE** : Periodically sampled and not 100% tested.(dV=0V, f=1MHz)

## AC TEST CONDITIONS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Core Power Supply Voltage | $V_{DD}$ | 3.15~3.45 | V |
| Output Power Supply Voltage | $V_{DDQ}$ | 1.4~1.6 | V |
| Input High/Low Level | $V_{IH}/V_{IL}$ | 1.25/0.25 | V |
| Input Reference Level | $V_{REF}$ | 0.75 | V |
| Input Rise/Fall Time | $T_R/T_F$ | 1.0/1.0 | ns |
| Input and Out Timing Reference Level | | 0.75 | V |
| Clock Input Timing Reference Level | | Cross Point | V |

**NOTE** : Parameters are tested with RQ=250Ω and $V_{DDQ}$=1.5V.

## AC TEST OUTPUT LOAD

Dout — Z0=50Ω

20pF*    50Ω

0.75V

*Capacitive load consists of all components of the tester environment
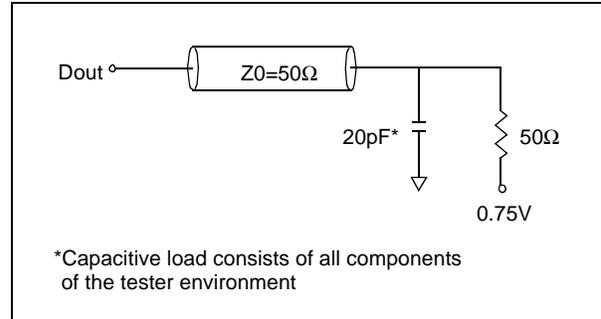
## AC CHARACTERISTICS

| Parameter | Symbol | -20 Min | -20 Max | -16 Min | -16 Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Clock Cycle Time | $t_{KHKH}$ | 5.0 | - | 6.0 | - | ns | |
| Clock High Pulse Width | $t_{KHKL}$ | 1.5 | - | 1.5 | - | ns | |
| Clock Low Pulse Width | $t_{KLKH}$ | 1.5 | - | 1.5 | - | ns | |
| Clock High to Output Valid | $t_{KHQV}$ | - | 2.5 | - | 3.0 | ns | |
| Clock High to Output Hold | $t_{KHQX}$ | 0.5 | - | 0.5 | - | ns | |
| Address Setup Time | $t_{AVKH}$ | 0.5 | - | 0.5 | - | ns | |
| Address Hold Time | $t_{KHAX}$ | 1.0 | - | 1.0 | - | ns | |
| Write Data Setup Time | $t_{DVKH}$ | 0.5 | - | 0.5 | - | ns | |
| Write Data Hold Time | $t_{KHDX}$ | 1.0 | - | 1.0 | - | ns | |
| $\overline{SW}$, $\overline{SW}$[a:d] Setup Time | $t_{WVKH}$ | 0.5 | - | 0.5 | - | ns | |
| $\overline{SW}$, $\overline{SW}$[a:d] Hold Time | $t_{KHWX}$ | 1.0 | - | 1.0 | - | ns | |
| $\overline{SS}$ Setup Time | $t_{SVKH}$ | 0.5 | - | 0.5 | - | ns | |
| $\overline{SS}$ Hold Time | $t_{KHSX}$ | 1.0 | - | 1.0 | - | ns | |
| Clock High to Output Hi-Z | $t_{KHQZ}$ | - | 2.5 | - | 3.0 | ns | |
| Clock High to Output Low-Z | $t_{KHQX1}$ | 0.5 | - | 0.5 | - | ns | |
| $\overline{G}$ High to Output High-Z | $t_{GHQZ}$ | - | 2.5 | - | 3.0 | ns | |
| $\overline{G}$ Low to Output Low-Z | $t_{GLQX}$ | 0.5 | - | 0.5 | - | ns | |
| $\overline{G}$ Low to Output Valid | $t_{GLQV}$ | - | 2.5 | - | 3.0 | ns | |
| ZZ High to Power Down(Sleep Time) | $t_{ZZE}$ | - | 5.0 | - | 6.0 | ns | |
| ZZ Low to Recovery(Wake-up Time) | $t_{ZZR}$ | - | 5.0 | - | 6.0 | ns | |

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# K7P403611M
# K7P401811M

128Kx36 & 256Kx18 SRAM

## TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES ($\overline{SS}$ Controlled, $\overline{G}$=Low)
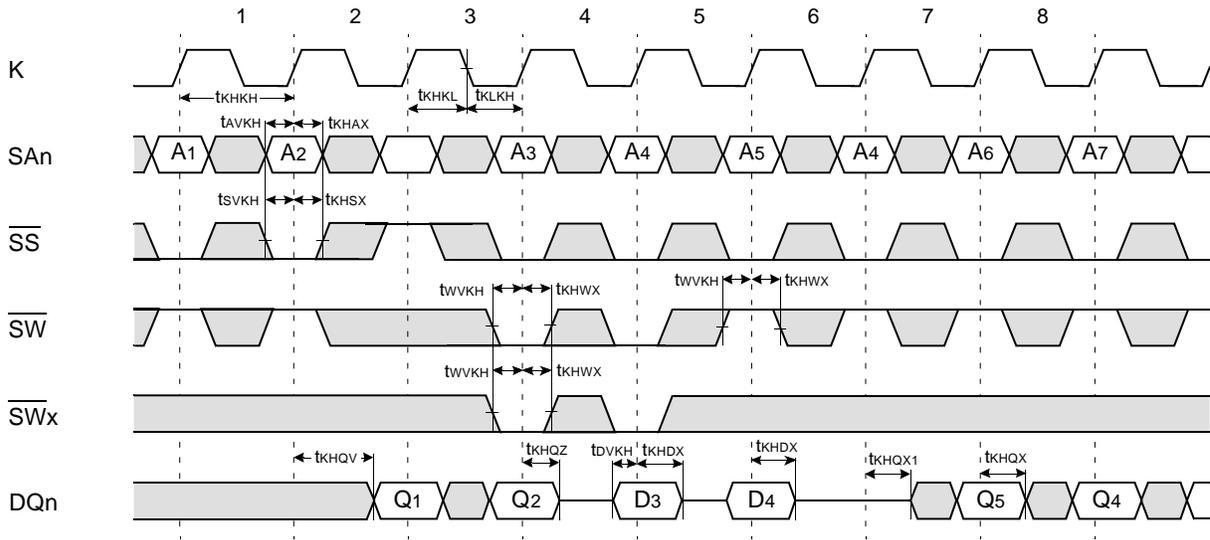


**NOTE**

1. $D_3$ is the input data written in memory location $A_3$.
2. $Q_4$ is the output data read from the write data buffer(not from the cell array), as a result of address $A_4$ being a match from the last write cycle address.

## TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES ($\overline{G}$ Controlled, $\overline{SS}$=Low)



**NOTE**

1. $D_3$ is the input data written in memory location $A_3$.
2. $Q_4$ is the output data read from the write data buffer(not from the cell array), as a result of address $A_4$ being a match from the last write cycle address.

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## TIMING WAVEFORMS OF STANDBY CYCLES
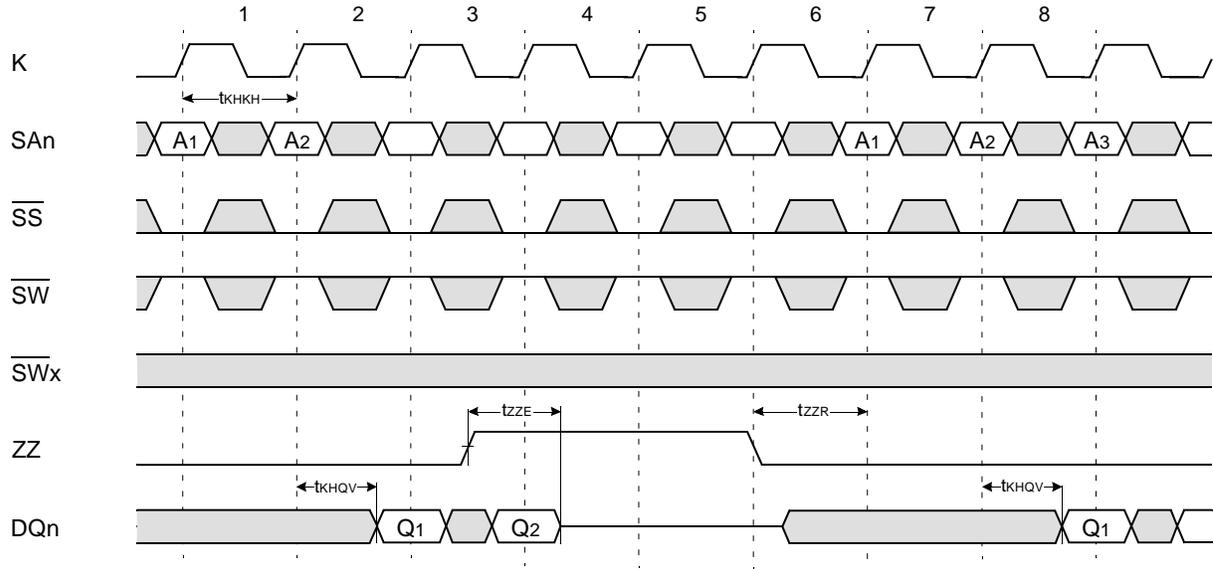
## PROGRAMMABLE IMPEDANCE OUTPUT BUFFER OPERATION

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to $V_{SS}$ through a precision resistor(RQ). The value of RQ is five times the output impedance desired. For example, 250Ω resistor will give an output impedance of 50Ω. The allowable range of RQ to guarantee impedance matching with a tolerance of 10% is between 175Ω and 350Ω. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with $\overline{G}$ high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Periodic readjustment is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. Impedance updates occur no more often than every 32clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33continuous read cycles have occurred, an impedance update will occur the next time $\overline{SS}$ or $\overline{G}$ are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

## DC Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Impedance Control Resistor Range | RQ | 175 | 250 | 350 | Ω | - |
| Driver Impedance | $Z_D$ | RQ/5-10% | - | RQ/5+10% | Ω | 1 |

**NOTE** : 1. Measured at $V_{OUT}=V_{DDQ}/2$. $I_{OUT}=(V_{DDQ}/2)/(RQ/5) \pm 10\%$ @ $V_{OUT}=V_{DDQ}/2$.

## AC Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Output Impedance Update $\overline{G}$ Setup Time | $t_{GHKH}$ | 0.5 | - | - | ns | - |
| Output Impedance Update $\overline{G}$ Hold Time | $t_{KHGX}$ | 1.0 | - | - | ns | - |

## TIMING WAVEFORMS OF Driver Impedance Update Control
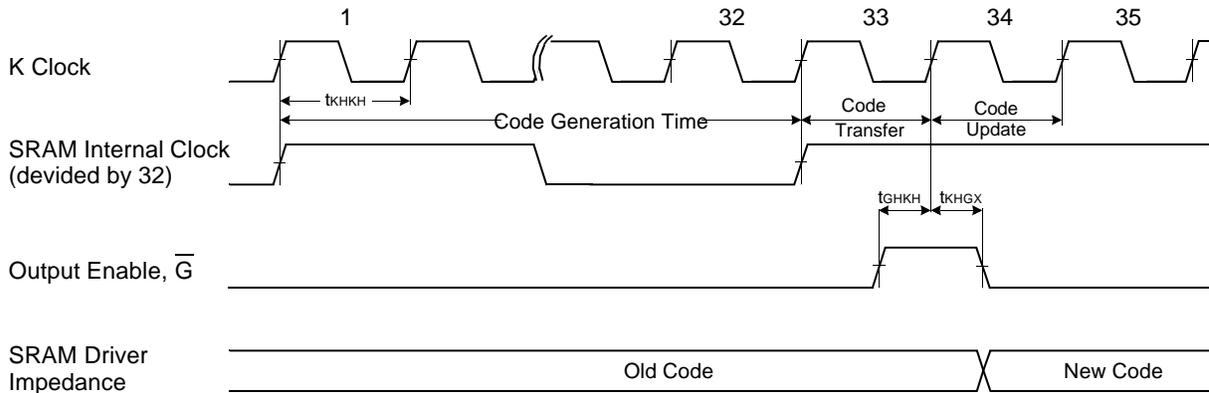
## IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to $V_{SS}$ to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to $V_{DD}$ through a resistor. TDO should be left unconnected.

## JTAG Block Diagram
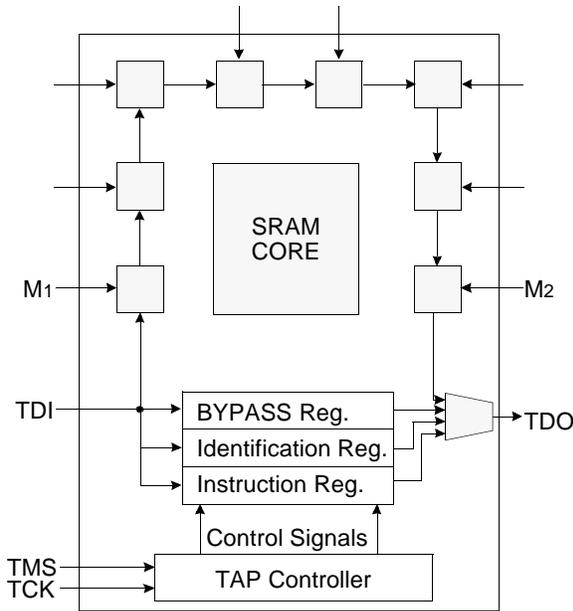


## JTAG Instruction Coding

| IR2 | IR1 | IR0 | Instruction | TDO Output | Notes |
|-----|-----|-----|-------------|------------|-------|
| 0 | 0 | 0 | SAMPLE-Z | Boundary Scan Register | 1 |
| 0 | 0 | 1 | IDCODE | Identification Register | 2 |
| 0 | 1 | 0 | SAMPLE-Z | Boundary Scan Register | 1 |
| 0 | 1 | 1 | BYPASS | Bypass Register | 3 |
| 1 | 0 | 0 | SAMPLE | Boundary Scan Register | 4 |
| 1 | 0 | 1 | BYPASS | Bypass Register | 3 |
| 1 | 1 | 0 | BYPASS | Bypass Register | 3 |
| 1 | 1 | 1 | BYPASS | Bypass Register | 3 |

**NOTE** :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to $V_{SS}$ when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

## TAP Controller State Diagram

# K7P403611M
# K7P401811M
## 128Kx36 & 256Kx18 SRAM
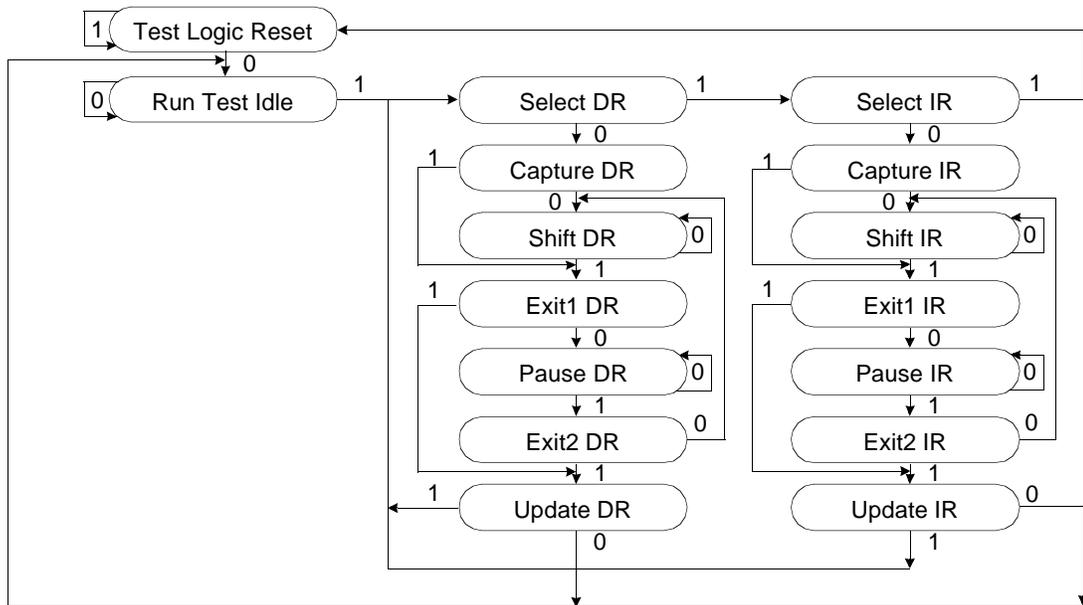
## SCAN REGISTER DEFINITION

| Part | Instruction Register | Bypass Register | ID Register | Boundary Scan |
|---|---|---|---|---|
| 128Kx36 | 3 bits | 1 bits | 32 bits | 70 bits |
| 256Kx18 | 3 bits | 1 bits | 32 bits | 51 bits |

## ID REGISTER DEFINITION

| Part | Revision Number (31:28) | Part Configuration (27:18) | Vendor Definition (17:12) | Samsung JEDEC Code (11: 1) | Start Bit(0) |
|---|---|---|---|---|---|
| 128Kx36 | 0000 | 00101 00100 | XXXXXX | 00001001110 | 1 |
| 256Kx18 | 0000 | 00110 00011 | XXXXXX | 00001001110 | 1 |

## BOUNDARY SCAN EXIT ORDER(x36)

| | | | | | | |
|---|---|---|---|---|---|---|
| 36 | 3B | $SA_9$ | | $SA_8$ | 5B | 35 |
| 37 | 2B | NC | | NC | 6B | 34 |
| 38 | 3A | $SA_{10}$ | | $SA_7$ | 5A | 33 |
| 39 | 3C | $SA_{11}$ | | $SA_6$ | 5C | 32 |
| 40 | 2C | $SA_{12}$ | | $SA_5$ | 6C | 31 |
| 41 | 2A | $SA_{13}$ | | $SA_4$ | 6A | 30 |
| 42 | 2D | $DQc_9$ | | $DQb_9$ | 6D | 29 |
| 43 | 1D | $DQc_8$ | | $DQb_8$ | 7D | 28 |
| 44 | 2E | $DQc_7$ | | $DQb_7$ | 6E | 27 |
| 45 | 1E | $DQc_6$ | | $DQb_6$ | 7E | 26 |
| 46 | 2F | $DQc_5$ | | $DQb_5$ | 6F | 25 |
| 47 | 2G | $DQc_4$ | | $DQb_4$ | 6G | 24 |
| 48 | 1G | $DQc_3$ | | $DQb_3$ | 7G | 23 |
| 49 | 2H | $DQc_2$ | | $DQb_2$ | 6H | 22 |
| 50 | 1H | $DQc_1$ | | $DQb_1$ | 7H | 21 |
| 51 | 3G | $\overline{SW}c$ | | $\overline{SW}b$ | 5G | 20 |
| 52 | 4D | ZQ | | $\overline{G}$ | 4F | 19 |
| 53 | 4E | $\overline{SS}$ | | K | 4K | 18 |
| 54 | 4G | NC | | $\overline{K}$ | 4L | 17 |
| 55 | 4H | NC | | $\overline{SW}a$ | 5L | 16 |
| 56 | 4M | $\overline{SW}$ | | $DQa_1$ | 7K | 15 |
| 57 | 3L | $\overline{SW}d$ | | $DQa_2$ | 6K | 14 |
| 58 | 1K | $DQd_1$ | | $DQa_3$ | 7L | 13 |
| 59 | 2K | $DQd_2$ | | $DQa_4$ | 6L | 12 |
| 60 | 1L | $DQd_3$ | | $DQa_5$ | 6M | 11 |
| 61 | 2L | $DQd_4$ | | $DQa_6$ | 7N | 10 |
| 62 | 2M | $DQd_5$ | | $DQa_7$ | 6N | 9 |
| 63 | 1N | $DQd_6$ | | $DQa_8$ | 7P | 8 |
| 64 | 2N | $DQd_7$ | | $DQa_9$ | 6P | 7 |
| 65 | 1P | $DQd_8$ | | ZZ | 7T | 6 |
| 66 | 2P | $DQd_9$ | | $SA_3$ | 5T | 5 |
| 67 | 3T | $SA_{14}$ | | $SA_2$ | 6R | 4 |
| 68 | 2R | $SA_{15}$ | | $SA_1$ | 4T | 3 |
| 69 | 4N | $SA_{16}$ | | $SA_0$ | 4P | 2 |
| | | | | | | |
| 70 | 3R | $M_1$ | | $M_2$ | 5R | 1 |

## BOUNDARY SCAN EXIT ORDER(x18)

| | | | | | | |
|---|---|---|---|---|---|---|
| 26 | 3B | $SA_9$ | | $SA_8$ | 5B | 25 |
| 27 | 2B | NC | | NC | 6B | 24 |
| 28 | 3A | $SA_{10}$ | | $SA_7$ | 5A | 23 |
| 29 | 3C | $SA_{11}$ | | $SA_6$ | 5C | 22 |
| 30 | 2C | $SA_{12}$ | | $SA_5$ | 6C | 21 |
| 31 | 2A | $SA_{13}$ | | $SA_4$ | 6A | 20 |
| | | | | $DQa_9$ | 6D | 19 |
| 32 | 1D | $DQb_1$ | | | | |
| 33 | 2E | $DQb_2$ | | | | |
| | | | | $DQa_8$ | 7E | 18 |
| | | | | $DQa_7$ | 6F | 17 |
| 34 | 2G | $DQb_3$ | | | | |
| | | | | $DQa_6$ | 7G | 16 |
| | | | | $DQa_5$ | 6H | 15 |
| 35 | 1H | $DQb_4$ | | | | |
| 36 | 3G | $\overline{SW}b$ | | | | |
| 37 | 4D | ZQ | | $\overline{G}$ | 4F | 14 |
| 38 | 4E | $\overline{SS}$ | | K | 4K | 13 |
| 39 | 4G | NC | | $\overline{K}$ | 4L | 12 |
| 40 | 4H | NC | | $\overline{SW}a$ | 5L | 11 |
| 41 | 4M | $\overline{SW}$ | | $DQa_4$ | 7K | 10 |
| | | | | | | |
| | | | | | | |
| 42 | 2K | $DQb_5$ | | $DQa_3$ | 6L | 9 |
| 43 | 1L | $DQb_6$ | | | | |
| | | | | | | |
| 44 | 2M | $DQb_7$ | | $DQa_2$ | 6N | 8 |
| 45 | 1N | $DQb_8$ | | $DQa_1$ | 7P | 7 |
| | | | | | | |
| | | | | ZZ | 7T | 6 |
| 46 | 2P | $DQb_9$ | | $SA_3$ | 5T | 5 |
| 47 | 3T | $SA_{14}$ | | $SA_2$ | 6R | 4 |
| 48 | 2R | $SA_{15}$ | | | | |
| 49 | 4N | $SA_{16}$ | | $SA_1$ | 4P | 3 |
| 50 | 2T | $SA_{17}$ | | $SA_0$ | 6T | 2 |
| 51 | 3R | $M_1$ | | $M_2$ | 5R | 1 |

**NOTE** : 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

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## JTAG DC OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | 3.15 | 3.3 | 3.45 | V | |
| Input High Level | $V_{IH}$ | 2.0 | - | $V_{DD}$+0.3 | V | |
| Input Low Level | $V_{IL}$ | -0.3 | - | 0.8 | V | |
| Output High Voltage($I_{OH}$=-2mA) | $V_{OH}$ | 2.4 | - | $V_{DD}$ | V | |
| Output Low Voltage($I_{OL}$=2mA) | $V_{OL}$ | $V_{SS}$ | - | 0.4 | V | |

**NOTE** : 1. The input level of SRAM pin is to follow the SRAM DC specification.

## JTAG AC TEST CONDITIONS

| Parameter | Symbol | Min | Unit | Note |
|---|---|---|---|---|
| Input High/Low Level | $V_{IH}/V_{IL}$ | 3.0/0.0 | V | |
| Input Rise/Fall Time | TR/TF | 2.0/2.0 | ns | |
| Input and Output Timing Reference Level | | 1.5 | V | 1 |

**NOTE** : 1. See SRAM AC test output load on page 5.

## JTAG AC Characteristics

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| TCK Cycle Time | $t_{CHCH}$ | 50 | - | ns | |
| TCK High Pulse Width | $t_{CHCL}$ | 20 | - | ns | |
| TCK Low Pulse Width | $t_{CLCH}$ | 20 | - | ns | |
| TMS Input Setup Time | $t_{MVCH}$ | 5 | - | ns | |
| TMS Input Hold Time | $t_{CHMX}$ | 5 | - | ns | |
| TDI Input Setup Time | $t_{DVCH}$ | 5 | - | ns | |
| TDI Input Hold Time | $t_{CHDX}$ | 5 | - | ns | |
| SRAM Input Setup Time | $t_{SVCH}$ | 5 | - | ns | |
| SRAM Input Hold Time | $t_{CHSX}$ | 5 | - | ns | |
| Clock Low to Output Valid | $t_{CLQV}$ | 0 | 10 | ns | |

## JTAG TIMING DIAGRAM

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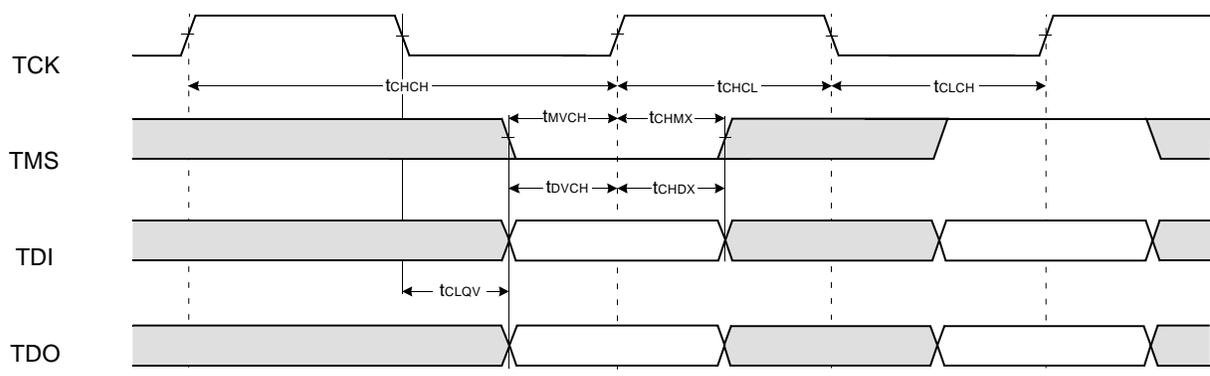
## 119 BGA PACKAGE DIMENSIONS
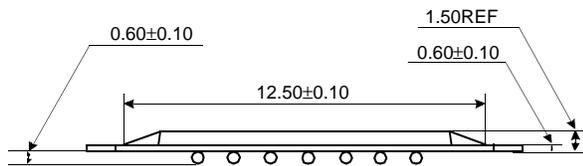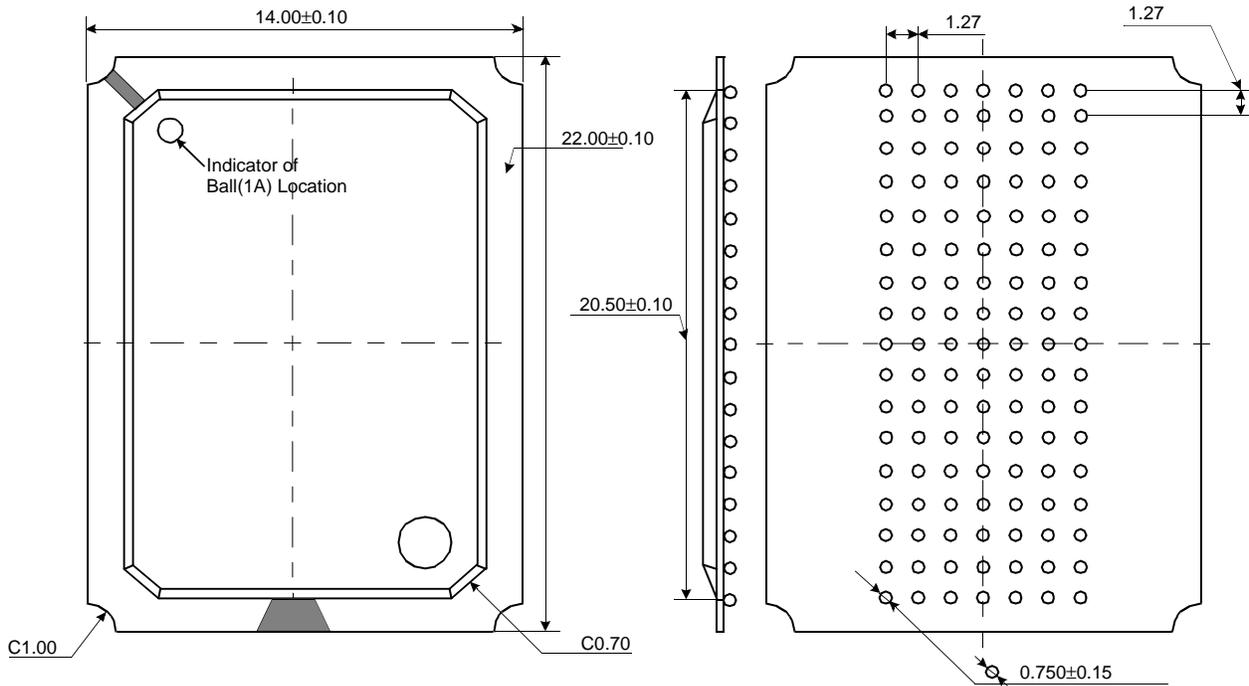


**NOTE** :
1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

## 119 BGA PACKAGE THERMAL CHARACTERISTICS

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Junction to Ambient(at air flow of 1m/sec) | Theta_JA | - | - | 17 | °C/W | |
| Junction to Case | Theta_JC | - | - | 4 | °C/W | |
| Junction to Solder Ball | Theta_JB | - | - | 10 | °C/W | |